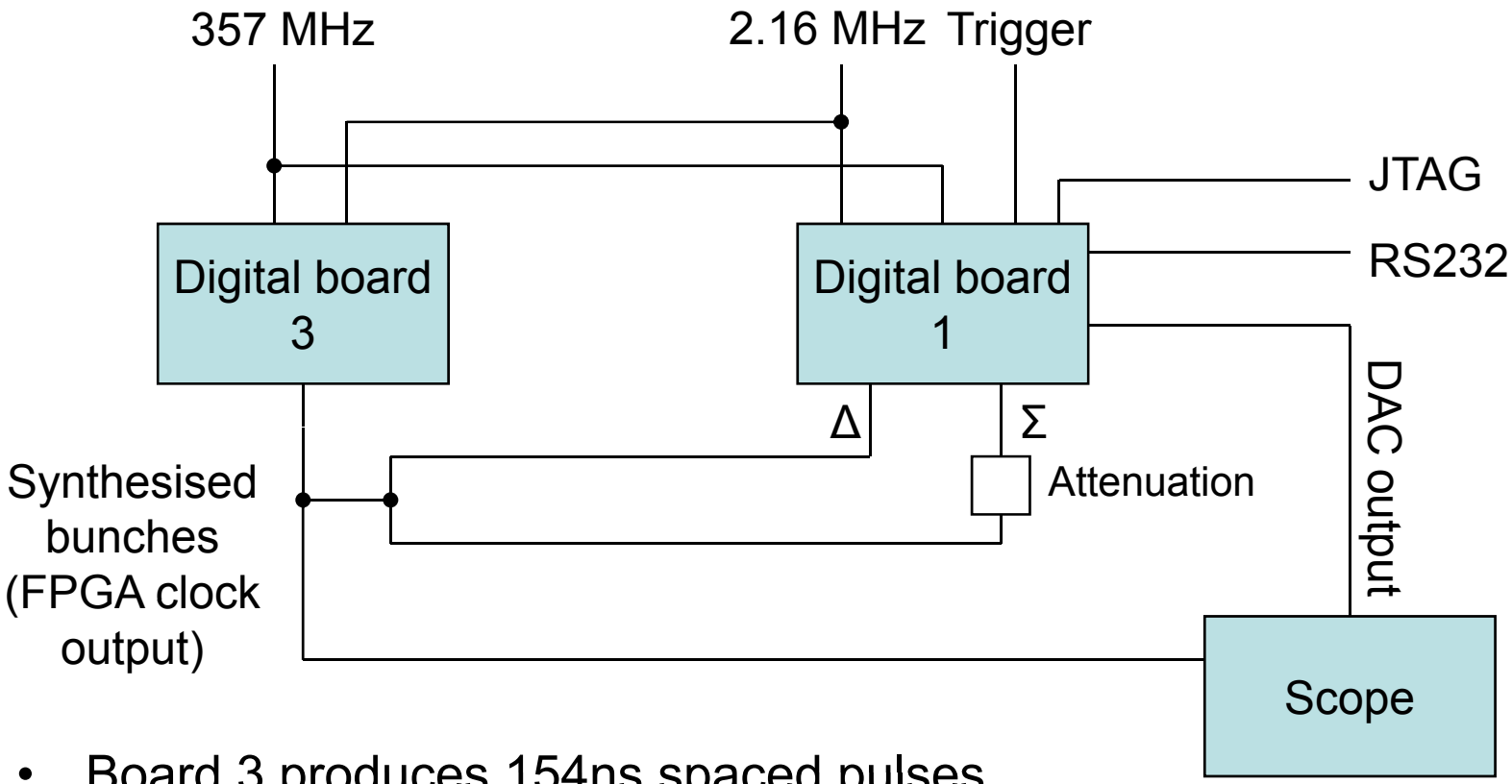
Test benching at ATF

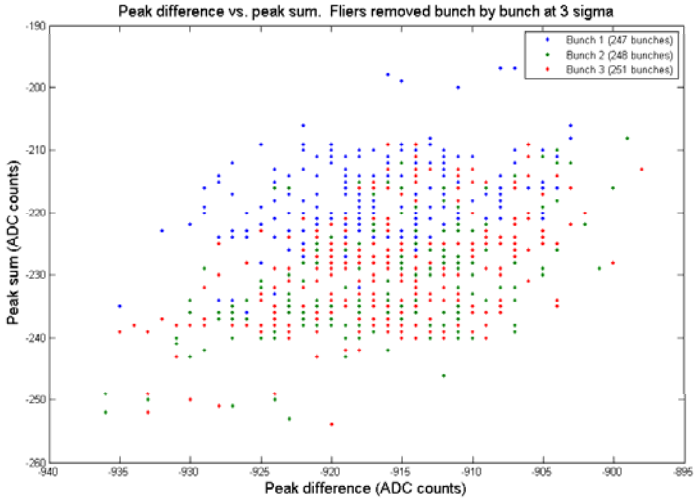


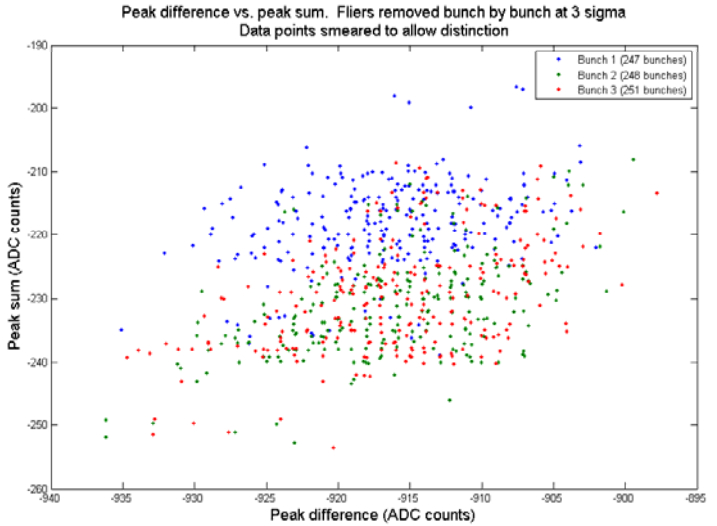
- Board 3 produces 154ns spaced pulses
- Board 1 runs FONT4 firmware
- Currently locked to all 2.16MHz cycles – will soon use ATF trigger to select a cycle

Test results so far

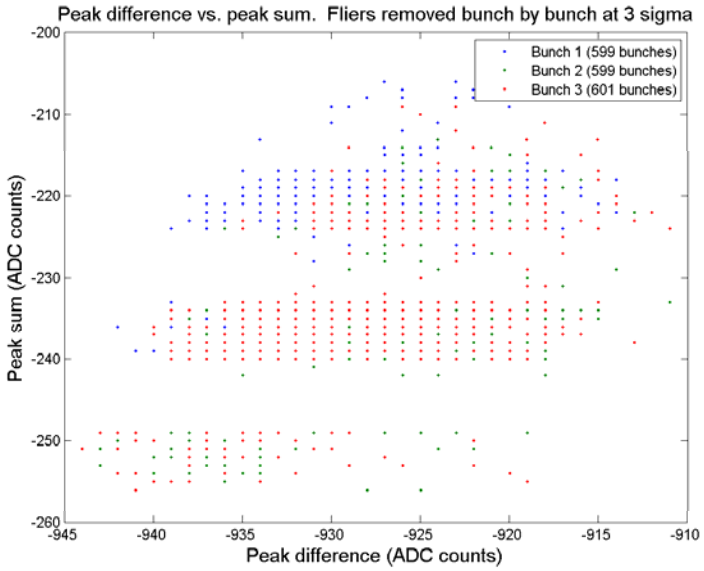
- Once set up, began DAC investigation
- Able to change bunch sample sent to DAC
- Qualitatively sensible feedback signals seen
  - Signals of correct and consistent polarity (unlike last week's plot)
  - Tested both with and without charge normalisation
- Will get quantitative confirmation this week
  - Vary attenuation on sum and difference inputs
  - Log DAC output

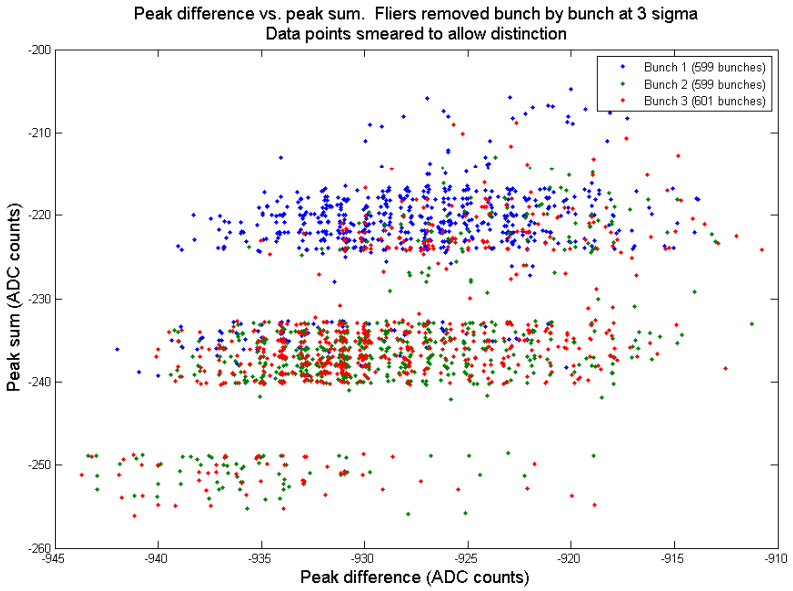
- First data run with modified firmware





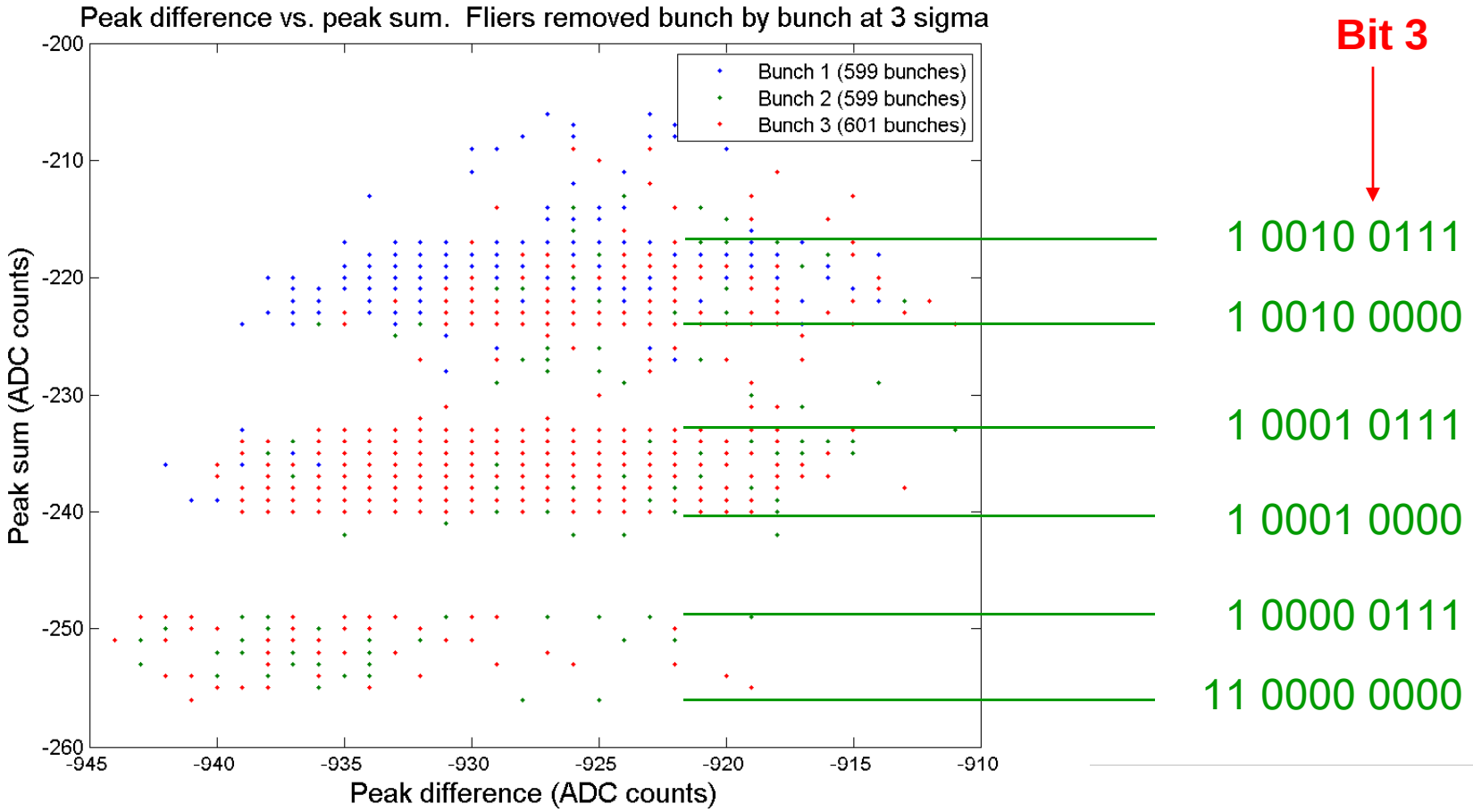
- Second data run with the same FPGA bitstream





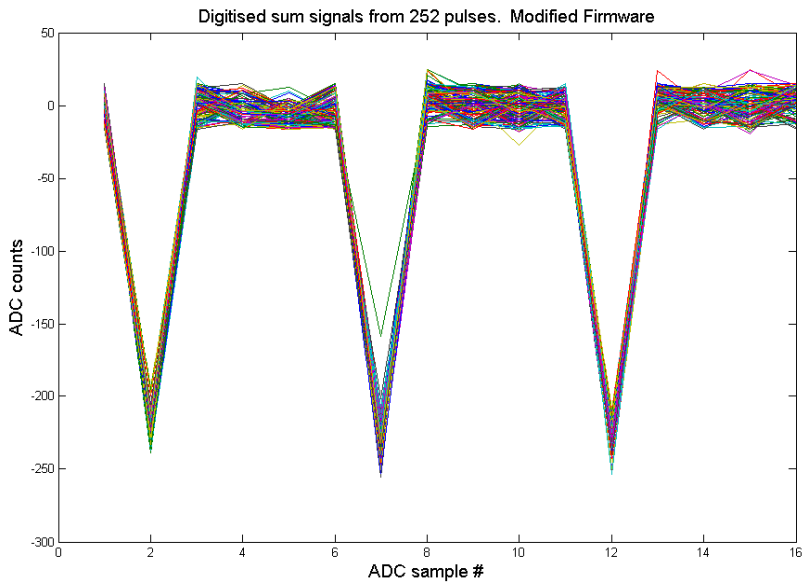
Sum signal banding

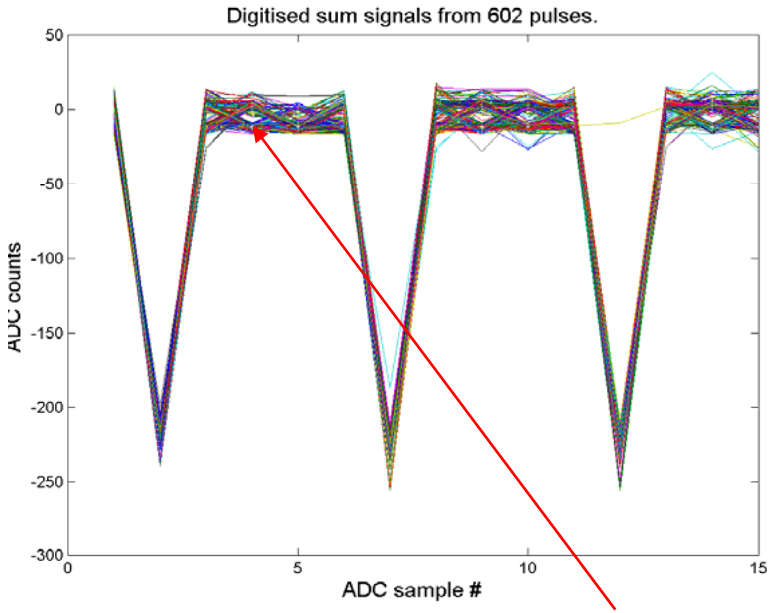
- Bit 3 tending to zero during second run



Other anomalies

- First run (left) and second run (right) overlayed sums (same runs as slide 3)





- Must suspect bit errors again

'Eyes' in noise region

Possible cause

- This behaviour not seen in March 08
- However, modifying firmware reduced FPGA timing slack (357 MHz distribution) by factor of 2
  - March: slack 33ps
  - Modified: slack 17ps
- Suspect timing is too tight for consistent operation
- Investigating options at present
  - e.g. Manually editing FPGA LUTs of well timed firmware
- Will attempt to confirm this using test bench

Update on sum / difference signal widths

- Last week's scan over BPM processor pulse results
  - Difference pulse of different width to sum pulse (scope)
  - Gaussian fit of difference from ADC didn't match scope
- However, BPM processor was in non-linear regime
  - Colin believes the pulse would be broadened and flattened
  - ADC scanned only flattened peak, hence fit problems
  - Sum signal much smaller → better fit