Silicon tracker – Update

ILD detector optimization – May 14th 2008

Marcel Vos (IFIC Valencia) for the SiLC collaboration,
thanks to V. Saveliev, A. Savoy-Navarro

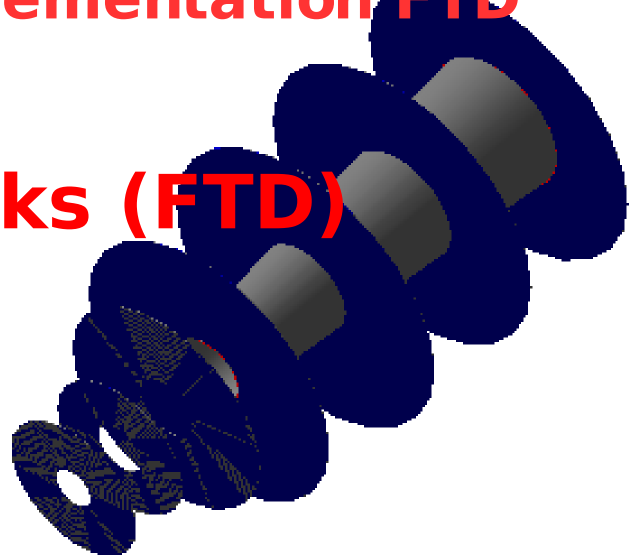
Inner silicon: Mokka implementation FTD

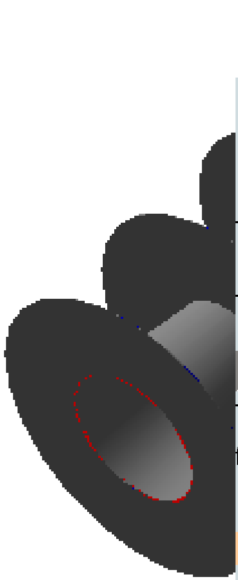
Forward Tracking Disks (FTD)

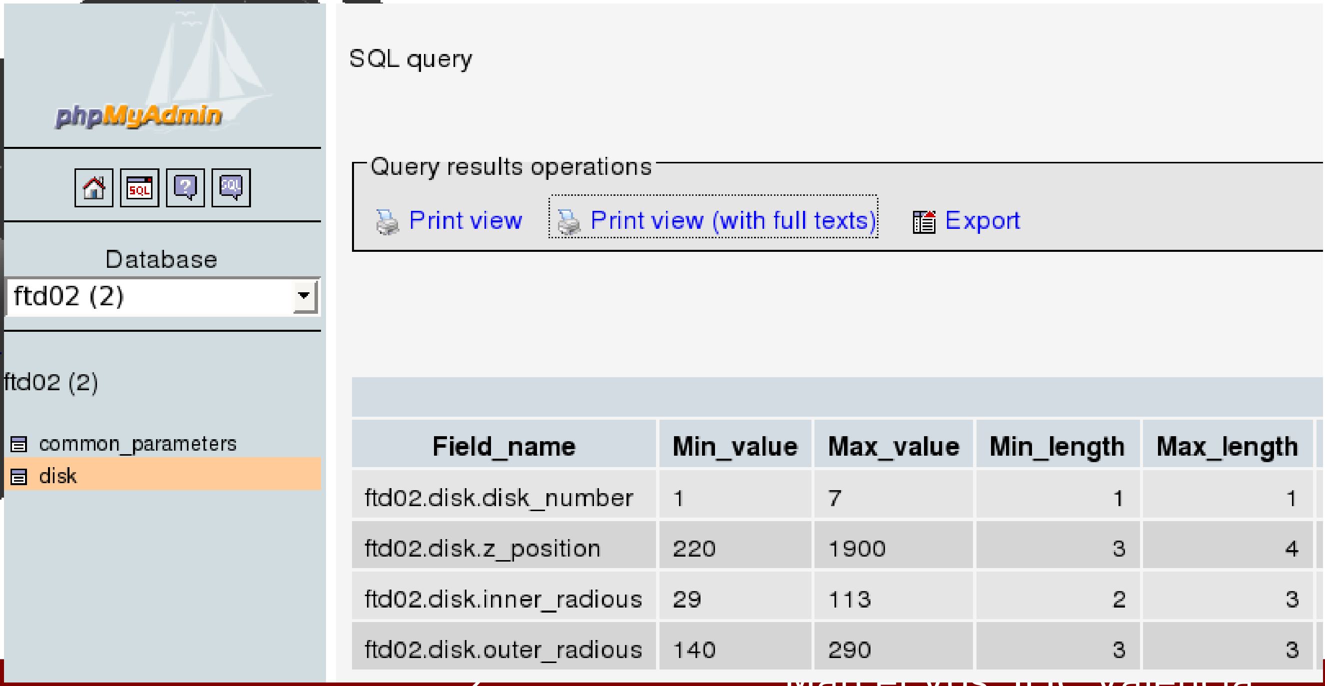
3 pixel disks (1 % X_0)

4 strip disks (0.5 % X_0)

extended layout wrt TESLA







Field_name	Min_value	Max_value	Min_length	Max_length
ftd02.disk.disk_number	1	7	1	1
ftd02.disk.z_position	220	1900	3	4
ftd02.disk.inner_radious	29	113	2	3
ftd02.disk.outer_radious	140	290	3	3

The silicon tracker elements

The silicon tracker geometry and material have been implemented in Mokka

With limitations: lack of detail in the services (= overly optimistic?)

With flaws: outermost silicon (SET, ETD) represented by circular structures, should follow the ECAL face

Digitization

Now, what about digitization?

Very detailed digitizer developed by Zbynek Drasal. Too detailed for current goals and for the level of detail of the ILD design.

Feed best guesses of spatial resolution and integration time into simple digitizer (based on Gaussian smearing of simulated hit position + some way to select hits from a time window).

SIT

	radius	half-length	thickness	R-ϕ resolution	z-resolution	Read-out time
SIT layer 1	160 mm	380 mm	275 μm Si + 1 mm C	4 μm	50 μm	1 BX
SIT layer 2	270 mm	660 mm	275 μm Si + 1 mm C	4 μm	50 μm	1 BX

Each of these detector layers consists of active material (275 μm Si), and a second cylinder – closely spaced to the active material - that represents the detector support structure and services (1 mm C). Each layer thus presents 0.5 % of a radiation length to perpendicularly incident tracks.

In the baseline option, the SIT layers are to be equipped with double-sided micro-strip detectors, where strips of both sides are placed at a small stereo angle (baseline option). The detector design should aim for an excellent R-ϕ resolution, as good as 4 μm. The requirement on the precision of the z-measurement is somewhat more relaxed. The possibility of using pixel sensors is being investigated, which would lead to a much improved resolution in this second coordinate. The default values for the R-ϕ and z-resolution to be used in the digitization of simulated data are given in the table.

SIT

Simulation | Digitization

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EXPLANATION

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SET

	radius	half-length	thickness	R-ϕ resolution	z-resolution	Read-out time
SET layer 1	1587.5 mm	1500.0 mm	275 µm Si + 1 mm C	7 µm	100 µm	1 BX
SET layer 2	1592.5 mm	1500.0 mm	275 µm Si + 1 mm C	7 µm	100 µm	1 BX

FTD

	z-value	Inner radius	Outer radius	thickness	R-ϕ resolution	z-resolution	Read-out time
FTD disk 1	220 mm	29.0 mm	140.0	50 μm	7 μm	100 μm	~ 10s BX
FTD disk 2	350 mm	32.0 mm	210.0	50 μm	7 μm	100 μm	~ 10s BX
FTD disk 3	500 mm	35.0 mm	270.0	50 μm	7 μm	100 μm	~ 10x BX
FTD disk 4	850 mm	51.0 mm	290.0	275 μm	7 μm	1000 μm	1 BX
FTD disk 5	1200 mm	72.0 mm	290.0	275 μm	7 μm	1000 μm	1 BX
FTD disk 6	1550 mm	93.0 mm	290.0	275 μm	7 μm	1000 μm	1 BX
FTD disk 7	1900 mm	113.0 mm	290.0	275 μm	7 μm	1000 μm	1 BX

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FTD disk 1	220 mm	29.0 mm	140.0	50 μm	7 μm	100 μm	~ 10s BX
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FTD disk 3	500 mm	35.0 mm	270.0	50 μm	7 μm	100 μm	~ 10x BX
FTD disk 4	850 mm	51.0 mm	290.0	275 μm	7 μm	1000 μm	1 BX
FTD disk 5	1200 mm	72.0 mm	290.0	275 μm	7 μm	1000 μm	1 BX
FTD disk 6	1550 mm	93.0 mm	290.0	275 μm	7 μm	1000 μm	1 BX
FTD disk 7	1900 mm	113.0 mm	290.0	275 μm	7 μm	1000 μm	1 BX

ETD

	z-value	Inner radius	Outer radius	thickness	resolution	Read-out time
ETD disk 1	2368 mm	305.0 mm	1500.0?	275 µm Si + 1 mm C	7 µm U	1 BX
ETD disk 2	2368 mm	305.0 mm	1500.0?	275 µm Si + 1 mm C	7 µm V	1 BX
ETD disk 3	2368 mm	305.0 mm	1500.0?	275 µm Si + 1 mm C	7 µm X	1 BX

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Summary

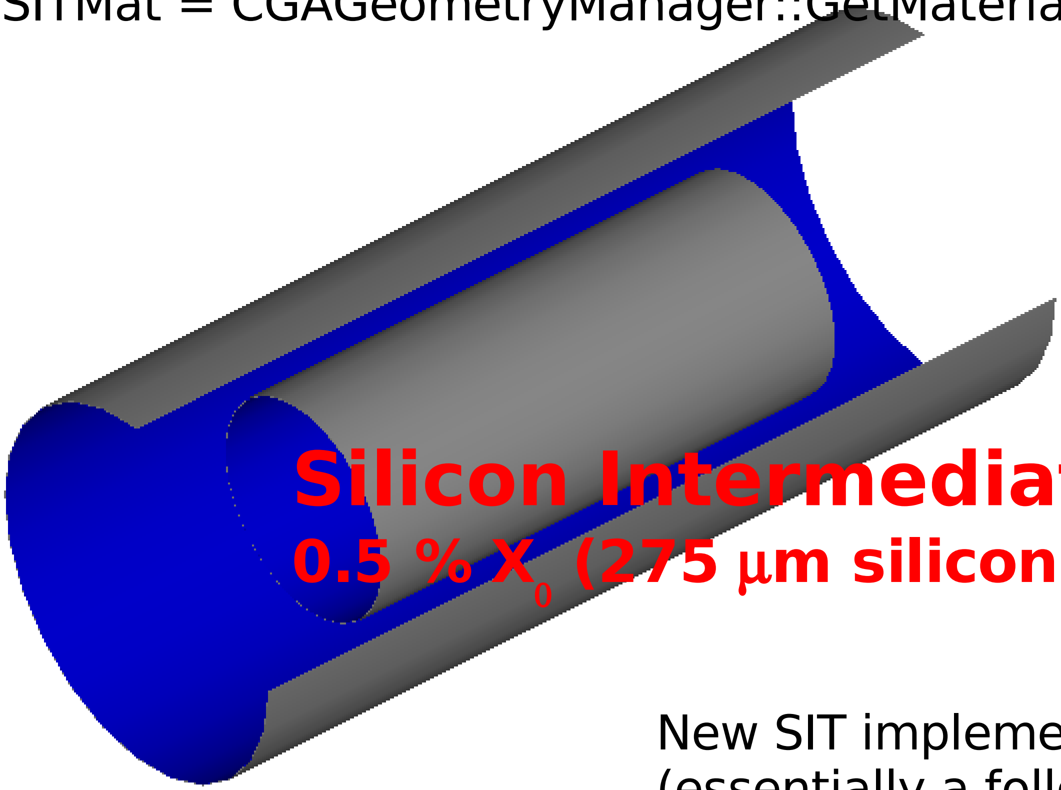
SiLC has provided a list of digitization parameters for all four sub-detectors: propose to use these for large MC production

Different from what was there: impact on tracking?

Inner silicon: Mokka implementation SIT

```
// sensitive silicon cylinders...
G4Tubs *SitSolid = new G4Tubs("Sit",
                    inner_radious, inner_radious+sensitive_thickness,
                    half_z, start_phi, stop_phi);

SITMat = CGAGeometryManager::GetMaterial("silicon_2.33gccm");
```

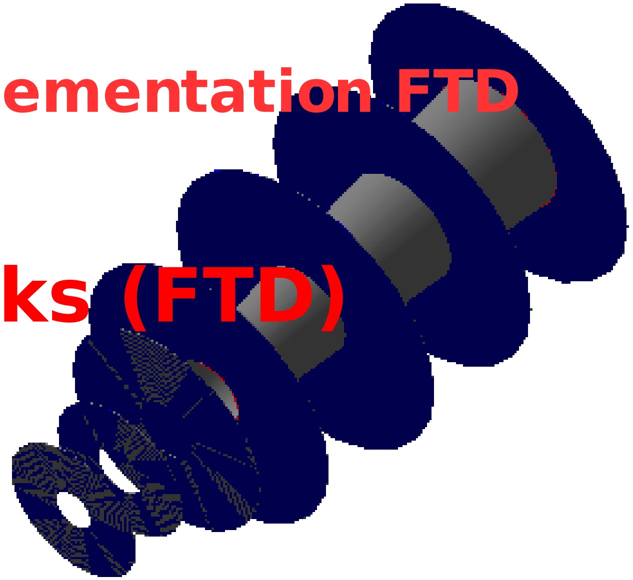


Silicon Intermediate Tracker (SIT)

0.5 % X_0 (275 μm silicon + 1mm C support)

New SIT implementation by Valeri Saveliev
(essentially a follow-up of Hengne Li's work)

Inner silicon: Mokka implementation FTD

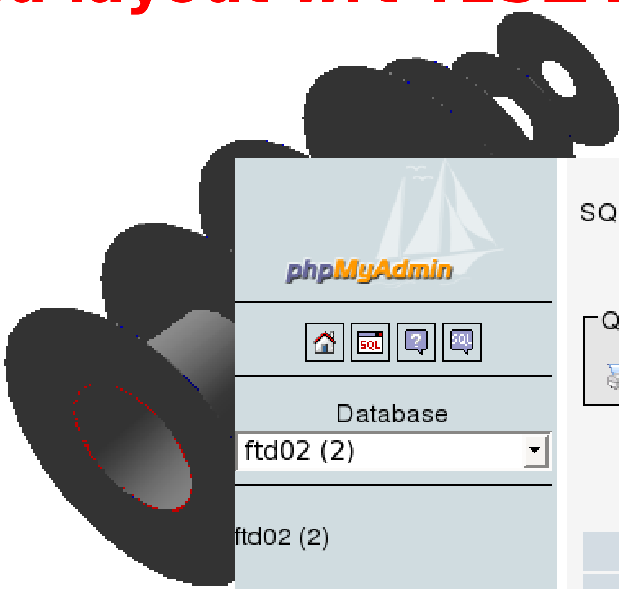


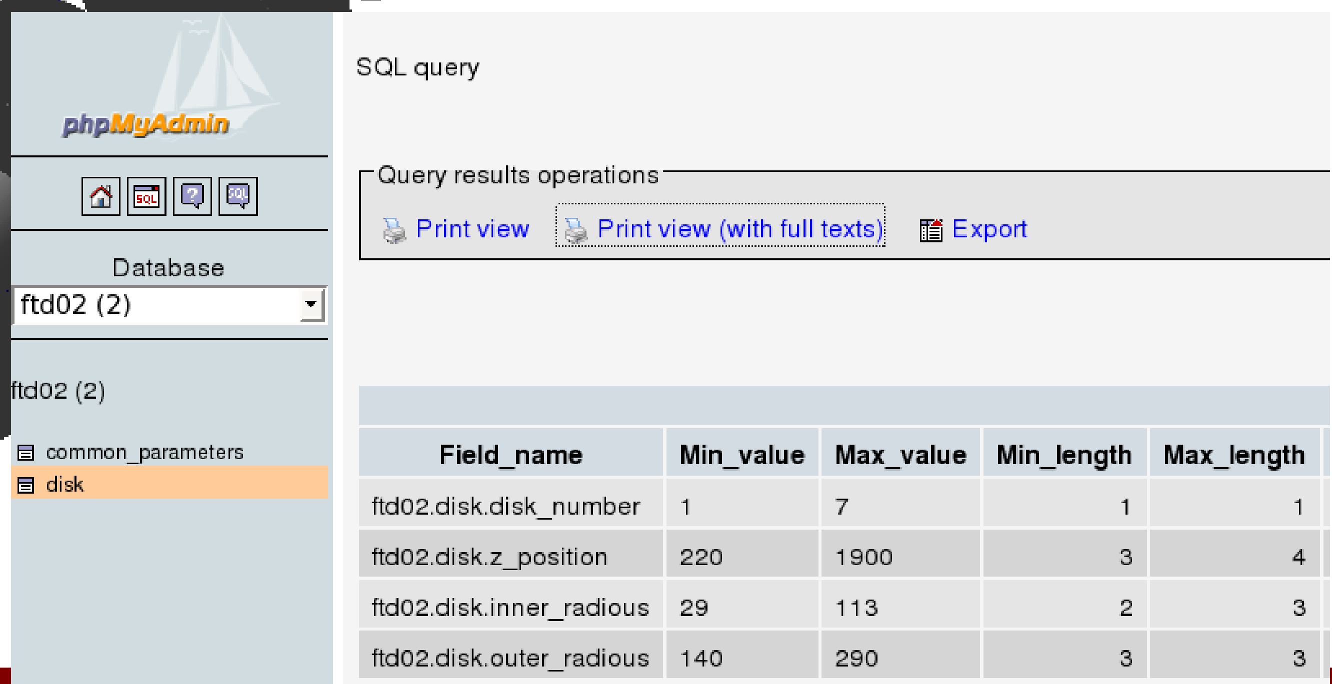
Forward Tracking Disks (FTD)

3 pixel disks (1 % X_0)

4 strip disks (0.5 % X_0)

extended layout wrt TESLA





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FTD parameters

Disk number	1	2	3	4	5	6	7
Z-position	220	350	500	850	1200	1550	1900
Inner radius	29	32	35	51	72	93	113
Outer radius	140	210	270	290	290	290	290

Reduced to accomodate for SIT cylinders

Matching TPC inner radius. Should this be reduced?

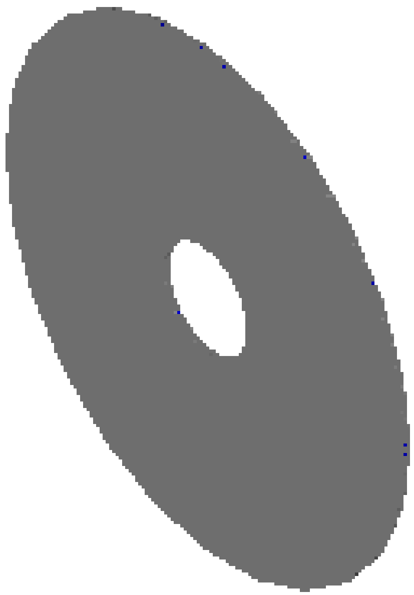
Covering ~ full length of TPC

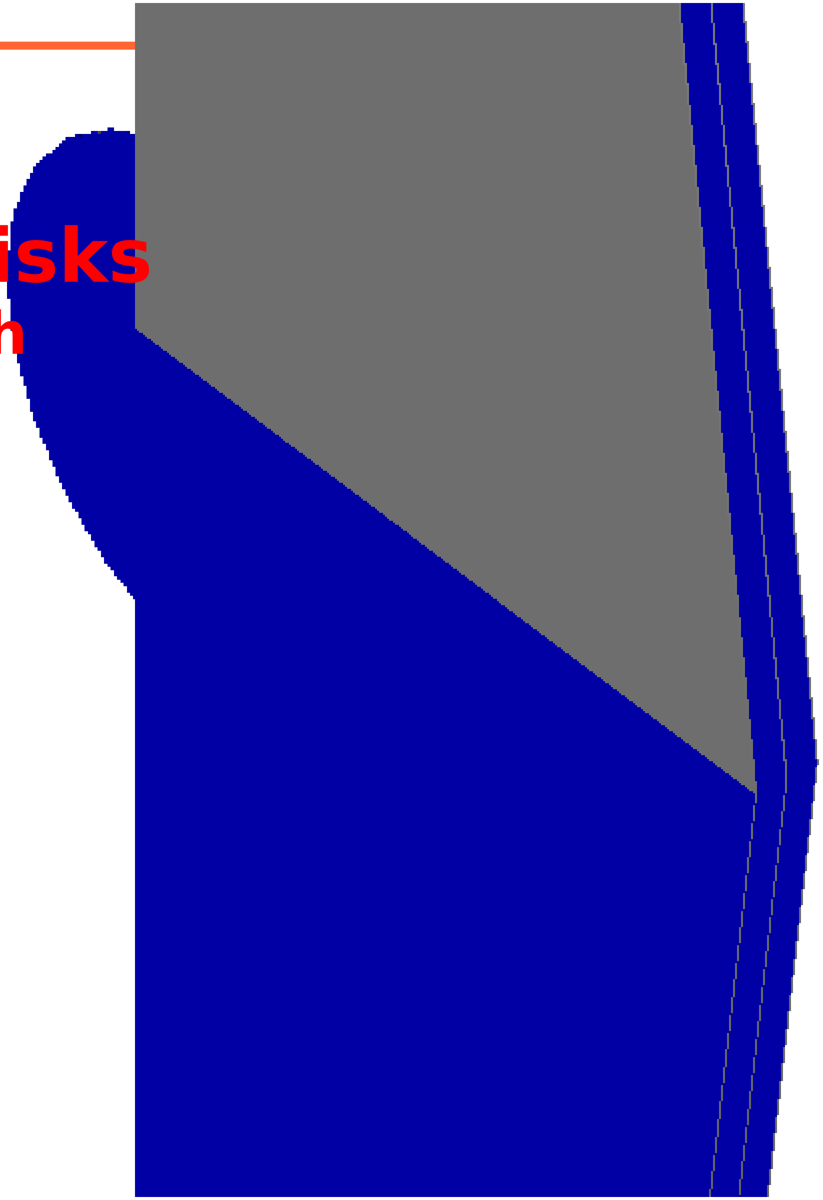
ETD Mokka implementation

End-cap tracking disks

Silicon – carbon sandwich

3 XUV layers x 0.65 % X_0



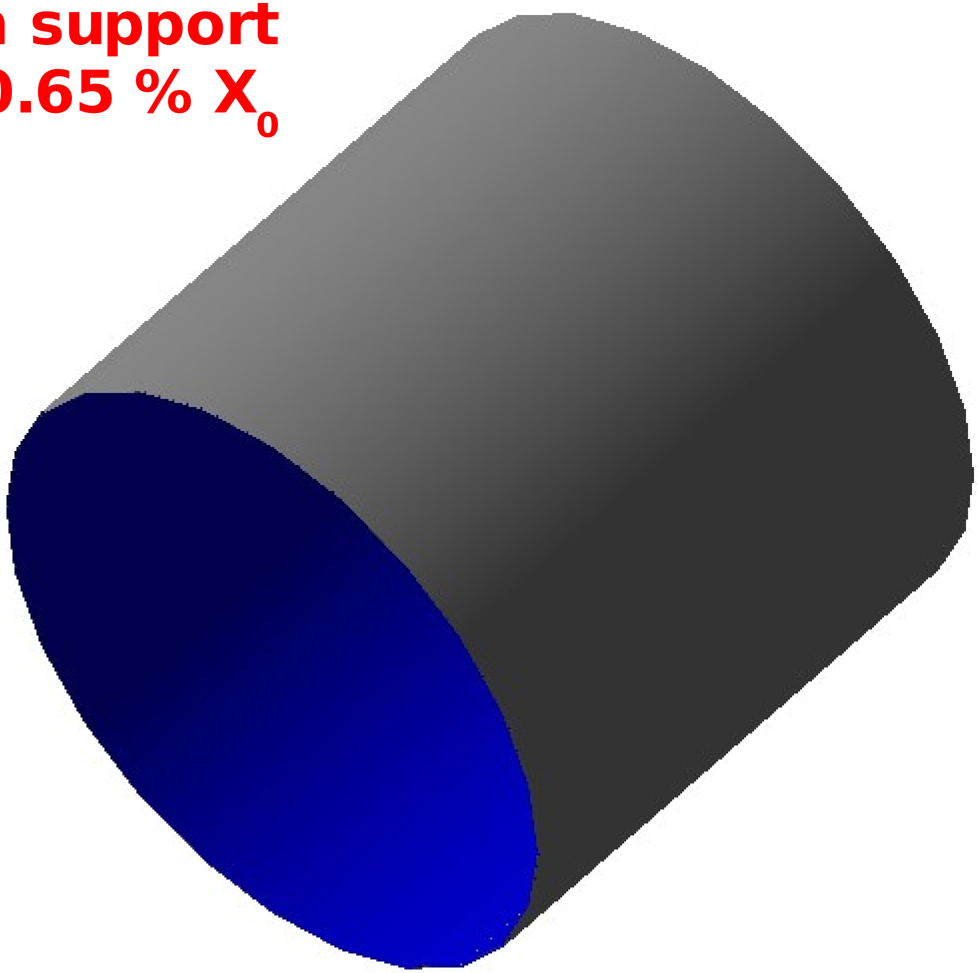


SET Mokka implementation

Silicon External Tracker

Silicon + carbon support

2 XUV layers x 0.65 % X_0



LDC/GLD convergence to ILD

LDCPrime

Sub-Detector	Parameter	GLD	LDC	GLD’	LDC’
TPC	R_{inner} (m)	0.45	0.30	0.45	0.30
	R_{outer} (m)	2.00	1.58	1.80	1.80
	Z_{max} (m)*	2.50	2.16	2.35	2.35
Barrel ECAL	R_{inner} (m)**	2.10	1.60	1.85	1.82
	Material	Sci/W	Si/W	Sci/W	Sci/W
Barrel HCAL	Material	Sci/W	Sci/Fe	Sci/Fe	Sci/Fe
Endcap ECAL	Z_{min} (m)***	2.80	2.30	2.55	2.55
Solenoid	B-field	3.0	4.0	3.50	3.50
VTX	Inner Layer (mm)	20	16	18	18

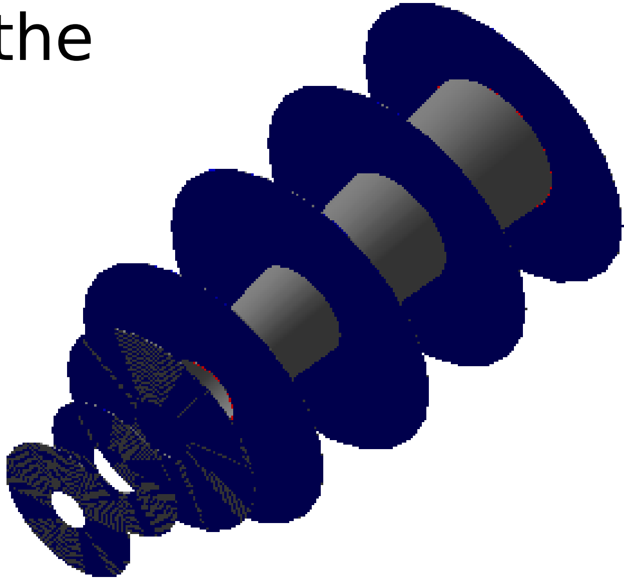
From Frank Gaede, December 6th.

Convergence for detector parameters linked to B or R. TPC inner radius or innermost silicon unchanged in “Primed” layouts

Material

The principal challenge is reducing the material to the bare minimum

Final detector optimisation must be done with realistic estimates for detector elements, support and services



Now: evaluate sensitivity of physics programme to increased material by defining a pessimistic scenario?

TPC inner radius

A crucial decision on the path to the LOI. Particularly important for the design of the inner silicon tracker (SIT/BIT) and (FTD/FIT)

The TPC geometries of GLDPrime and LDCPrime in the excel file sent by Jenny List last December:

inner radius; 39.5 cm (GLD') 30.05 cm (LDC')

inner radius sensitive volume; 43.0 cm (GLD') 37.1 cm (LDC')

Final TPC inner radius depends on a large number of issues:

Engineering constraints: Opening scenario foresees TPC to slide over Beam Delivery System. TPC Inner radius therefore limited by size of BDS.

Technology constraints: minimal TPC radius to cope with background and positive ion flux, minimal thickness (cm) of the TPC field cage?

Tracking performance: central detector global performance benefits from reduction in material associated with small TPC radius, forward track matching between FTD and TPC benefits from larger inner radius, two-track resolution in jets

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Central tracking

Precise space points in SIT/BIT are needed to bridge the gap between VXD and TPC

- for momentum resolution
- for pattern recognition (non-prompt tracks)

How many layers are needed clearly depends on the width of the gap.

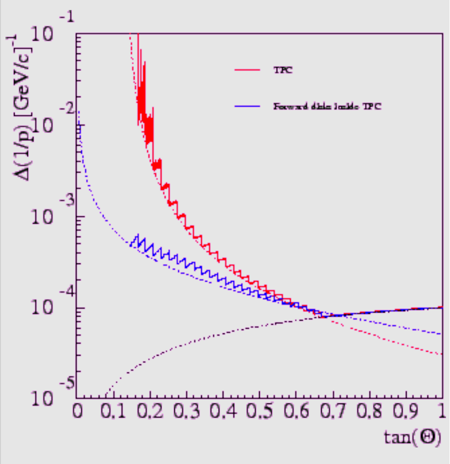
The impact of additional layers on tracking is well-established, but the effect of the material on global performance needs to be evaluated.

Forward tracking

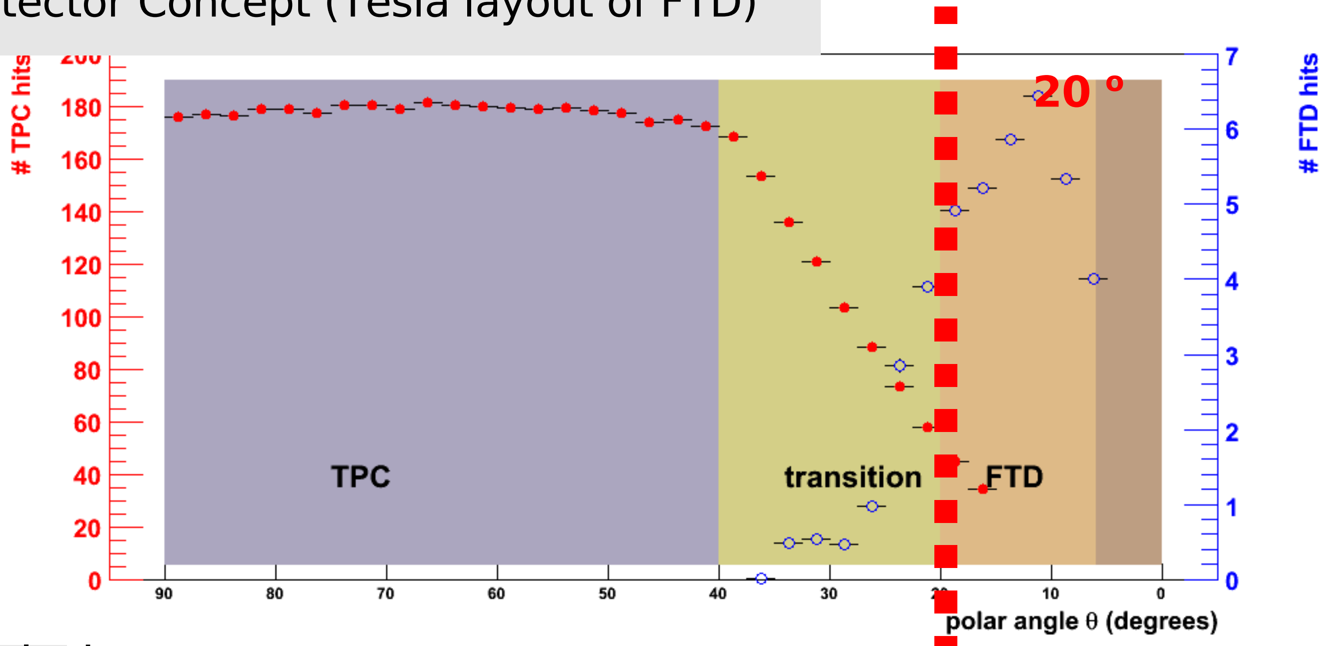
(Very) forward tracking in a gaseous + silicon tracker

For track polar angles below 40º reduced TPC coverage
Below ~ 30º FTD starts to contribute
Below ~ 20º FTD dominates the measurements

TPC/FTD hits vs. polar angle Large Detector Concept (Tesla layout of FTD)



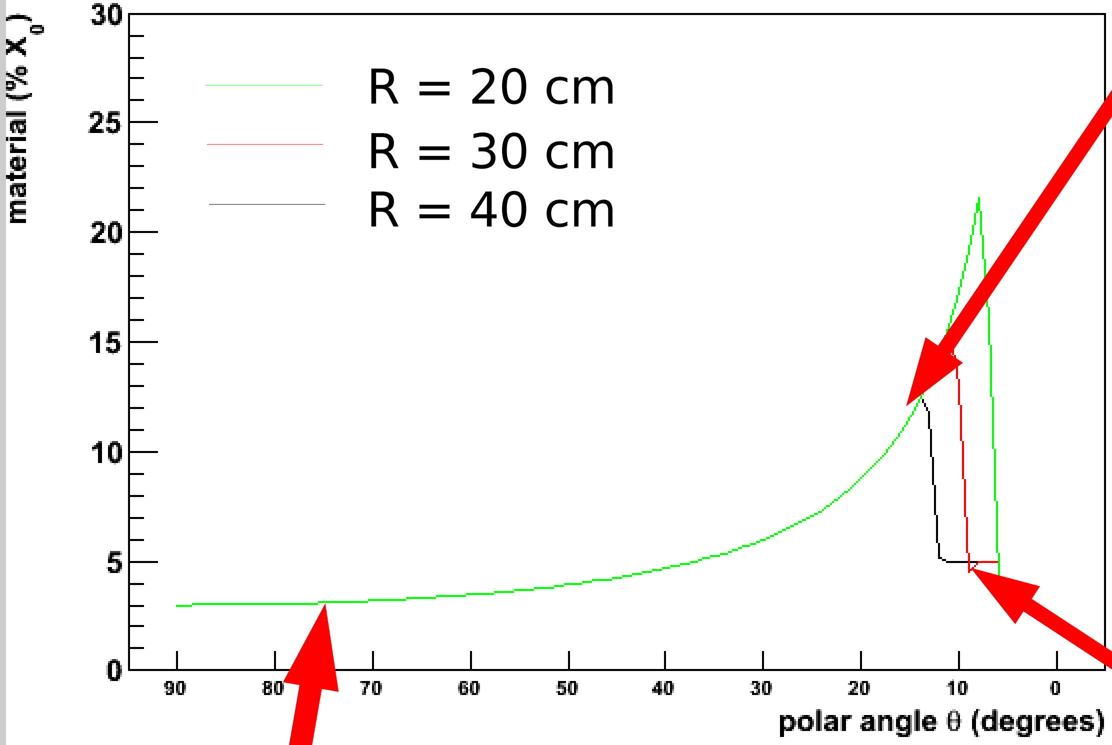
SGV momentum resolution



Full Mokka simulation + Marlin reconstruction

Forward tracking

Connection FTD – TPC at small angle becomes more difficult for small TPC inner radius



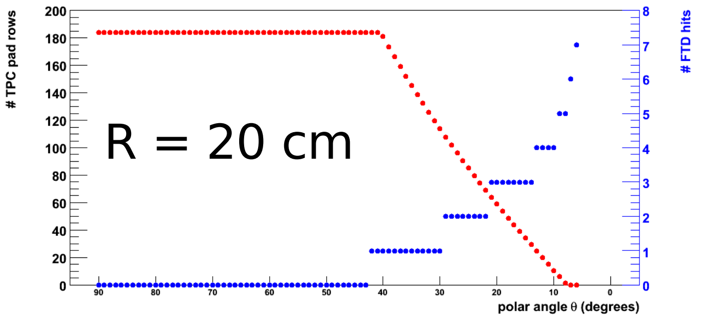
1/sin θ increase of the path length through the TPC entrance

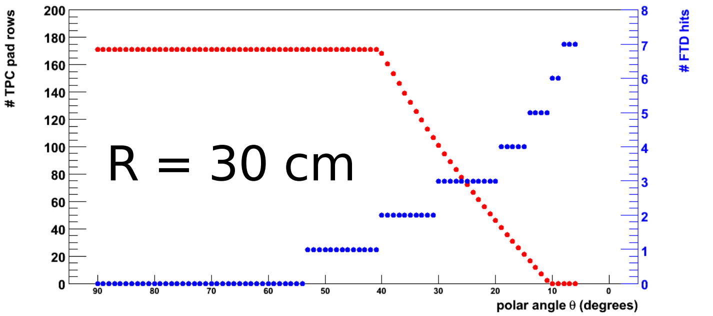
Return to flat FTD material

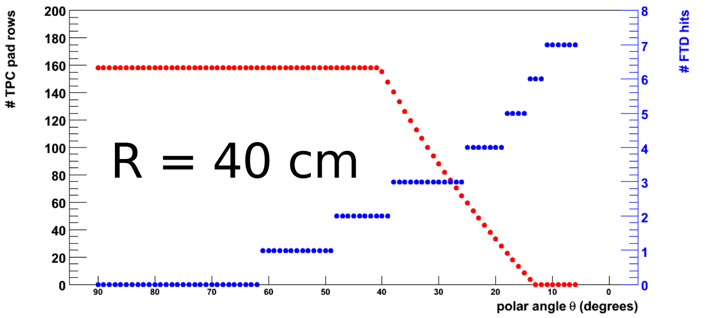
Assume 3 % X0 in TPC field cage + VXD/SIT services on perpendicular traversal

Forward Tracking

Number of TPC read-outs vs number of Silicon layers







A TPC of outer radius of 170 cm and a length of 200 cm is considered. A pad row width of 7.8 mm is considered (note that this is a more conservative assumption than keeping the number of pad rows constant). For the FTD and SIT layout the one in LDC01_05Sc is used. The inner radius of the TPC is varied, taking values of 20, 30 and 40 cm. SIT and FTD are simply squashed (all z-values remain the same, but the outer radii are scaled to match the varying TPC radius). The number of pad rows and FTD layers can now be counted as a function of polar angle.

LDC/GLD

Apart from TPC inner radius and the number of layers in SIT and BIT, important differences between both concepts occur in:

FTD/FIT: FTD covers full length of LDC TPC, FIT is much shorter

ETD: Encap Tracking Disks may consist of multiple layers in GLD

SET: not present in GLD

A starting point for the discussion between the GLD and LDC members of SILC. Expect to come up with a real plan in Sendai.

Silicon tracker parameters for optimization

The questions we would like to see answered in the next year(s)

Parameter	Affects	Changed in	LDC/GLD differences
Material	Overall performance, PatRec	Mokka description	All
Number of layers	All aspects	Mokka description	SIT, ETD
Layout	Momentum resolution	Mokka description	FTD
Rϕ resolution	Momentum resolution	Digitizer	FTD, ETD
R/z segmentation	Pattern recognition	Digitizer	SIT, FTD

Comparison of physics impact of optimistic/pessimistic scenarios for material in SIT/FTD, integrated scenarios for TPC endplate material (ETD), VXD services (FTD)?

Basic tracking performance studies varying TPC inner radius/number of SIT layers?

Other parameters: small-scale dedicated productions could be very interesting.

Conclusions

SiLC has provided the layout of SIT, FTD, ETD and SET.

Analysis of differences between GLD and LDC within SiLC ongoing.

The LOI exercise provides important tools for physics optimization of key parameters of silicon tracker elements.