IN2P3

Omega

LAL LPNHE

Digital Interface inside ASICs
&
Improvements for ROC Chips

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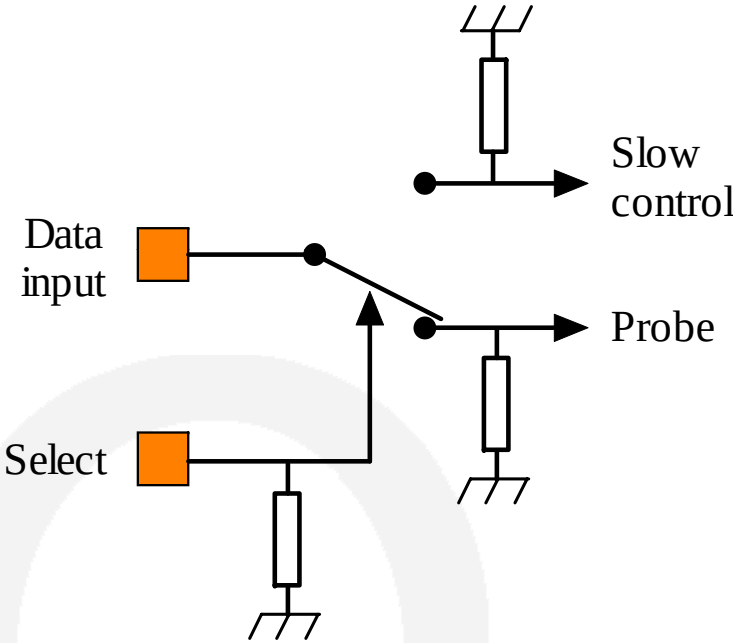
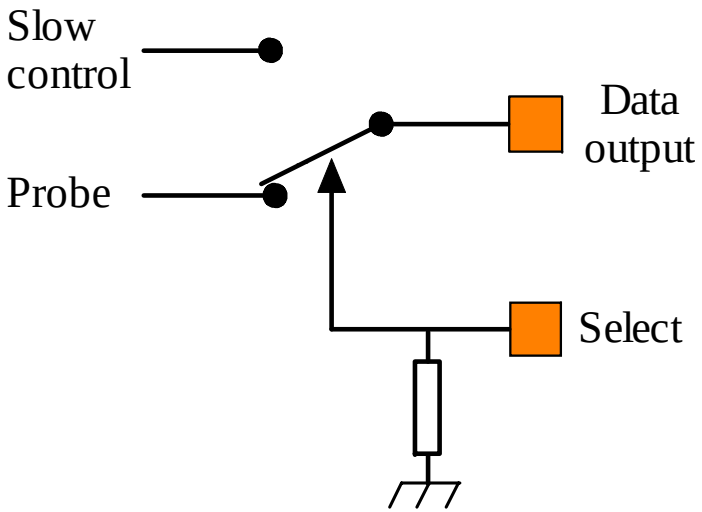
Probe and Slow Control shift registers: Multiplex

- Multiplex these 2 registers (in, out, clock, reset) ➔ save PADS (8 ➔ 4+1)

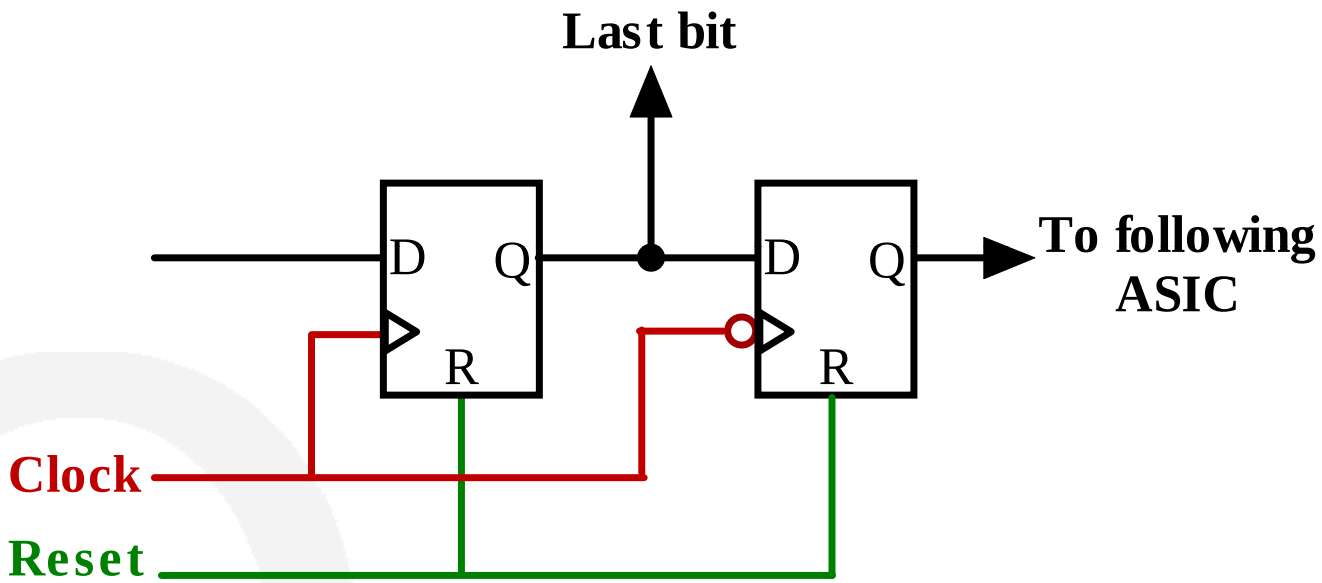




- Select line added : default register is probe to prevent glitch on SC

Probe and Slow Control shift registers: Extra FF

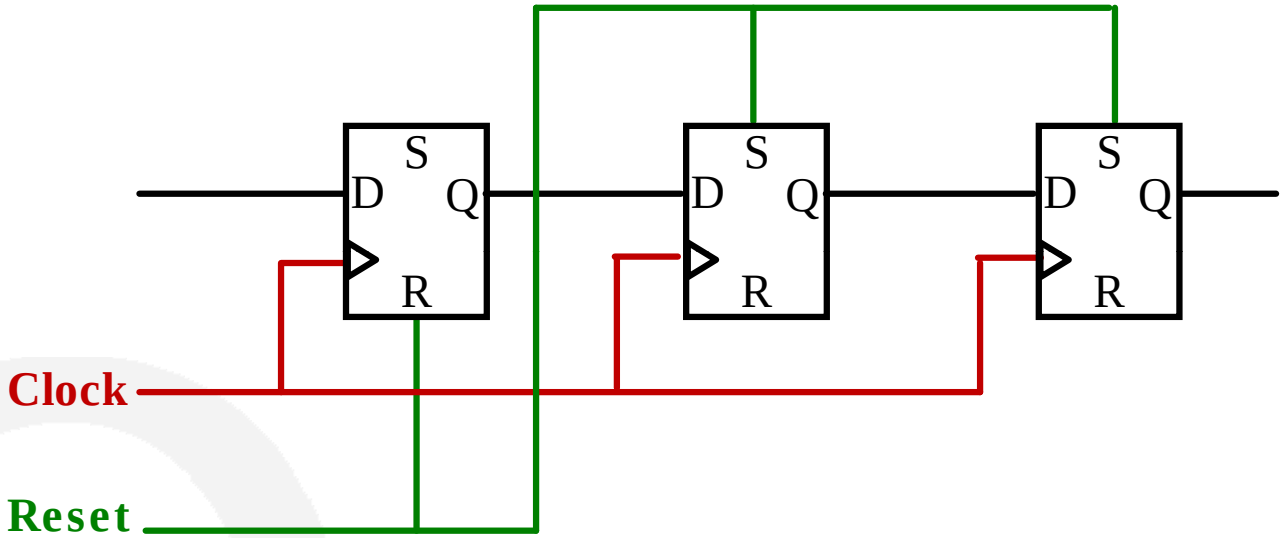
- Improve shift registers daisy chain between ASICs:
  - Add opposite edge FF at the end of shift registers



- Chip “N” sends data at falling edge and chip “N+1” captures at rising edge (time margin = half period clock)
- Inside chip ➔ use clock reversing to prevent timing problem

Slow Control shift registers: default configuration

- Use Set / Reset of Flip-Flops for default configuration



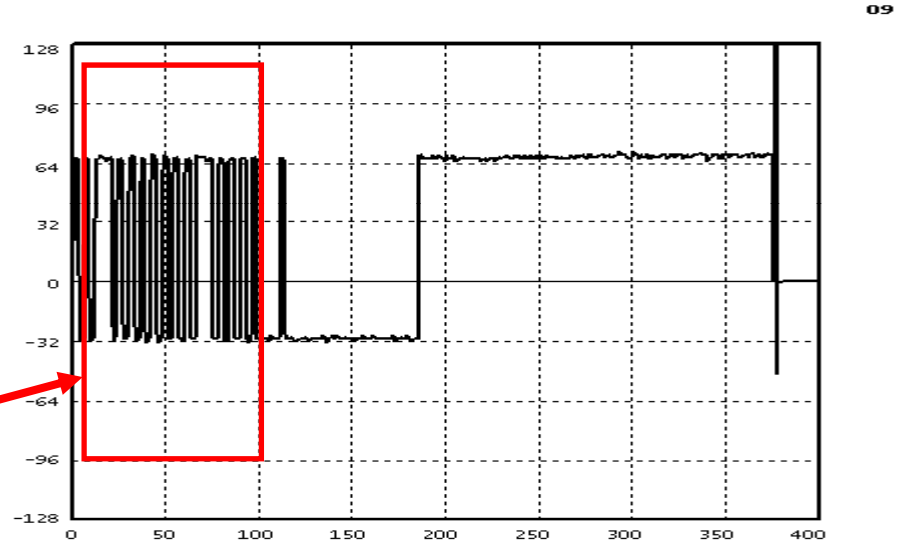
Example default configuration : “011”

- Implemented for digital interfaces (HARDOC2 and SPIROC2)

DHCAL : Data Readout

- During readout, remove “bad frame” (address pointer error when chip is not full)

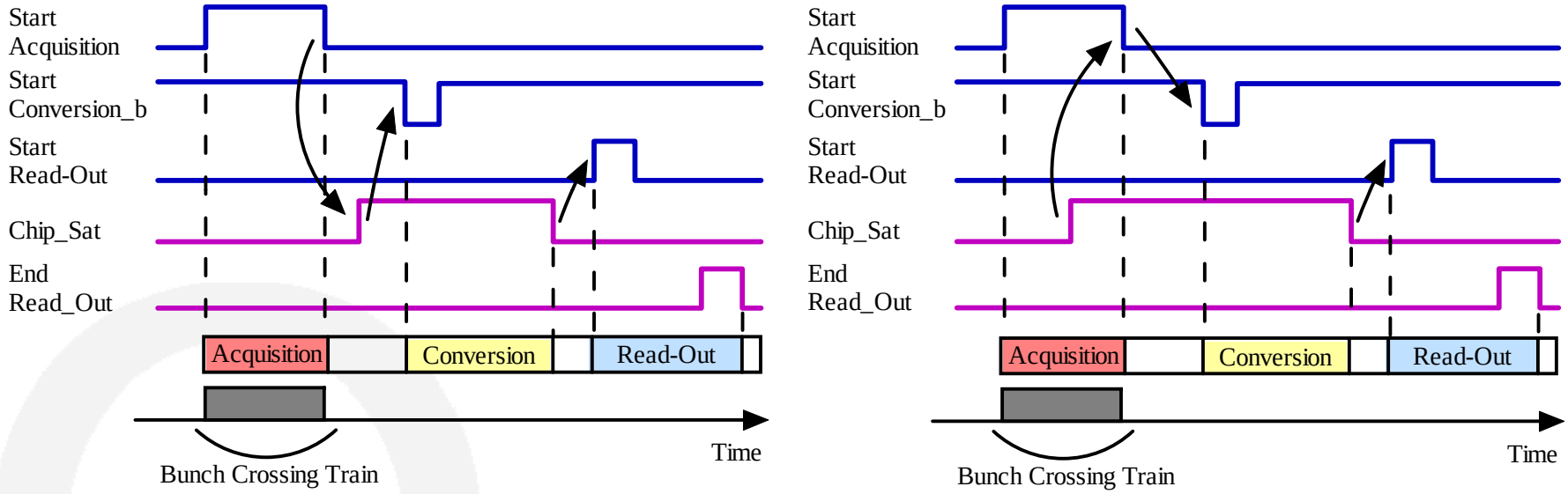
First irrelevant frame



- Capacity of 127 trigger instead of 128 ➔ change digital memory limits

SPIROC ➔ All ROC Chips : StartAcquisition

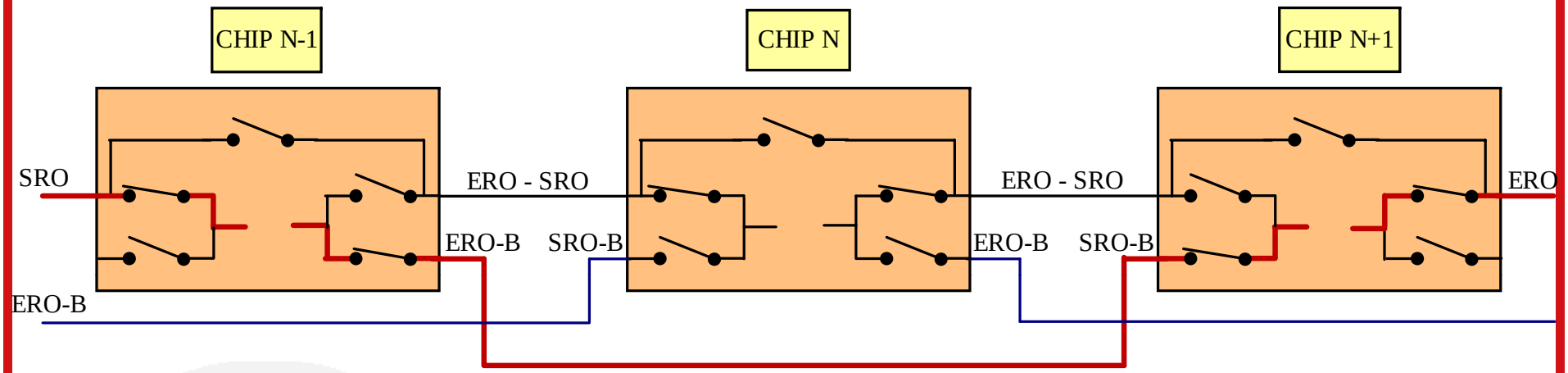
- Change for SPIROC like ➔ “StartAcquisition” active on level.



- RamFull ➔ ChipSat (uniformity between ROC chips)
- Allow to remove “RamFullExt” signal (DHCAL) and to let DAQ stop acquisition

StartReadOut and EndReadOut: bypass

- Add bypass for these 2 signals (SRO, ERO ➔ SRO-B, ERO-B).

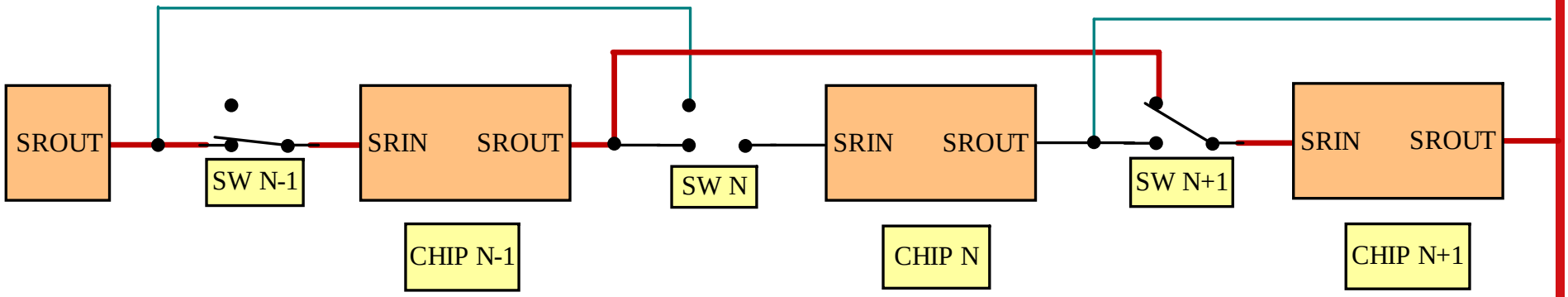


In red, StartReadOut and EndReadOut flow if chip “N” fails

- Chip N can bypass itself by SC
- Chip “N-1” and chip “N+1” can bypass chip “N” by SC
- If Chip N fails :
  - Chip N-1 sends EndReadOut signal on EndReadOutBypass
  - Chip N+1 reads StartReadOut signal on StartReadOutBypass

Slow Control: bypass

- Add bypass jumpers on PCB

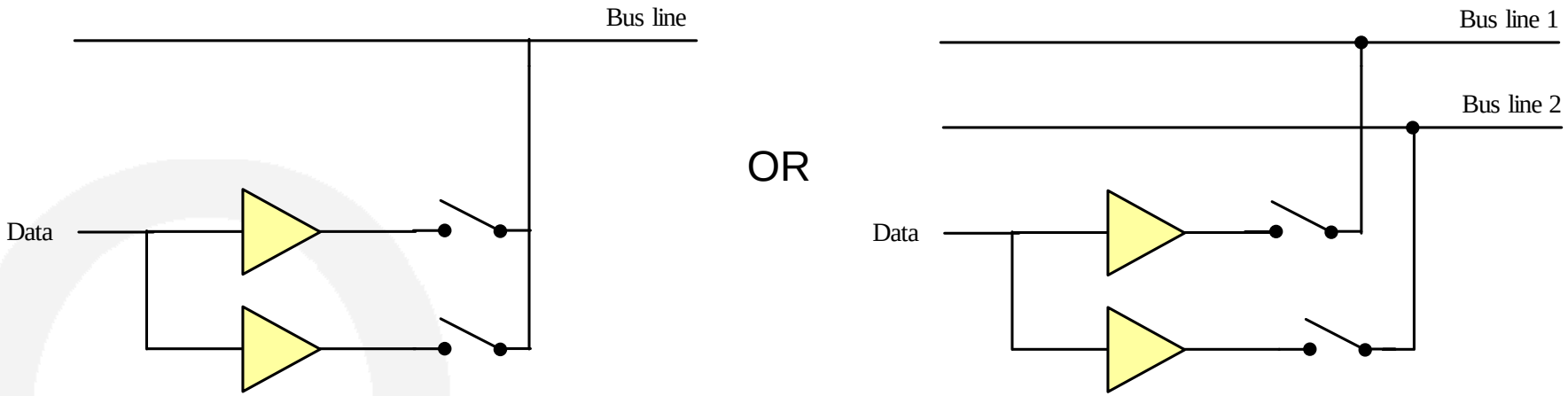


In red, SC flow if chip “N” fails

- Default position is chip “N” reads chip “N-1”
- If Chip N fails :
  - Switch N removed
  - Switch N+1 ➔ in position to read chip “N-1”

Data and TransmitOn: extra buffers

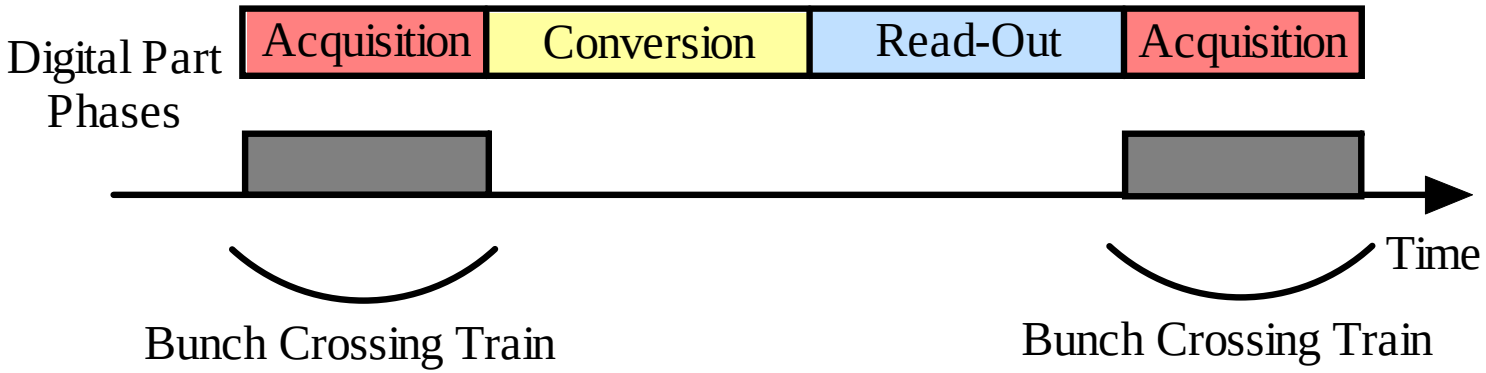
- Add 1 extra buffer on these 2 signals
- Each one is removable from bus line by SC



- Allow to remove one buffer that stick the bus line

Power On digital: Timing aspect 1/2

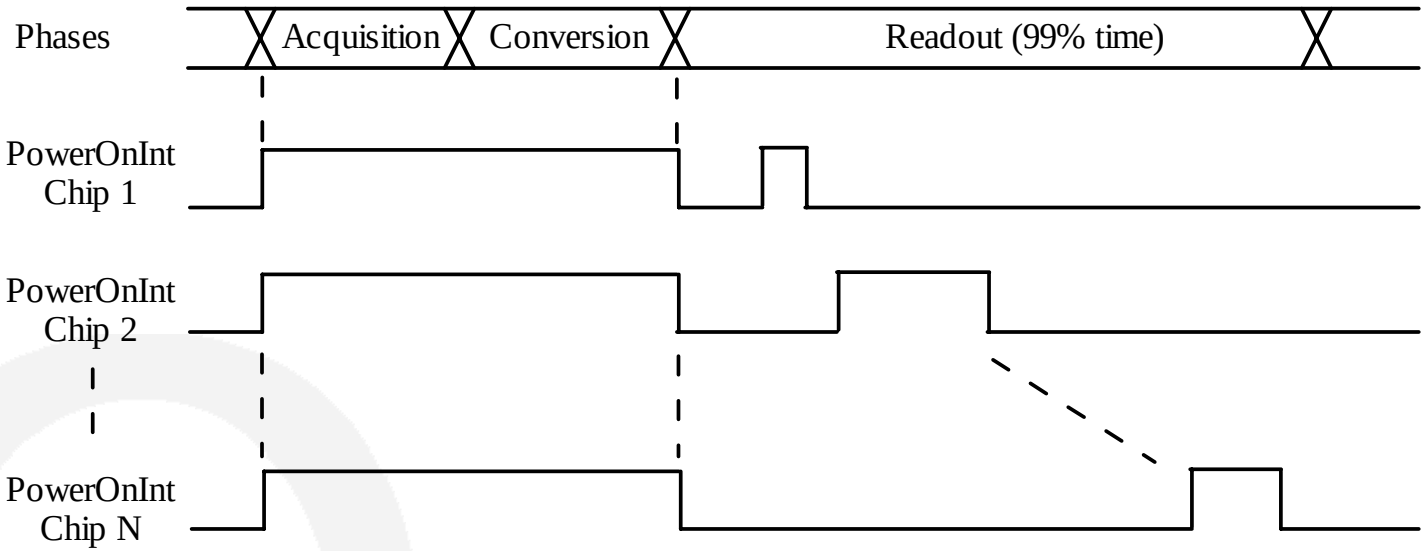
- ILC based on a 200 ms bunch crossing period



- Timing aspect of each phases:
  - Acquisition: 1 ms (common)
  - Conversion : max 103 us = 12 bits ADC @ 40 MHz (common)
  - Readout (daisy chained) @ 5 MHz:
    - max 4 ms for 1 HARDROC
    - max 3.8 ms for 1 SPIROC
    - max 0.6 ms for 1 SKIROC
- Max working time for 1 chip < 5 ms (195 ms idle)

Power On digital: Timing aspect 2/2

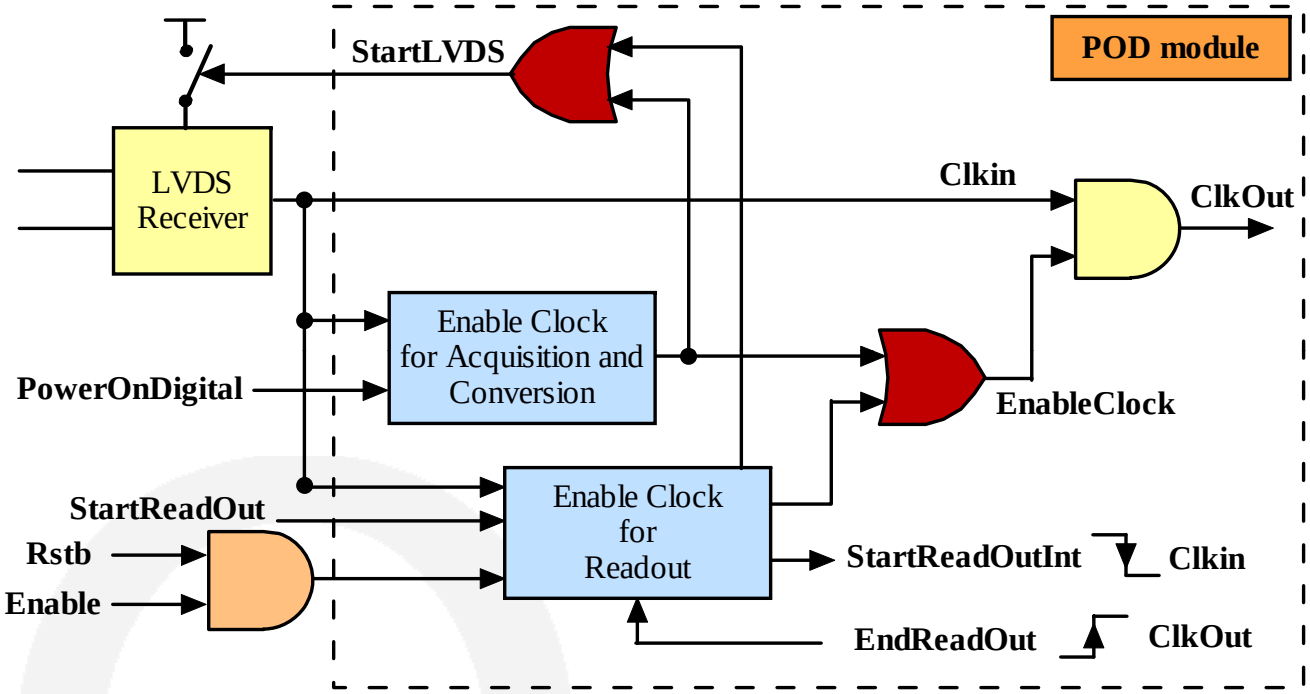
- PowerON start/stop clocks and LVDS receiver bias current to meet power budget.

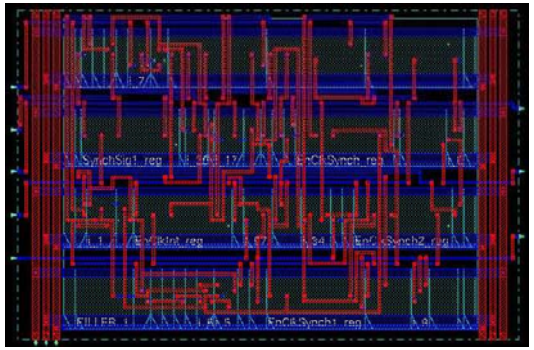


- 2 working modes :
  - Acquisition, Conversion ➔ common to all managed by DAQ
  - Readout ➔ daisy chained managed by StartReadOut and EndReadOut

Power On Digital: POD block diagram

- POD module inserted for the 2 clock LVDS receivers

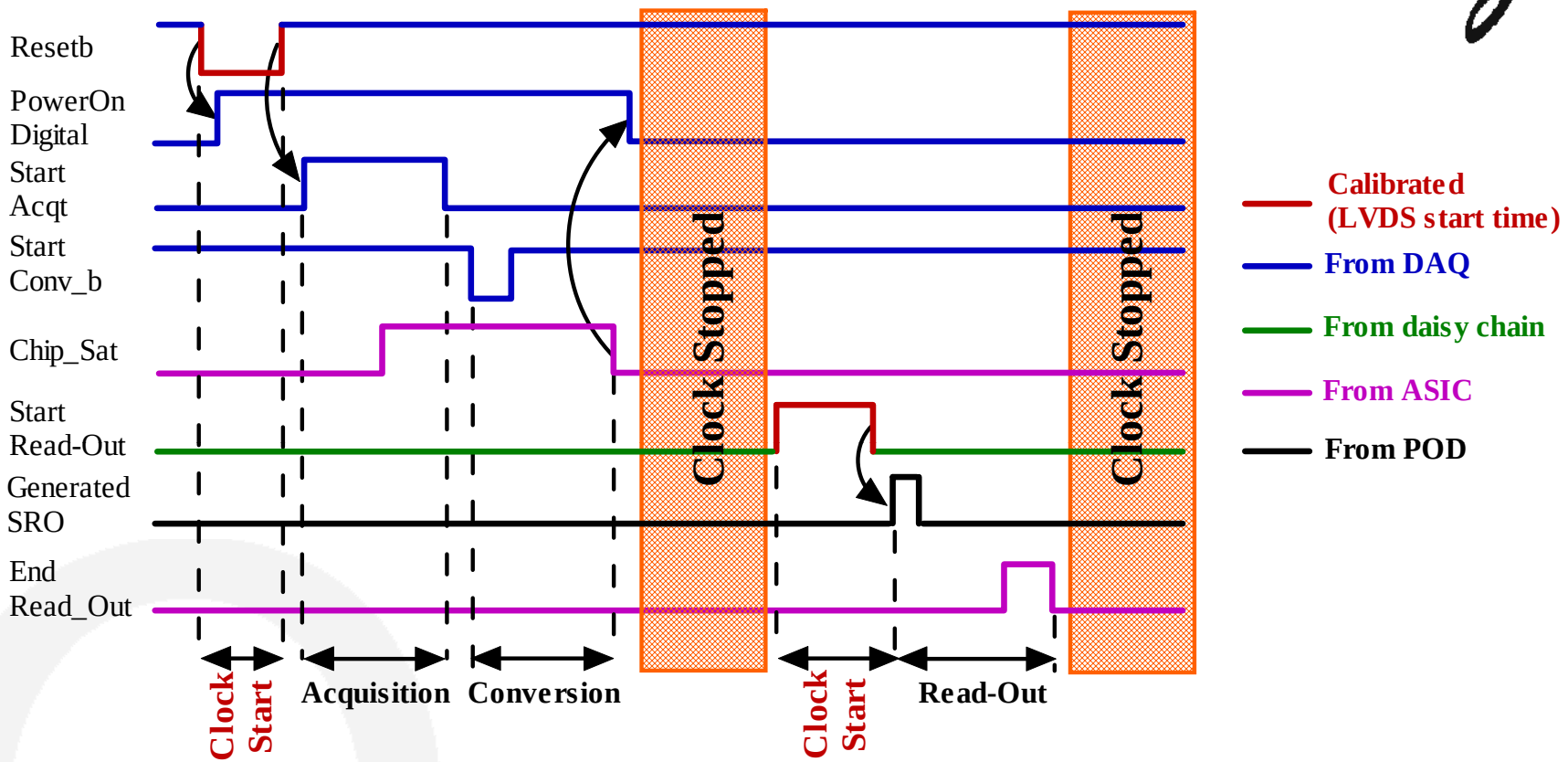




- Clock is started asynchronously, enabled and stopped synchronously (at ‘0’)

- 2 others LVDS receivers (RazChn/NoTrig and ValEvt) active during PowerOnAnalog (during bunch crossing)

Power On digital: sequence



- Some security added:
  - StartReadOut managed asynchronously ➔ low pass filter added
  - Possibility to use StartReadOut instead of the one generated by POD (like first prototype of ROC chips)
  - PowerOnDigital at '1' can force the clock

CONCLUSION

- Next run for SPIROC2 and HARDROC2 is 9 June 2008

- Many improvements already inserted for the run:
  - Shift registers improvements (multiplex, default, extra FF)
  - Bypass signals
  - Extra buffers
  - Bug correction for DHCAL

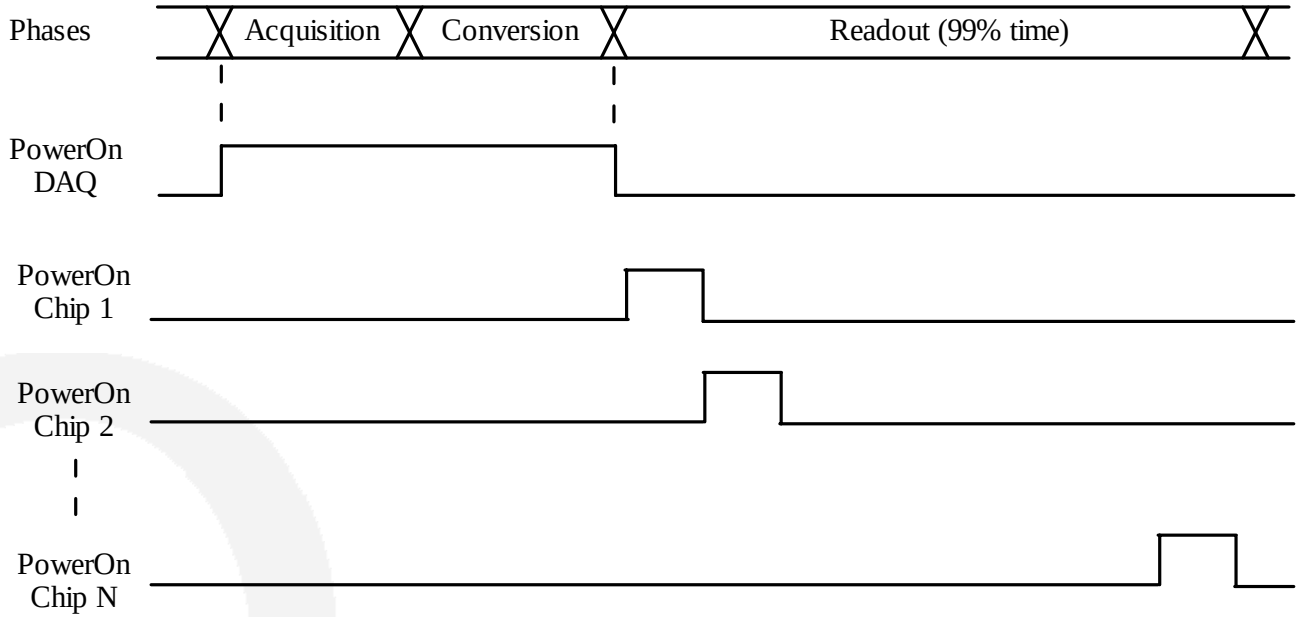
- 1 Major improvement for digital is POD module (in progress):
  - Start / Stop clocks
  - Start / Stop LVDS receivers

- POD should be implemented carefully but it is needed
  - Only way to meet power budget
  - Bypass signals have been added
  - 1 signal can overtake all the others

BACKUP SLIDES

Power On digital (very preliminary): 1/3

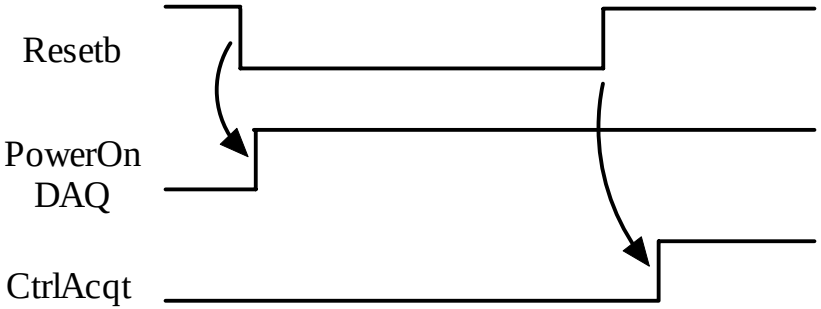
- PowerON must start/stop clocks and LVDS receiver to meet power budget.



- 2 working modes :
  - Acquisition, Conversion (common to all) ➔ managed by DAQ
  - Readout ➔ managed internally
- Internal PowerON ➔ OR of “PowerOnDAQ” and “PowerOnChip”

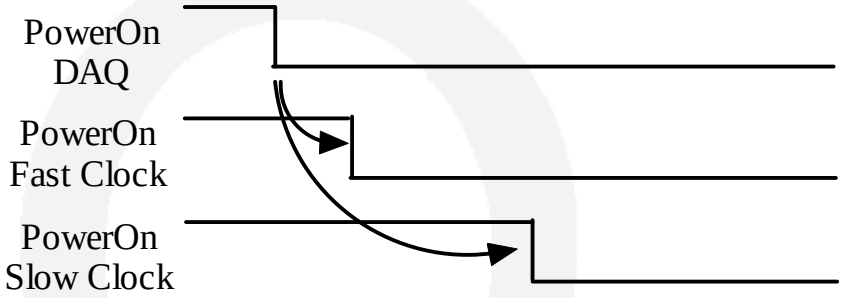
Power On digital from DAQ : 2/3

- PowerON set during a reset phase before each acquisition



  - Completely managed by DAQ
  - Reset pulse > LVDS start time

- PowerON release at the end of conversion

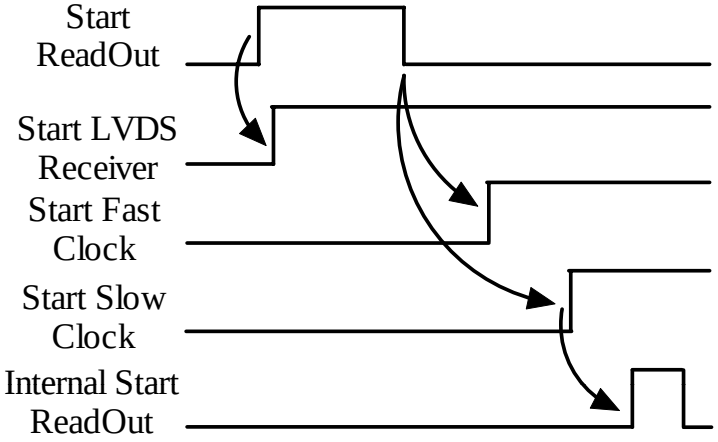


  - Synchronized internally to properly stop clocks
  - Effective PowerOn release ➔ after max 2 ticks of Slow Clock

- PowerON DAQ is asynchronously set and synchronously release (internally in each chips)

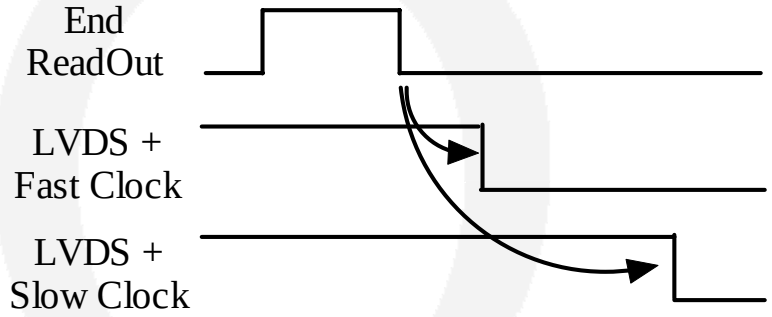
Power On digital for Readout : 3/3

- PowerON of Chip N set by chip “N-1”



  - Internally managed by ASIC
  - StartReadOut pulse > LVDS start time
  - Synchronous clocks start
  - Internal StartReadOut starts state machine

- PowerON release at the end of Readout of chip N



  - Synchronized internally to properly stop clocks
  - Effective PowerOn release ➔ after max 2 ticks of Slow Clock
  - PowerON stops LVDS and clock at the same time synchronously

- PowerON split into 2x“StartLVDS” and 2 x“StartClock”