Laboratoire d'Annecy-le-Vieux de Physique des Particules

Calorimeter for ILC

# Status of the DHCAL DIF

## Detector InterFace Board

Sébastien Cap, Guillaume Vouters,
Julie Prast



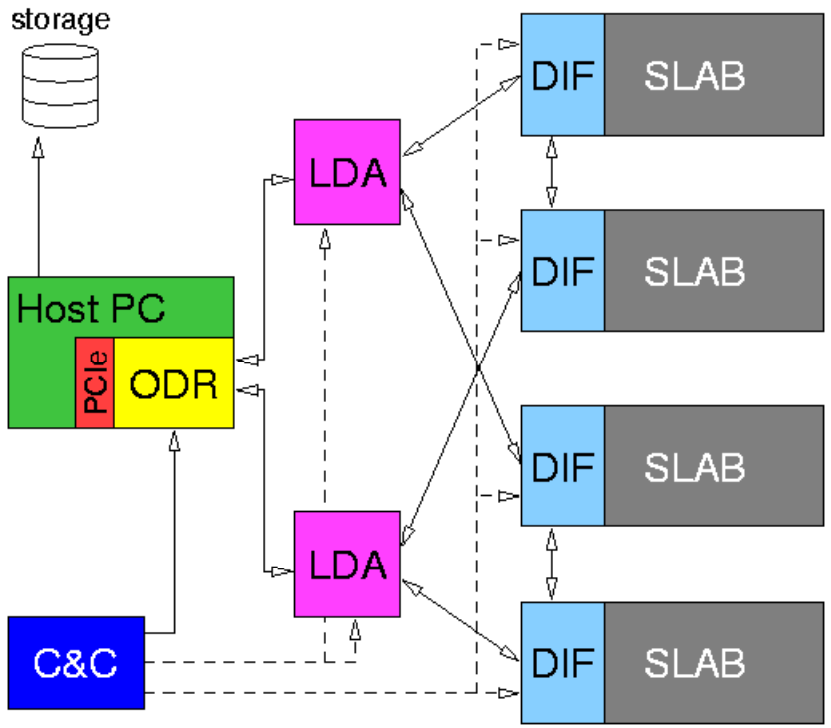
CENTRE NATIONAL DE LA RECHERCHE SCIENTIFIQUE

IN2P3 Institut National de Physique Nucléaire et de Physique des Particules

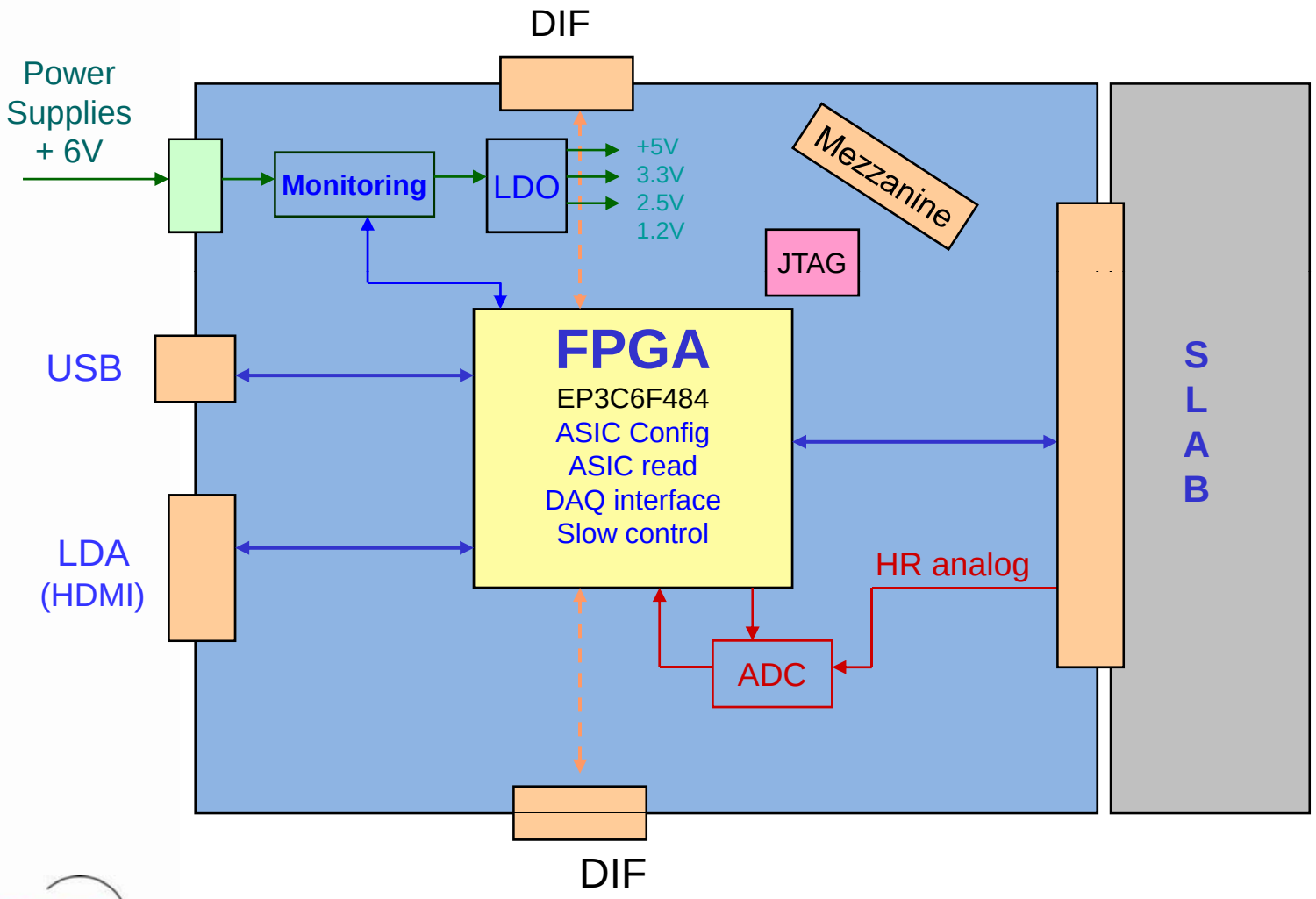
UNIVERSITE CHAMBERY ANNECY SAVOIE

# Aims of the DHCAL DIF

- Interface DHCAL ASUs with the DAQ
  - Configure the VFE chips
  - Perform digital readout
  - Power cycling, …
  - LDA interface (final DAQ)
  - PC interface through USB for debug and standalone.
- Others :
  - Micromegas and RPC
  - Asics : Hardrocs or Lyon's chip



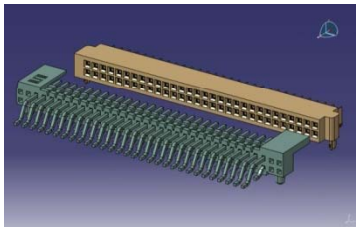
# Architecture of the DIF Board

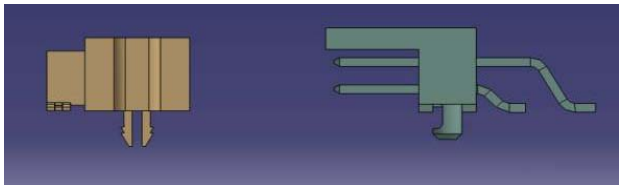


# SLAB Interface compliant with the DIF task force

| | | | |
|---|---|---|---|
| GND | 1 | 2 | GND |
| MUX3_CSn | 3 | 4 | Analog_0 |
| MUX2_CSn | 5 | 6 | GND |
| MUX1_CSn | 7 | 8 | Analog_1 |
| spare1 | 9 | 10 | GND |
| MUX_ENN | 11 | 12 | C_test |
| MUX_WRN | 13 | 14 | GND |
| spare2 | 15 | 16 | MUX_A4 |
| en_otaq | 17 | 18 | MUX_A3 |
| GND | 19 | 20 | MUX_A2 |
| SR_reset | 21 | 22 | MUX_A1 |
| hold | 23 | 24 | MUX_A0 |
| spare3 | 25 | 26 | Ramfullext |
| SR_IN | 27 | 28 | Reset_BCID |
| spare4 | 29 | 30 | GND |
| SR_OUT | 31 | 32 | Resetn |
| spare5 | 33 | 34 | Start_Conv_daqb |
| SR_clk | 35 | 36 | End_Readout |
| GND | 37 | 38 | Start_acq |
| TransmitOn_3 | 39 | 40 | RamFull |
| Pwr_analog | 41 | 42 | Dout_3 |
| TransmitOn_2 | 43 | 44 | GND |
| Pwr_dac | 45 | 46 | Dout_2 |
| Pwr_ss/Pwr_sca | 47 | 48 | Start_Readout |
| GND | 49 | 50 | Trig_ext |
| TransmitOn_1 | 51 | 52 | Start_Readout_Bypass |
| Pwr_digital | 53 | 54 | Dout_1 |
| TransmitOn_0 | 55 | 56 | GND |
| Pwr_adc | 57 | 58 | Dout_0 |
| SC_SROUT | 59 | 60 | SC_SRIN_BYPASS |
| SC_SROUT_BYPASS | 61 | 62 | SC_SRIN |
| SC_select | 63 | 64 | SC_reset |
| SC_clk | 65 | 66 | SC_load |
| User_LVDS_P | 67 | 68 | User_LVDS_N |
| Trig_Ext_P | 69 | 70 | Trig_Ext_N |
| DVDD | 71 | 72 | AVDD |
| Clk_5MHz_0_P | 73 | 74 | Clk_5MHz_0_N |
| Clk_5MHz_1_P | 75 | 76 | Clk_5MHz_1_N |
| GND | 77 | 78 | GND |
| Clk_40MHz_0_P | 79 | 80 | Clk_40MHz_0_N |
| Clk_40MHz_1_P | 81 | 82 | Clk_40MHz_1_N |
| DVDD | 83 | 84 | AVDD |
| Raz_Chn_P | 85 | 86 | Raz_Chn_N |
| Val_Evt_P | 87 | 88 | Val_Evt_N |
| AVDD | 89 | 90 | AVDD |

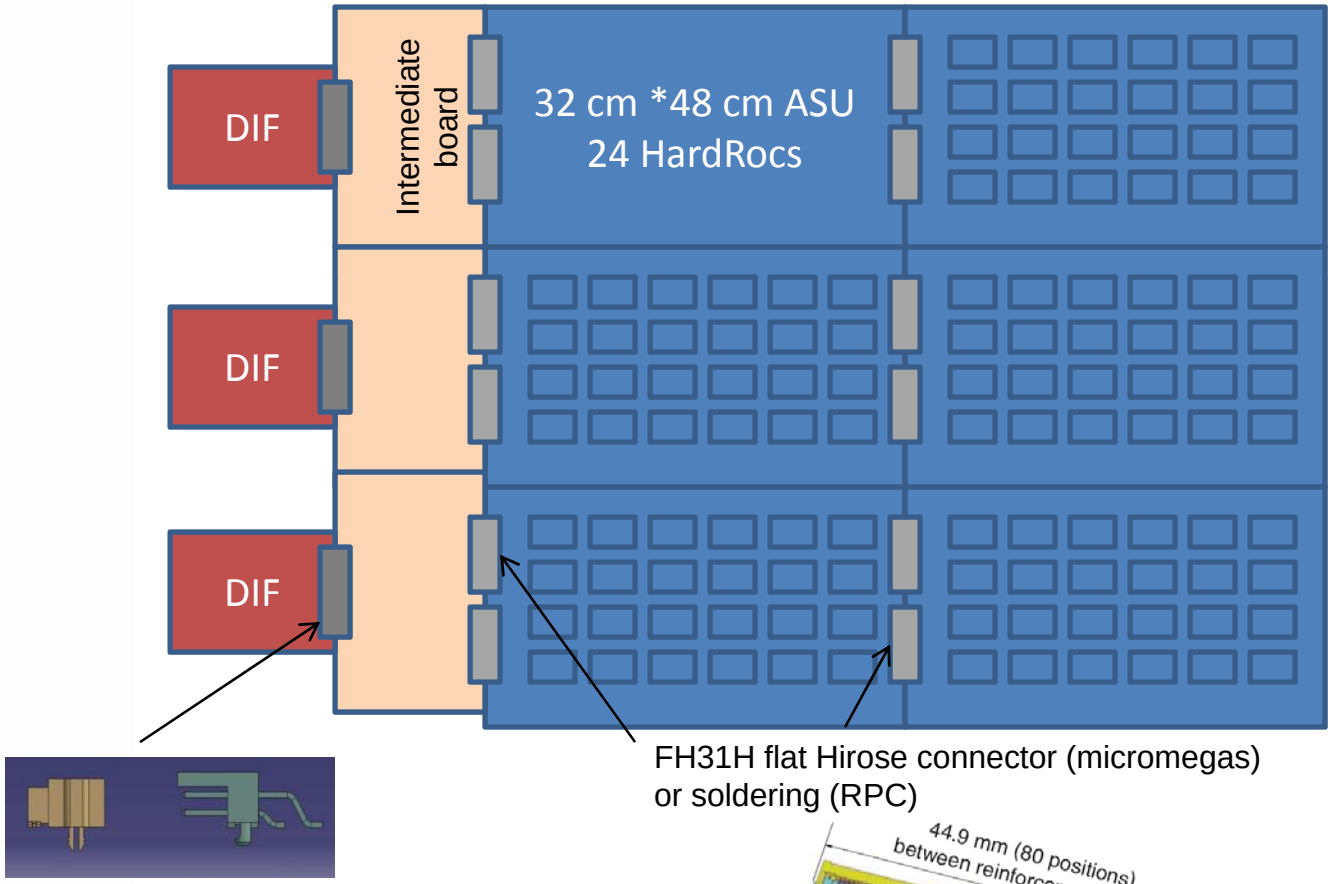
=> The DHCAL DIF can also be used for ECAL or AHCAL …



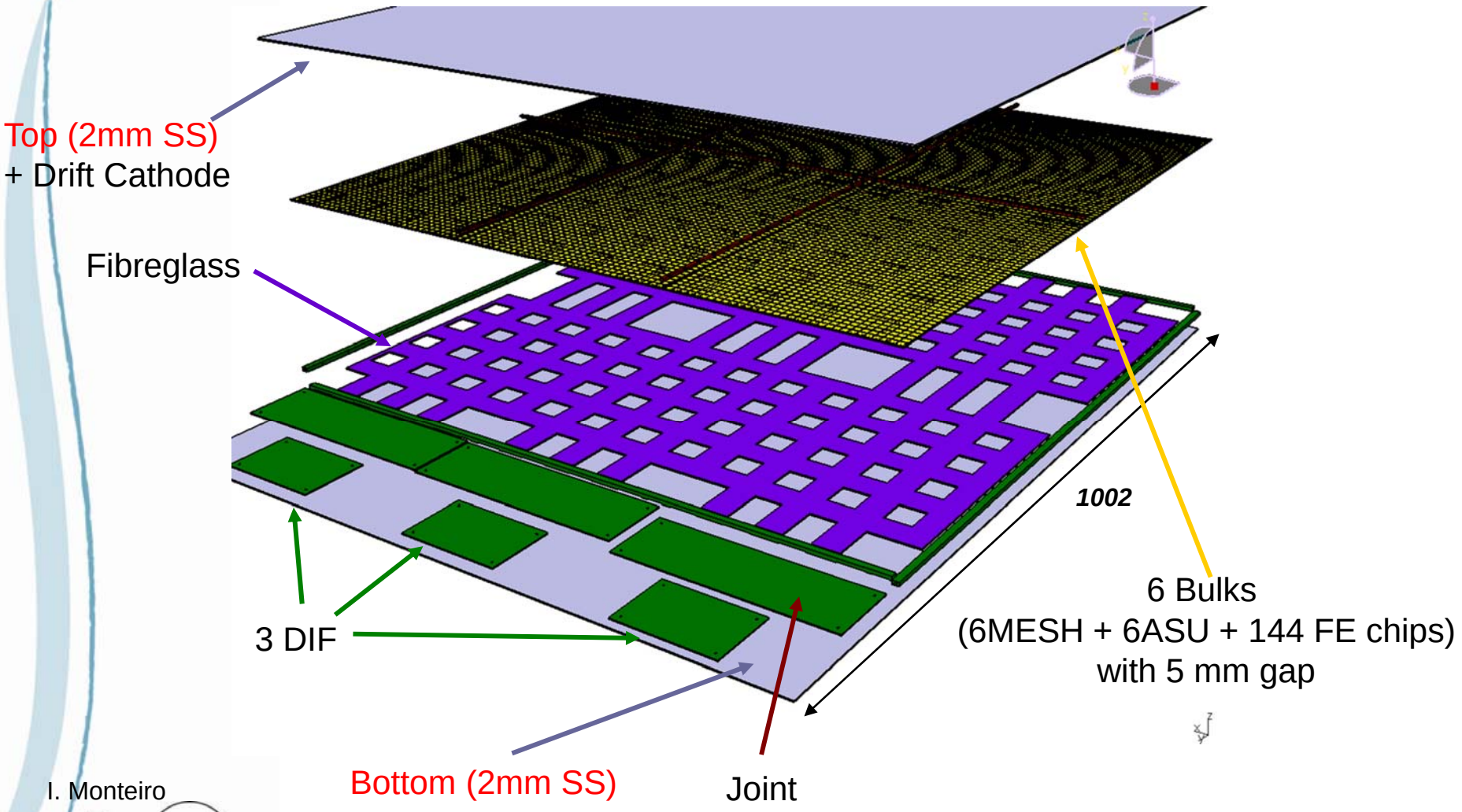


Samtec FSH/ SFMH 90 pin connector

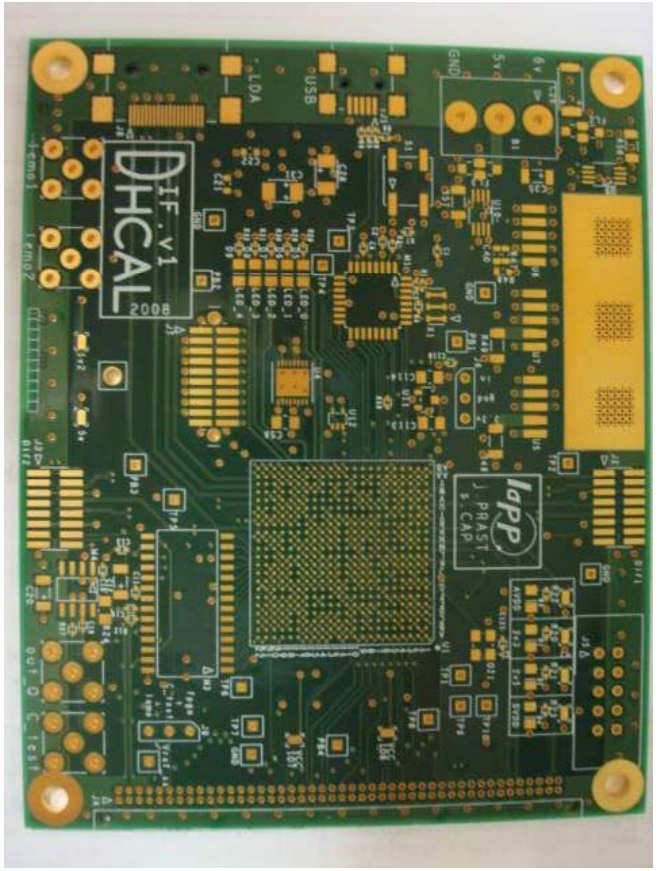
# The DHCAL M2 Architecture



# Design of a 1m$^2$ MicroMegas

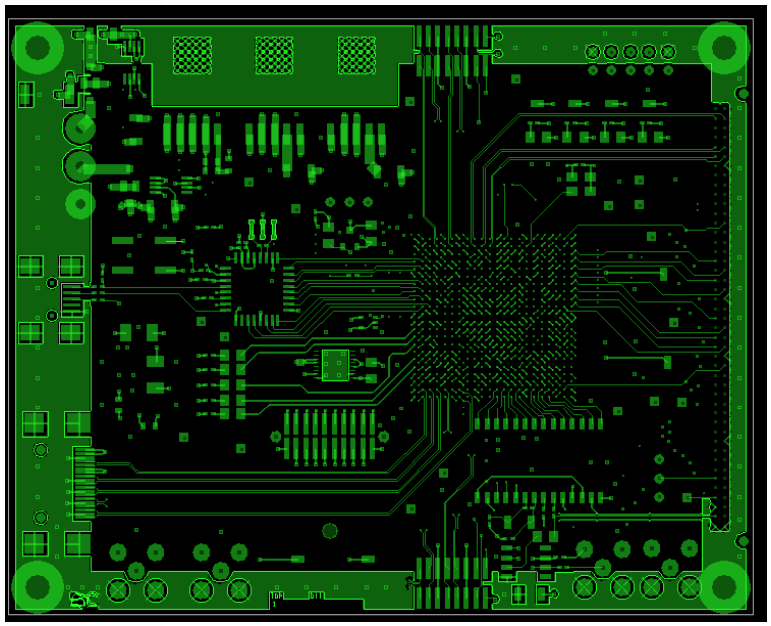


# Status of the DHCAL prototype




- Sent to production on April 29 th.
- 10 PCB are manufactured.
- Cabling in progress.
- Boards awaited next week.

# Mechanical and Electrical Characteristics



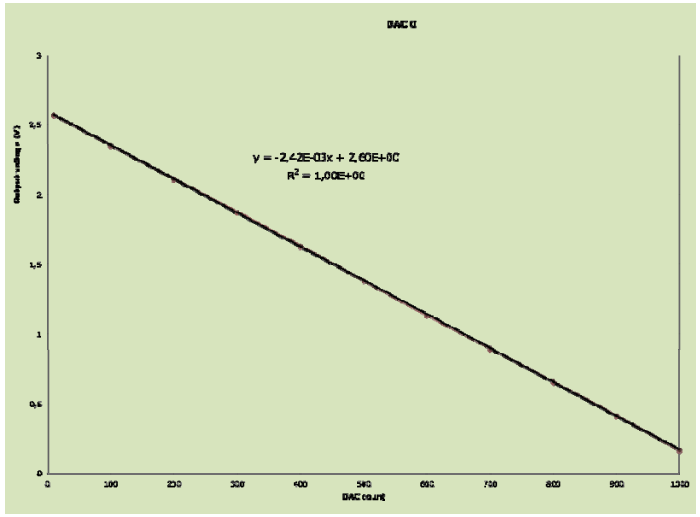
DIF Top View

- 8 cm *10 cm *1.5 mm
- 10 layers
  - 4 signal layers
  - Controlled impedance
  - Classe 6 (0.12 mm wire)

Many thanks to Sébastien Cap for the CAD.

# Firmware Status

- USB interface OK
  - R/W registers, commands, …
- Slow control OK
  - HardRoc configuration
  - Return signal (SC_q) check
- Acquisition and Digital Readout : to be tested (TBT)
- Analog readout: TBT
- Monitoring TBT
- LDA interface : to be dvlped

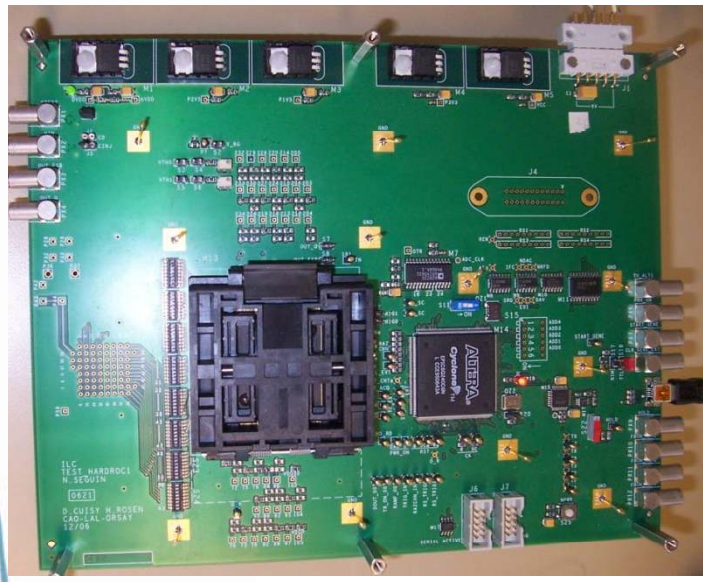


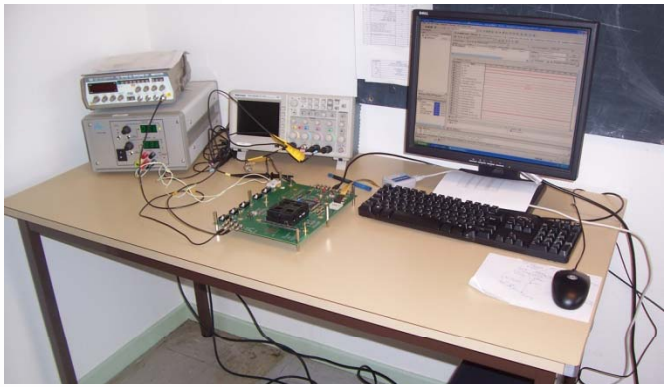

DAC output (V)= f (SC DAC value)

• Software is developed by Christophe Combaret (IPN Lyon). *See his talk*

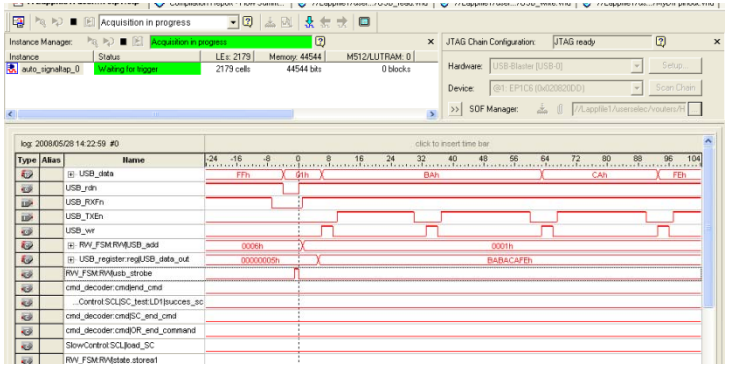
•*Congratulations to Guillaume Vouters for the main VHDL part.*

# FW validation on the HR test board





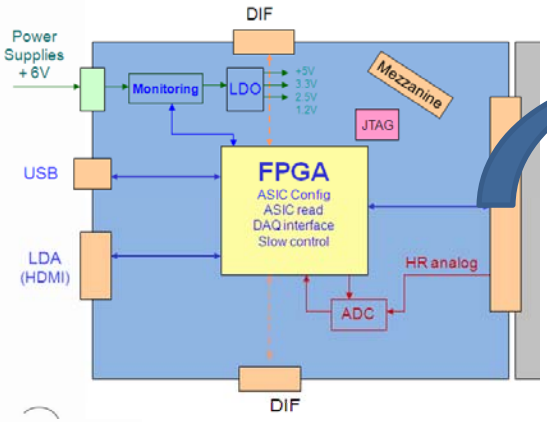
- LAL HardRoc test board
  - 1 HR + Cyclone FPGA.
  - 12 bits ADC for the analog RO.
  - Possibility of charge injection.
  - USB interface.
- FW debug with signal tap

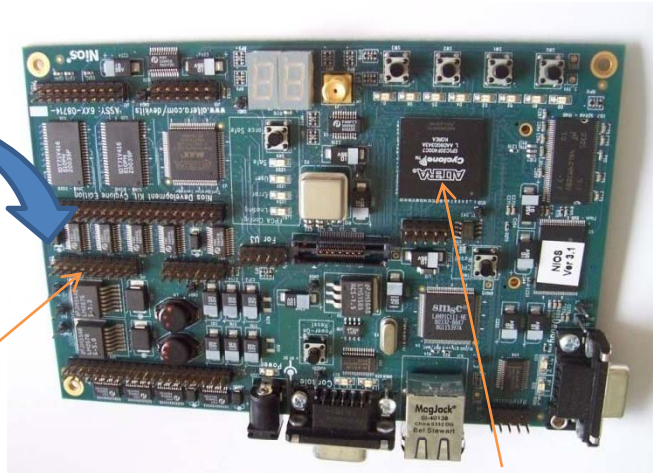


# Validation of the DHCAL DIF

- No ASU available with HR before …. ?
- Emulation of HardRocs using an Altera evaluation kit.
  - Fit the HR VHDL (digital part) in the FPGA.
  - User defined IO connector to interface with the DIF.

=> Will allow validation of the DIF and FW for N HR



User defined connector

FPGA to emulate HardRocs

# Conclusion

- DHCAL DIF will be back from production next week.
- Firmware and corresponding software (Lyon) are in progress.
  - Debug on the HardRoc test board (1 HR).
- Before ASU reception, the DIF will be tested using an Altera evaluation kit to emulate HardRocs.

=> Necessity to have a validated and reliable DIF for the November test beam.