LDA Status

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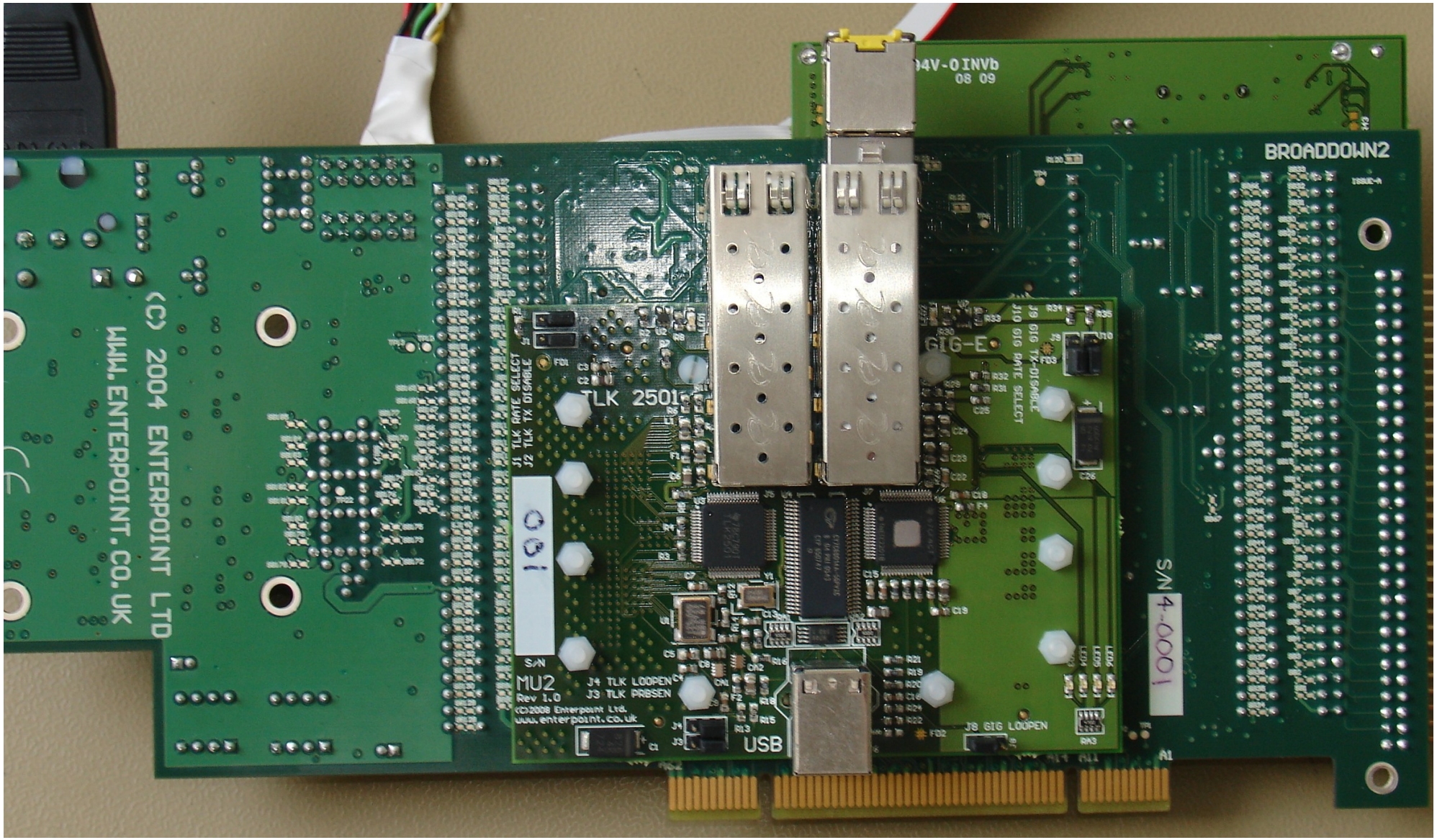
Current Hardware

- The external company (Enterpoint Ltd.) have delivered a HDMI interface board and a Gigabit Interface board.
- The remaining 4 Gigabit boards and 9 HDMI boards are in assembly and should be with us soon.
- Interface connectors need to be purchased, but we have obtained 1 set as a free sample from SAMTEC.
- 1 full LDA prototype now exists at Manchester.

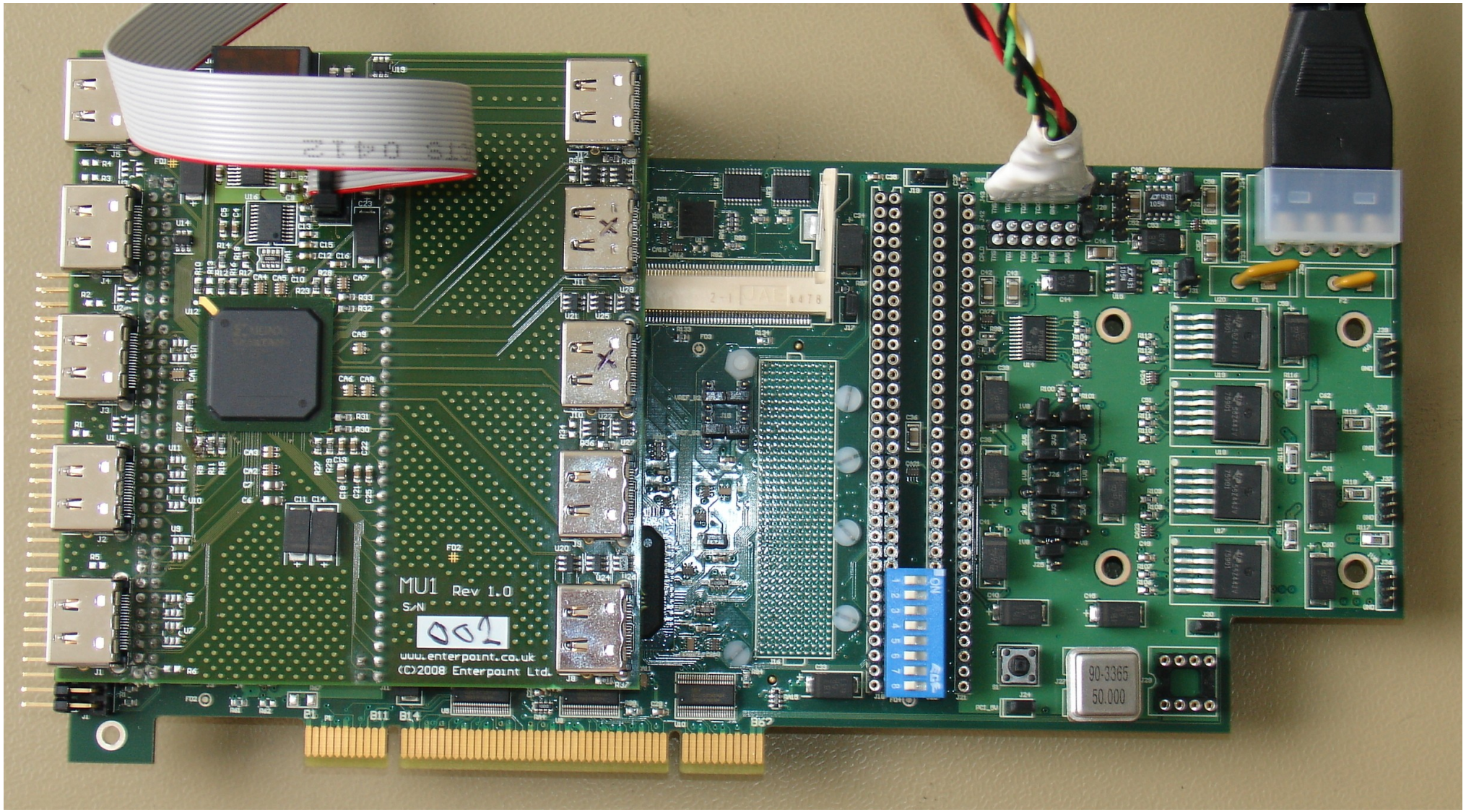
Gigabit Interface Board



Gigabit Interface Board

- Have obtained the Gigabit Embedded MAC IP from Xilinx as a free donation to the project, so work is proceeding in bring the Ethernet interface online.
- TLK interface is not being worked on currently.
- USB interface is semi-problematic as the Interface board shares some IO with the HDMI board, and so will need some thinking about. It also requires some programming of the Embedded CPU on the chip (CY7C68014A).

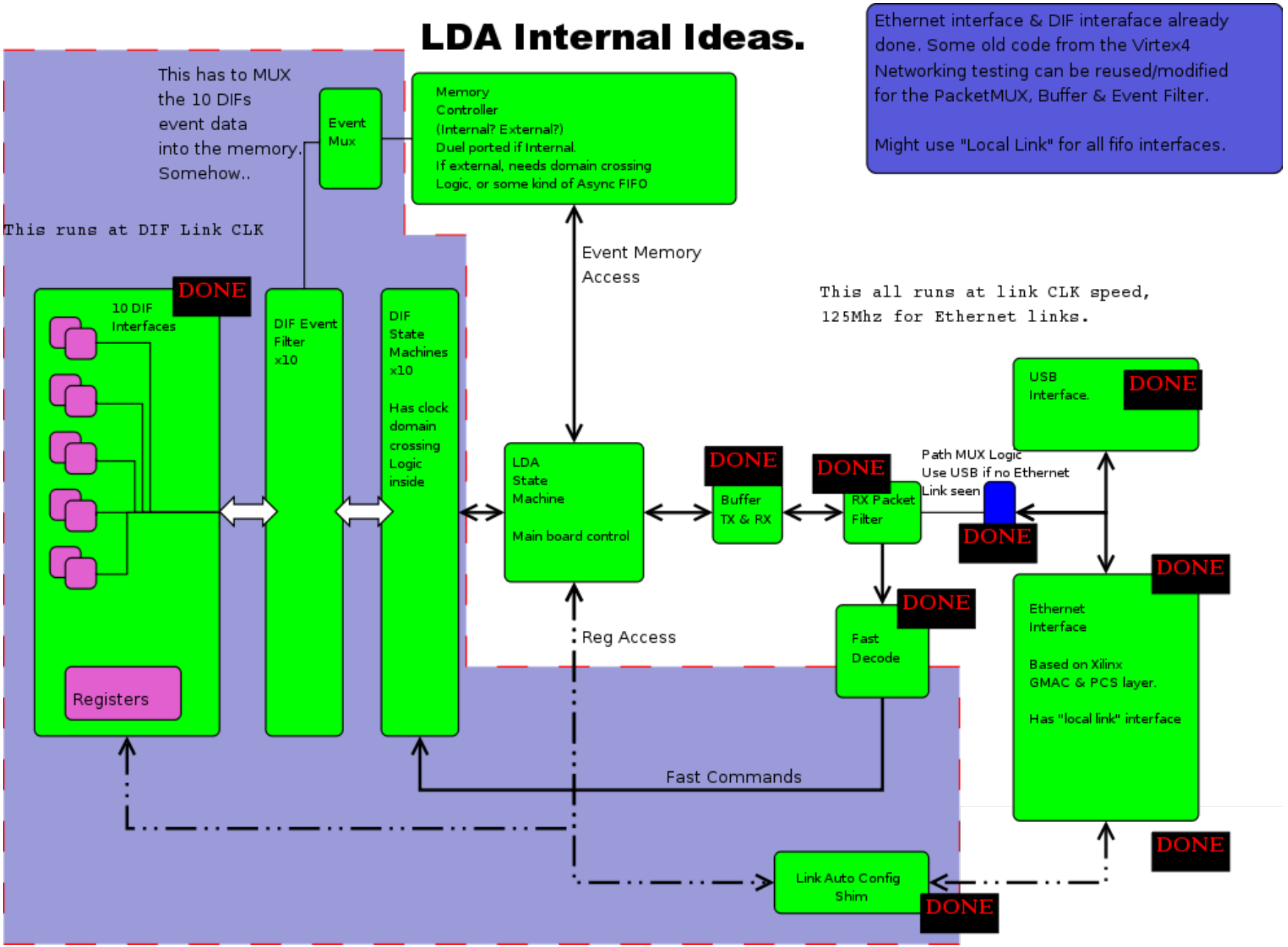
HDMI Interface Board



HDMI Interface Board

- **!!! Misunderstanding with Enterpoint means that current prototypes have DC coupled HDMI IO, not AC coupled !!!**
- Despite having 10 Connectors, only 8 of the links are fully wired. Requires the FPGA to be upgraded to S31000 to get the other 2 working. Costing is guessed as being just the difference between S3400 and S31000 price.
- Has shared IO with some of the Gigabit Interface boards, mostly the USB & LED IO.
- Re-mapping the firmware in the FPGA can help to alleviate some of this. Although we are very tight on pins.

Firmware Overview



Firmware Overview

- Work on the basic firmware framework is proceeding. Items marked “DONE” in the previous diagram exist and are being tested.
- LDA SERDES and the corresponding DIF SERDES have been tested on a simple development board.
- Ethernet Interface is the current priority.
- Firmware is envisioned to be in 2 clock domains, the 125Mhz domain of the Ethernet, and the (..)Mhz domain of the DIF links.
- Docs are slowly appearing on `http://www.hep.manchester.ac.uk/~mpkelly/calice/lda`

Plans I

- Current design uses ~40-50% of FPGA resources.
- Large number of Block rams are un-used, so might be able to use them as Internal DAQ buffers.
- A possible idea is to use the SO-DIMM socket to mount a little PCB with external RAM on. We have a very efficient ***ZBT*** memory controller from another project, plus the chips, so that is an attractive idea.
- Cannot use DDR2 memory, IO issues prevent it.

Plans II

- After going thought all the schematics is seems that all the IO on the SO-DIMM is available along with all the IO on the PCI socket.
- RHS DIL headers on Broaddown2 are NOT available as they share IO with the Ethernet Interface. Useful for debugging however.
- Need some way of assigning each LDA a unique ID at power up (NO free IO for a switch). Possible ideas are to code some into the CPLD's on the board, or HDMI FPGA and have that loaded over to the main FPGA. If we have SODIMM ZBT board, might place DIP switches on that.

Conclusion

- Things are proceeding well.
- Manpower is an issue, we have no time to work on everything at the same time.
- LDA state machine, DIF state machines, DIF Event receive and LDA Event processing are the main blocks still to do. Mostly based on existing blocks from this and other projects.
- USB and TLK interfaces are secondary tasks as far as Manchester is concerned. Although we do have ideas how to implement them.
- Will discuss more on this in the Meeting tomorrow.