# Toward a DAQ for the DHCAL $m^3$ (in Test Beams)

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***EUDET/Elec meeting***
***LAL, Orsay***
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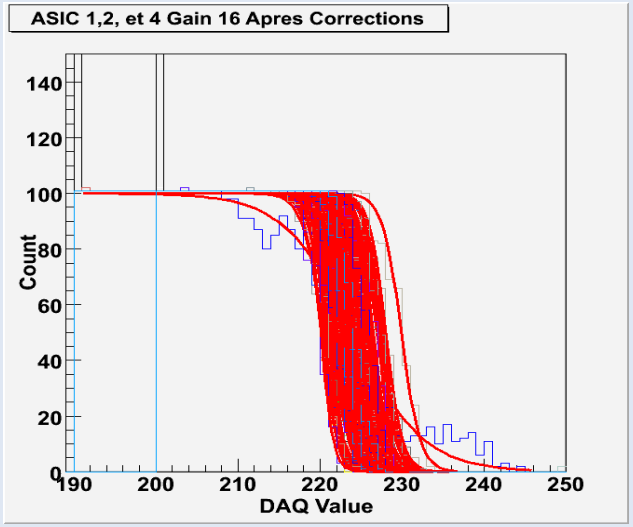
# Time line

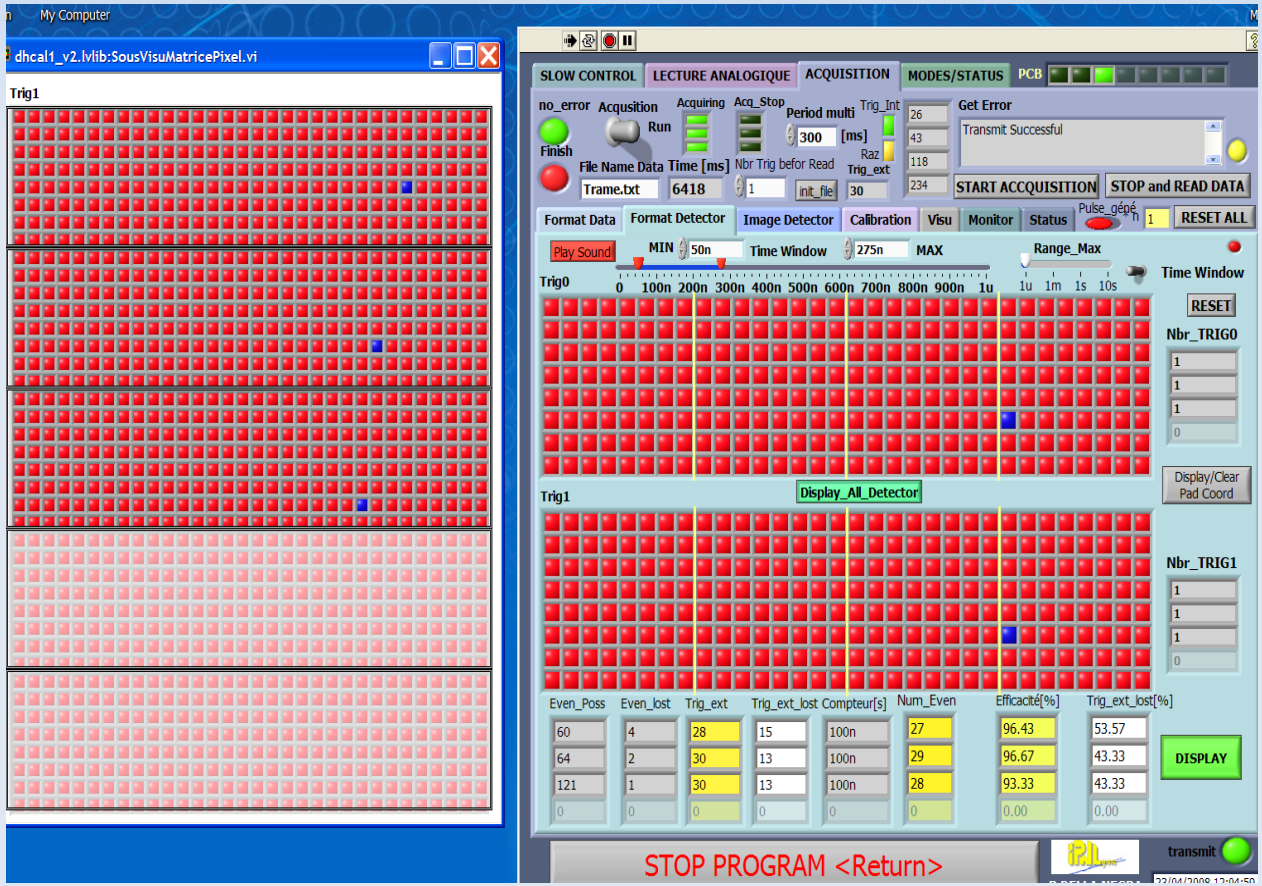
- *Cosmic DAQ*
  - *Running (new: analogue readout)*
- *Summer Test beam DAQ:*
  - *PS: July 10-17→ adapted cosmic DAQ ?*
  - *SPS: Aug. 6-11 → Adapted CALICE DAQ0*
  - *PS: beg. Nov → USB DAQ (m²)*
- *DAQ2 m³*
  - *summer 2009*

# Cosmic DAQ

- Based on LabView (R. Della Negra)
  - USB readout & control of ≤5 cards (on HUB)
    Using libDHCAL (C. Jauffret)
  - Analogue RO of 1 card (Being tested)

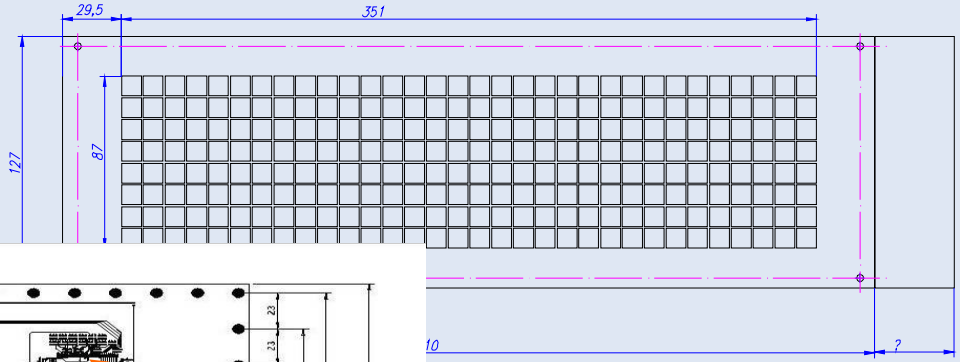
**Goal**:
- Characterise the Chamber, ASIC's, PCB's on cosmics
- Calibrate the ASIC's (EC)

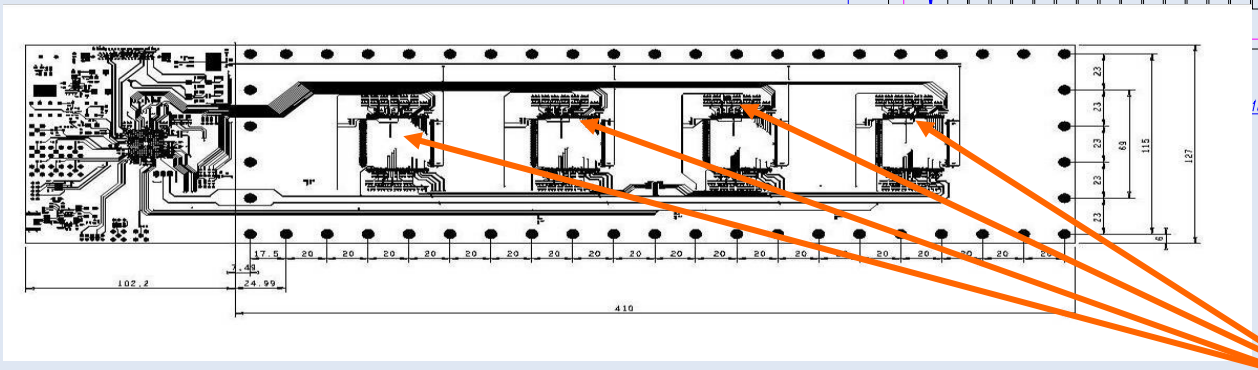


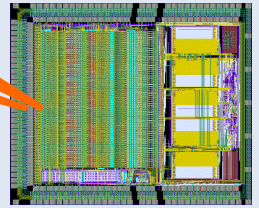



# DHCAL1 board

- 8×32 pads detector (GRPC and µMEGAS)
  - 8-layer PCB
  - 4 HARDROC's (64 ch each)
- integrated DIF
  - Code being re-used for the DHCAL DIF's
- USB connector
  - libDHCAL developed
    → C driver, LabView interface

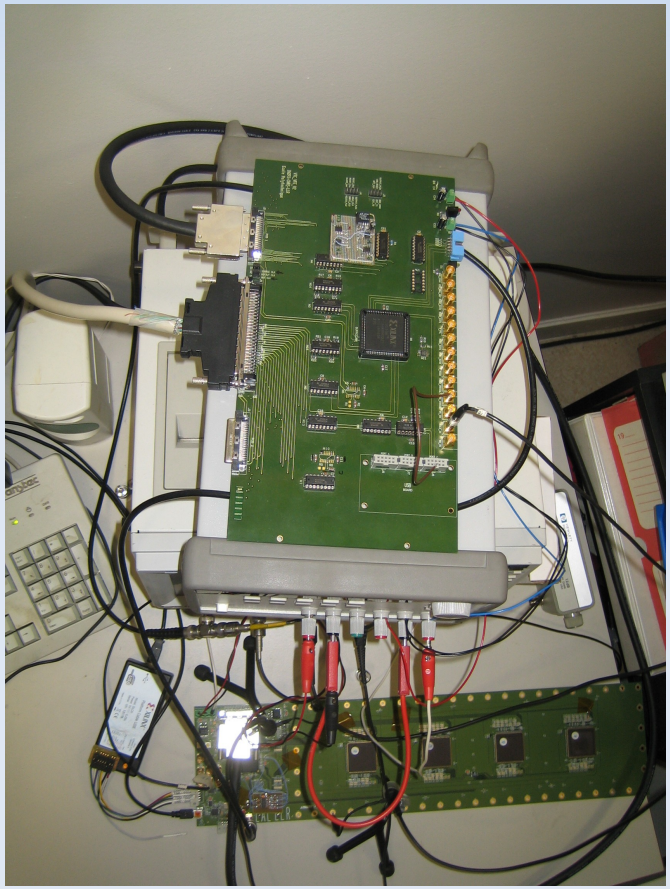


# Analogue Readout Extension:

- Goal: measure the shape of the signals
  - → optimisation of gains
- Use of the VTC card of the **ECAL cosmic bench**
  - VTC = LLR DAQ for ECAL Cosmic bench
    - HW: Boards + cables
    - Readout 1 card
      - Eventuality 2 (with adapted cables)
- Adaptation:
  - CPLD: Number of channels (↘4) ,
    Number of cycles (↗64)
  - HW: LVDS signals DHCAL ≠ ECAL
  - HW: New analogue drivers (AD8138)



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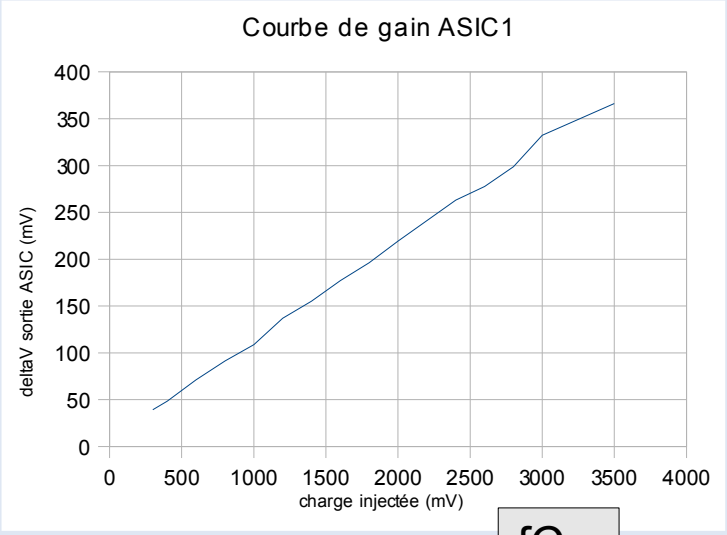
# Cosmic DAQ: Analogue RO perf

- First evaluation
  - Linarity,
- Ex: Analog output of first ASIC1
  - dominated by coherent noise
- OK for RPC response

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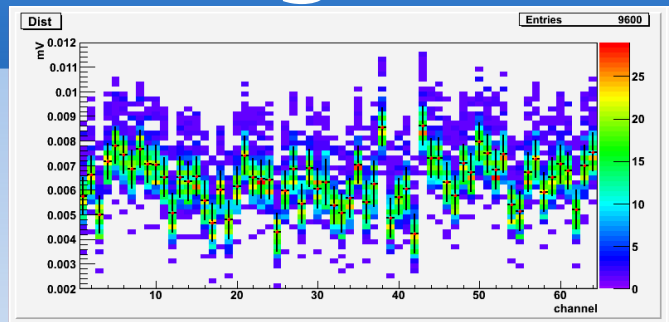
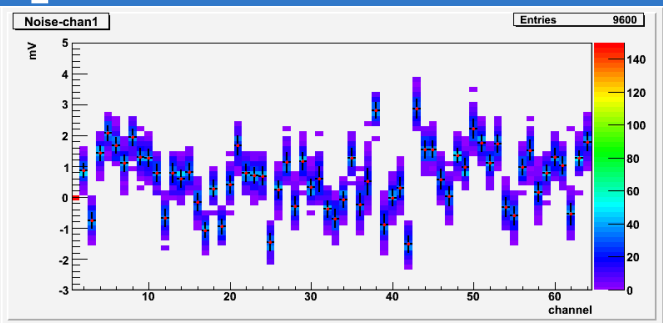
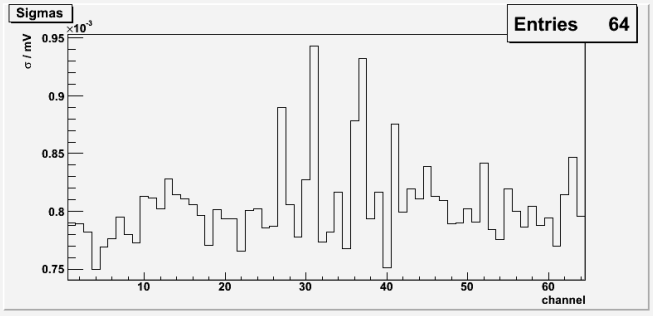
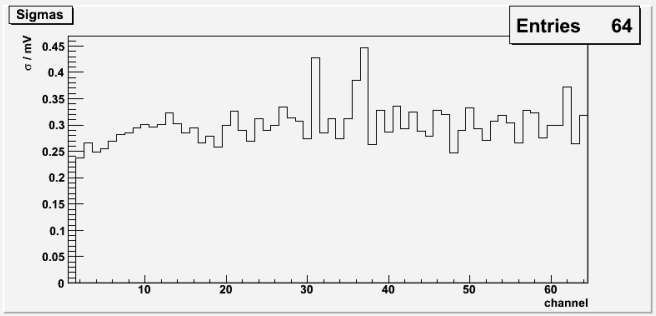
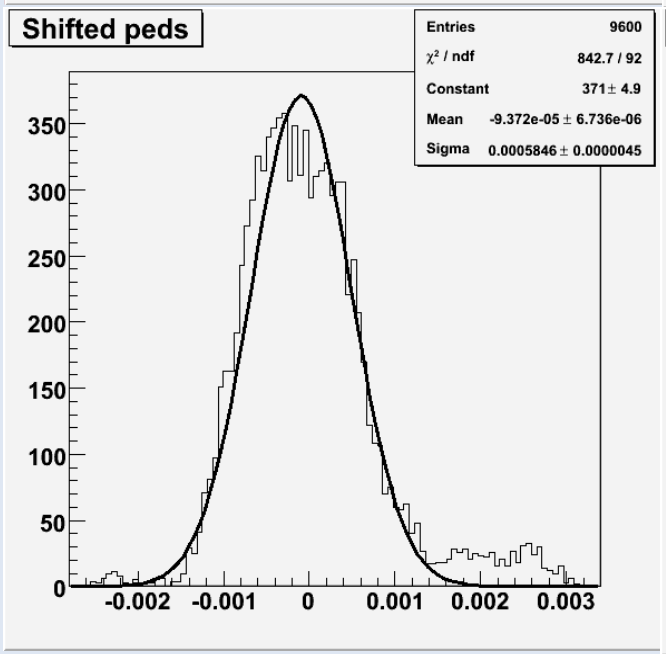
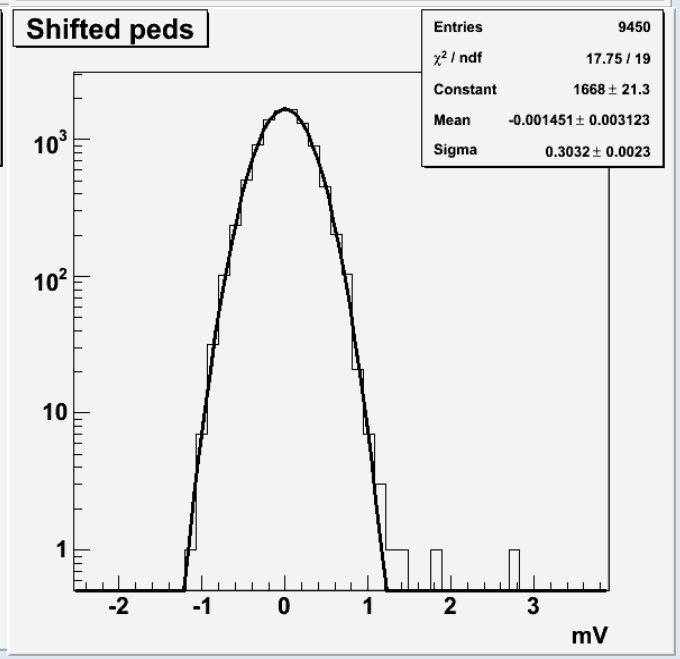


# Test beam DAQ in Aug.

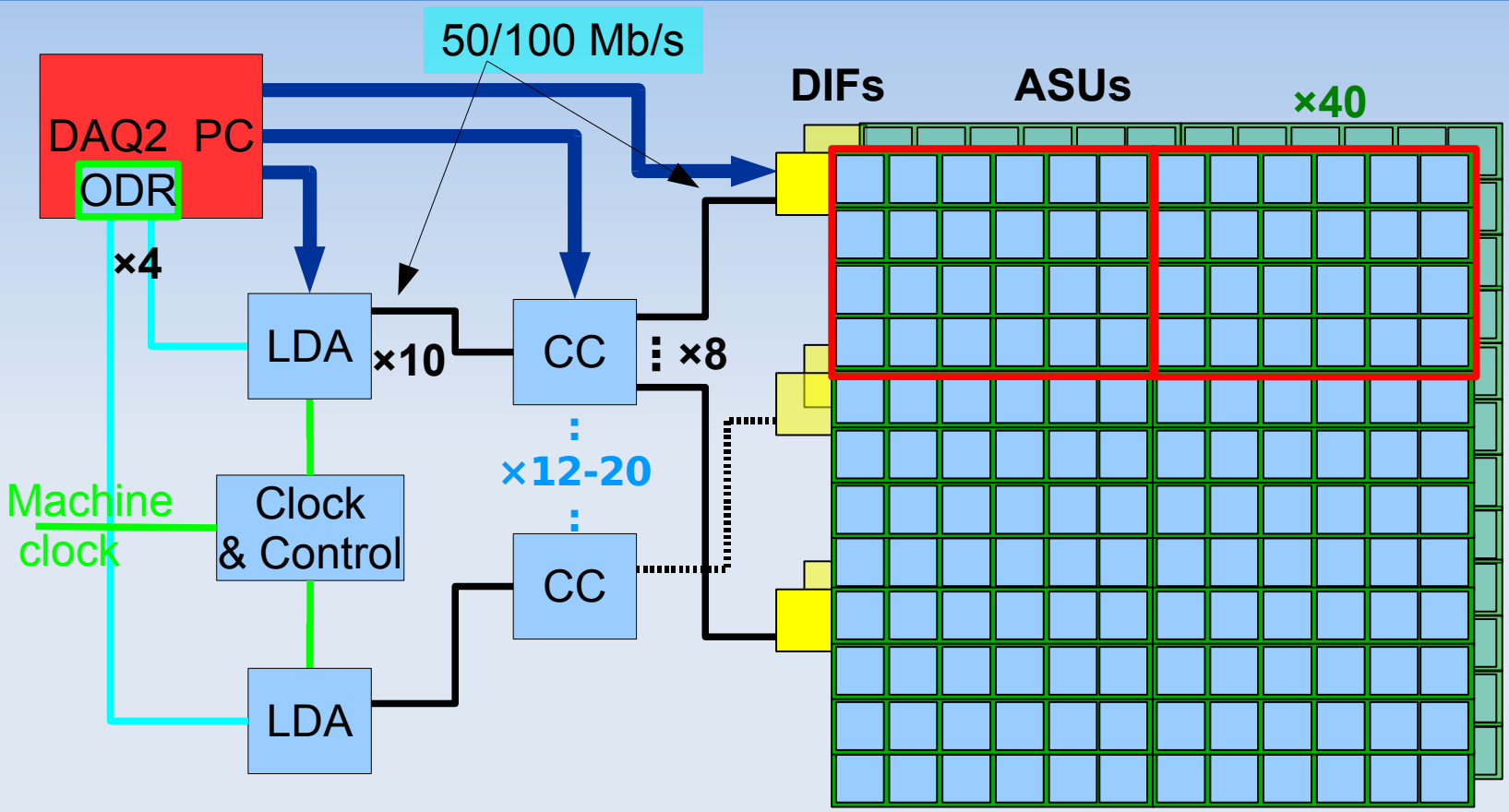
- 5-6 DHCAL1 board (20 HR's) in PS & SPS beams
- DAQ0 EUDET :
  - Use the complete DESY test bench

    *1 CRC (⊃ 6 FE) + VME Crate & controller + PC (with DAQ soft)*
  - **Avail. Early July → mid. August**
- USB for control and digital readout
  - libDHCAL + **Socket** (being written [*Simon Chollet*])
  - Protocol already defined (last year!) with Paul Dauncey.
- Config management & storing of data in LCIO files
- *RAW data Format to be defined*
- Analogue readout possible (level adaptation to be checked)
  - With analogue drivers replacement (done on 1 card now)

# DAQ m² (TB @ PS November)

- Direct USB readout of 3 DHCAL DIF.
  - 48 HardRoc/DIF, 144 in total
- use the DHCAL DIF test bench DAQ
  - Based one XDAQ [see pres. Of Ch. Combaret]
  - Altern: CALICE DAQ0
- Re-use of DHCAL USB code
  - Possible re-use of USB code for other DAQ's (ECAL Wafer,  in-situ DAQ, ...)
- Complementary with dev of next gen (DAQ2) ?
    - Database for the ASIC's configuration ?
    - Definition of the data format
    - Data classes
      - Should be compatible with LCIO format

# DAQ2 overview for the m³




1 PC: ~2 k€
1 ODR: ~4-5 k€
1 LDA: ~1.3 k€

Digital (Config, Controle)
Clock & Sync
Optique GigE
USB

3(4) DIF × 40 planes / 10(8?) conn.
- no CC: 12 (15?) LDA + 4 ODR's
- CC×8: ➔ 2 LDA, 1 ODR [5+4k€] + 12–20 CC

*Total data volume: (All HR full)~40×144×20kb = 117Mb*
*➔ ~ 50 ms on 2 GigE, ×2 sur LDA-CC, ... DIF*
*5 ASICs / plane (max 18) × 128 bits × ~100Hz → 128 kB/s*

# Concentrator Card

- Needed for DHCAL: 120 (40×3) DIF's
- Goal
  - **~Idem LDA**
  - Transparent
  - Broadcast of configs to all DIF's
    - Avoid management of adresses
      - ⇒ Modif of LDA's mecanism (ranges in place of fix adress), needed for redundancy ? (DIF bypass ?)
  - VHDL Blocks common to DIF /LDA
- Characteristics
  - ×8 channels
  - USB readout
  - Cheap
- Custom board
  - Cheaper (typ: 400€/card)
  - Prototype for a custom LDA:
    - → 40 channels
    - adapted for ILD embedding (see Rémi's talk)
- Conceptual work started [Frank Gastaldi, Antoine Mathieu]

# Tentative Path & Planning for CC

**Tentative agenda**

- Prototype 0 : Study of Firmware — ≤ dec 08
  - Mezzanine card around a big FPGA (XILINX evalution card) → *Sept 08*
  - Connection on 4 DIFS.
  - USB readout
  - Test of communication protocols

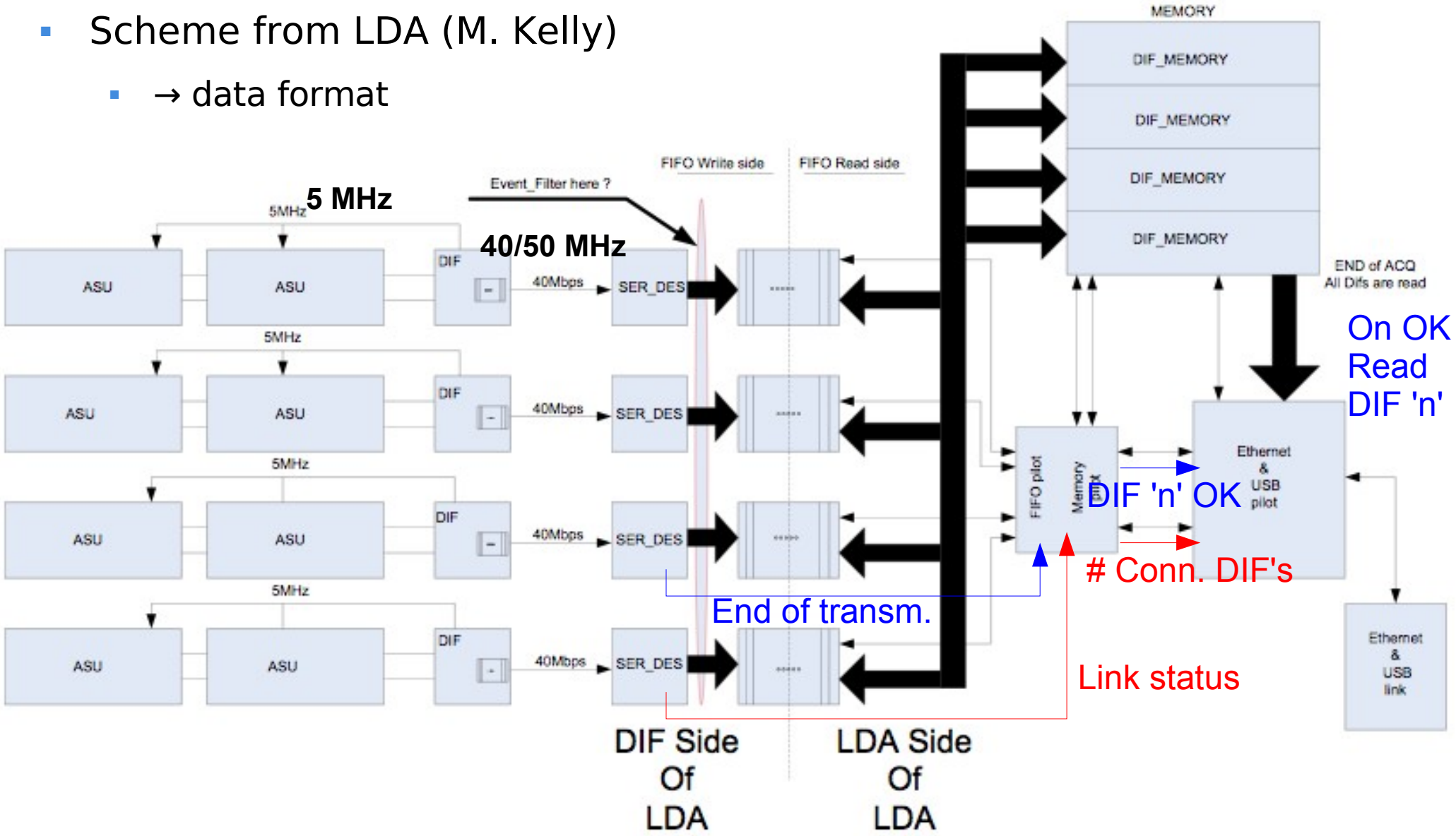
- Prototype 1: study for the production
  - 8 DIFs
  - Merging of data
  - USB readout

scheme: sept–dec 08
Prod: Jan-feb 09
Test: Feb-Apr 09
Prep final prod: Avr.-May 09

- Production & test of ~20 cards — June-July 09

# Merging scheme on CC / LDA

- Scheme from LDA (M. Kelly)
  - → data format



# RAW Data format

- ODR/LDA protocols [wrapping] well defined
- RAW data format (≃"out of DIF")
- Allow for merging, with internal consistency markers
- Example:

Inside a "LDA block" (as proposed By M. Kelly): words of 16

```
Nb_of_DIF                                   (filled by DIF, modified on CC when merging)
n ×  | DIF_Header == Word Type  + DIF_ID (typ. 8 bits) + type of Data (ASIC, SC, Config)
     | Nb_of_ASIC                          OR  | Nb_of_ADC_words      OR  | Nb_of_SC_words
     | n ×| Nb_of_words (filled on CC/LDA ?)  | n ×  ADC data             |....
     |     | ASIC Data stream
     | DIF trailer (padding words)
+ K character send by the DIF
```

Move Here ?

- CC: Change the Nb_of_DIF, count data words & aggregate the data
- Coding: 8b/10b corrects a bit the errors.
  Allow for End of data signal

# DAQ2 M³ Test Beam contingencies

- ASIC's in auto trig
- DHCAL Data rates in TB
  - Expected from 100 GeV π (J-C. Brient's note)
    - 5 ASIC's touched in average (max 18) / plane
    - All on the central DIF
  - 1 evt = 160bits
    - Readout time 1 ASIC @ 5Mb/s = 0.032ms
    - RO 1 plane ~ 0.16ms [6 kHz]
  - 1 full HR (128 events) = 20480 bits
    - Readout time 1 full HR @ 5Mb/s = 4ms
- see Remi's talk for ECAL
- TB rates: $10^4$ ($10^8$ at FNAL ???) part/s during 10s/min (SPS mode).
- RPC limitation: ~100Hz/cm²
  µMegas: basically not limited...

# DAQ2 TB working modes

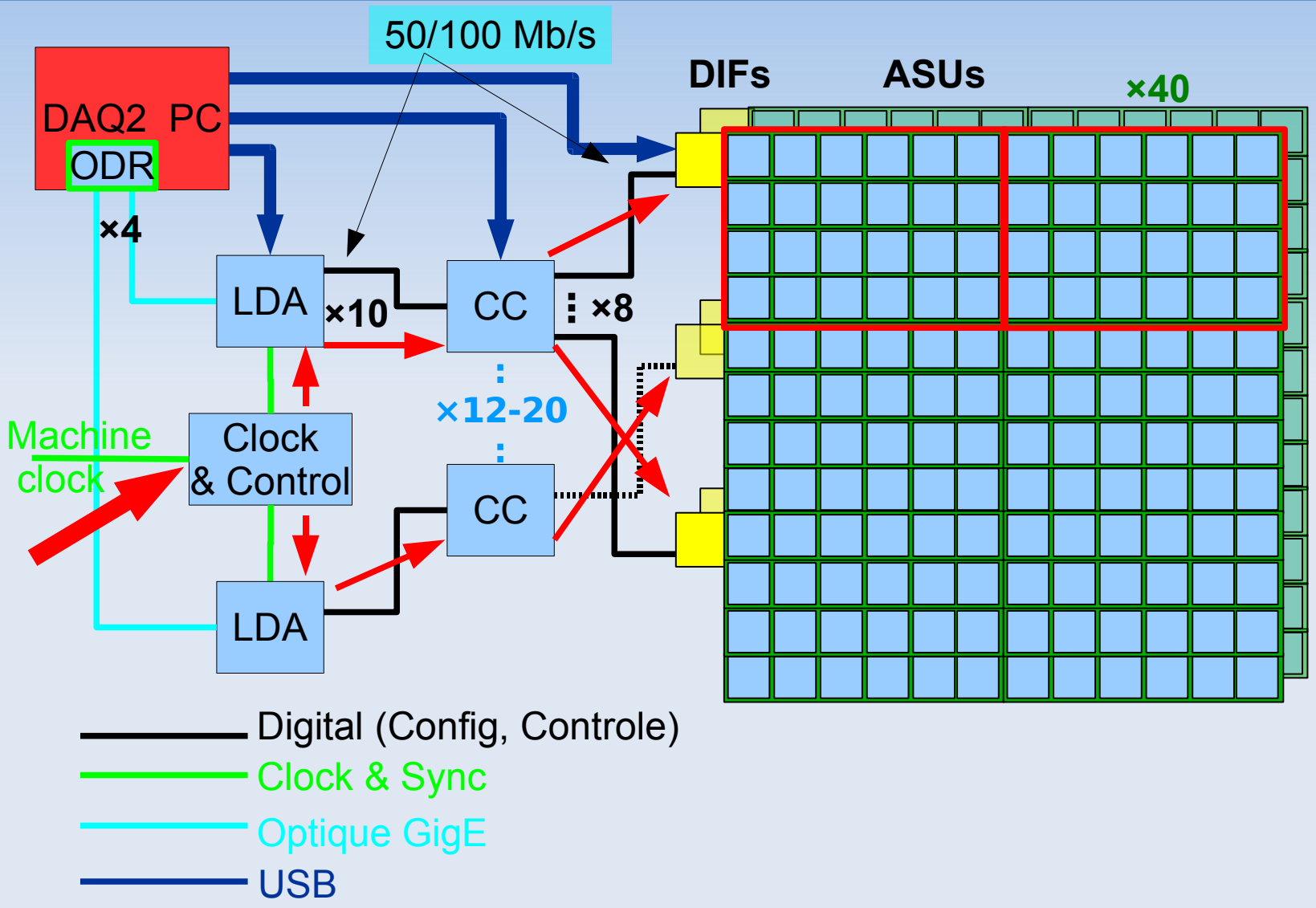
## **Burst mode** (≤128 FOR DHCAL)

- **No external trigger** but independent recording of trigger mode (⊃ Timestamp) *(could be 1 HR recording Trigger bits)*
- Data sync internal [synchronisation on reset of BC ID on all HR].
- Internal «RAM full» management needed Every 128 DHCAL [16 ECAL] events
  - LOCAL: in DIF with immediate RO of SLAB
    - 4 ms for 100 GeV π's without Reset (avoid loss of sync)
    - **Indiv DT**: might be hard too handle.
    - Local storage of data ????
  - Global
    - fast Ramfull → DAQ (stop of Acq, RO of all chips, and restart)
    - periodic interruptions (counting of part ? Hodoscope HR ?)

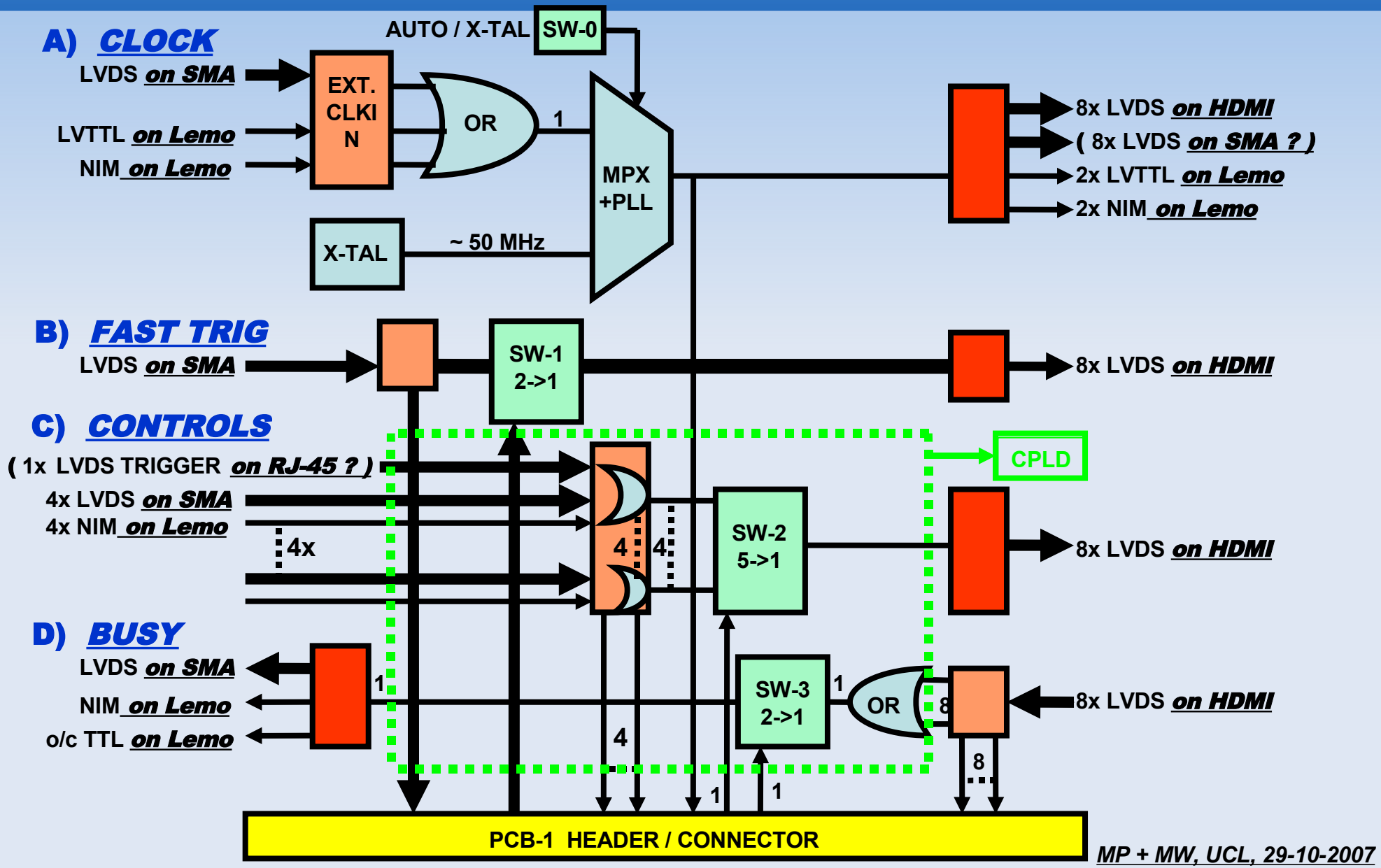
## **Single Event**

- **External trigger** (hodoscope) → DIF
  - Stop Acq
  - Read chips:
    ~0.16ms (+ noise if any)
    ⇒ **max 6kHz** on 100 GeV π's
  - Start Acq
- Data sync (for Event building)
  - On synchronized BC ID
  - On trigger timestamp (e.g. On DIF Timecounter on last internal trigger to ext. trigger)
- Fine if not RAM full
  e.g. # rejected triggers + noise event per chip < 128 [16 for the ECAL!]
  - Ideally: have a circular buffer

# DAQ2 signals



# Clock & Control Card [reminder]



# DAQ2 planning: test & integration

- Test set-up in September ?
  - Test of HW (⊃ CC)
  - Protocols, data format, config loading
  - Acquisitions modes
  - Integration
    - Event display, slow control, config database

**Test Setup:**
- 1 PC with DOOCS + libODR/device
- 1 ODR
- 1 LDA incl FW
- 1 CCC
- 1(2?) DIF

# Conclusion

- Lot of work ahead
- Pending questions
  - Configuration distribution: PROM vs SWITCHES (Physical mapping) optimal topology (for redundancy)
  - Running modes
  - Trigger distribution
  - Minimal amount of RAM in ~~DIF~~, CC, and LDA.
  - Complete out of DIF Data format
- Need some clarification on many points to have a working set-up for next year
  - Meeting tomorrow 9am room 032