IN2P3

Omega

CAL LUR IPN Orsay

CALICE Electronics issues

2 June, 2008

Orsay MicroElectronic Group Associated

Electronics for technological modules

- Summary of Argonne meeting
- Some issues from London's meeting
- pressing issues :
  - Hardroc, Spiroc and SKIROC results and plans [Omega,LPCC]
  - ASIC Production issues
  - ECAL ASUs and signals distribution [Cambridge, Manchester, LAL, LLR]
  - AHCAL HBUs [DESY]
  - DHCAL ASUs and DIF [Lyon, LAPP, LLR]
  - Power supplies considerations
  - 3rd generation R&D [Omega,LPCC,LPSC]

HARDROC2

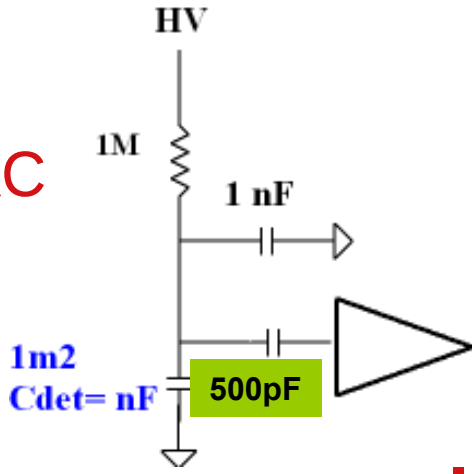
- HARDROC1 could go to production directly
  - No major bug
  - Measurements going on since > 1 year : still some imperfections found
  - Main drawback is package size and double row bonding yield

- HaRDROC2 could be prototyped in june 08
  - Keep HARDROC1 basic architecture and backward compatibility
  - Have 3 very different thresholds
  - Move bonding pads to single row
  - + many small changes

  (gain accuracy, power pulsing…)
  - Area : 25 mm2

HV sparks (ESD)

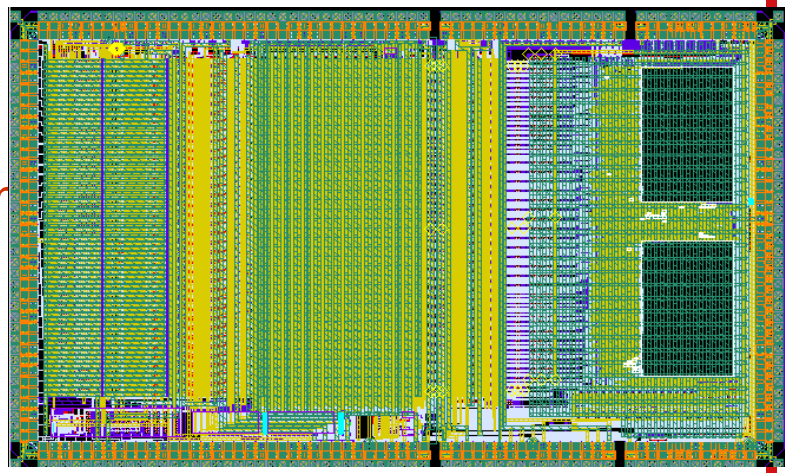
- ASIC inputs:
  - protection PADs (AMS library): robustness up to 2kV HBM (100pF)



- From T2K large µmegas [E. Delagnes], AC coupling necessary for area > 10cm^2:
  - **Maximum decoupling** capacitor that can be **integrated: ≈30pF** (50µm x 600 µm) and **loss of signal**
  - **EXTERNAL CAP=500 pF/ch** to ensure protection
  - Drawbacks of a decoupling cap: Xtalk, space
- HV sparks robustness for **large** GEM-like detectors requires dedicated design effort

SPIROC2

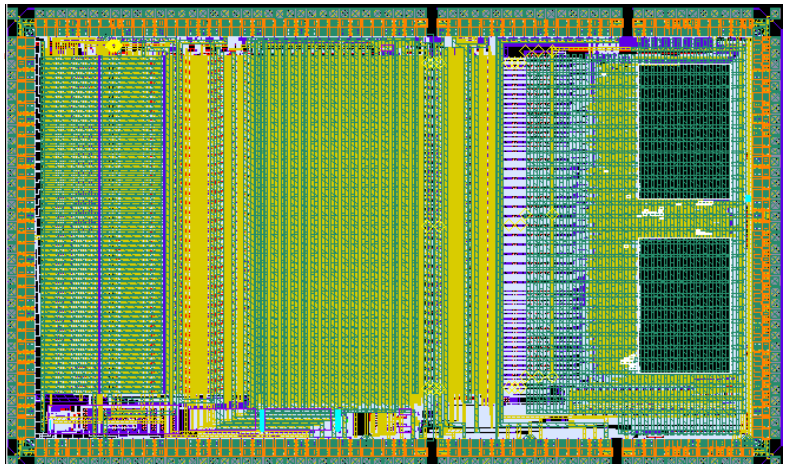
- SPIROC1 needs one more prototype before production
  - 2 major bugs : no probe, no ADC
  - Analog part so far OK, can be used to replace FLC_SiPM
  - Autotrigger at ~50-100 fC
  - Could be tested with existing detector and DAQ
  - Many more measurements to be done : complex chip
- SPIROC2 could be prototyped in june 08
  - If no major change
  - Possibly SKIROC compatible
  - TQFP208 package : 28x28x1.4 mm



SKIROC2

- SKIROC1 cannot be used for detector
  - Digital part outside
  - needs one more prototype before production
  - Analog part so far OK, can be used to replace FLC_PHY3
  - Many more measurements to be done

- SKIROC2 could be SPIROC2
  - Bypass input capacitance
  - Possibly limited dynamic range
  - But ECAL PCB needs 64 channels

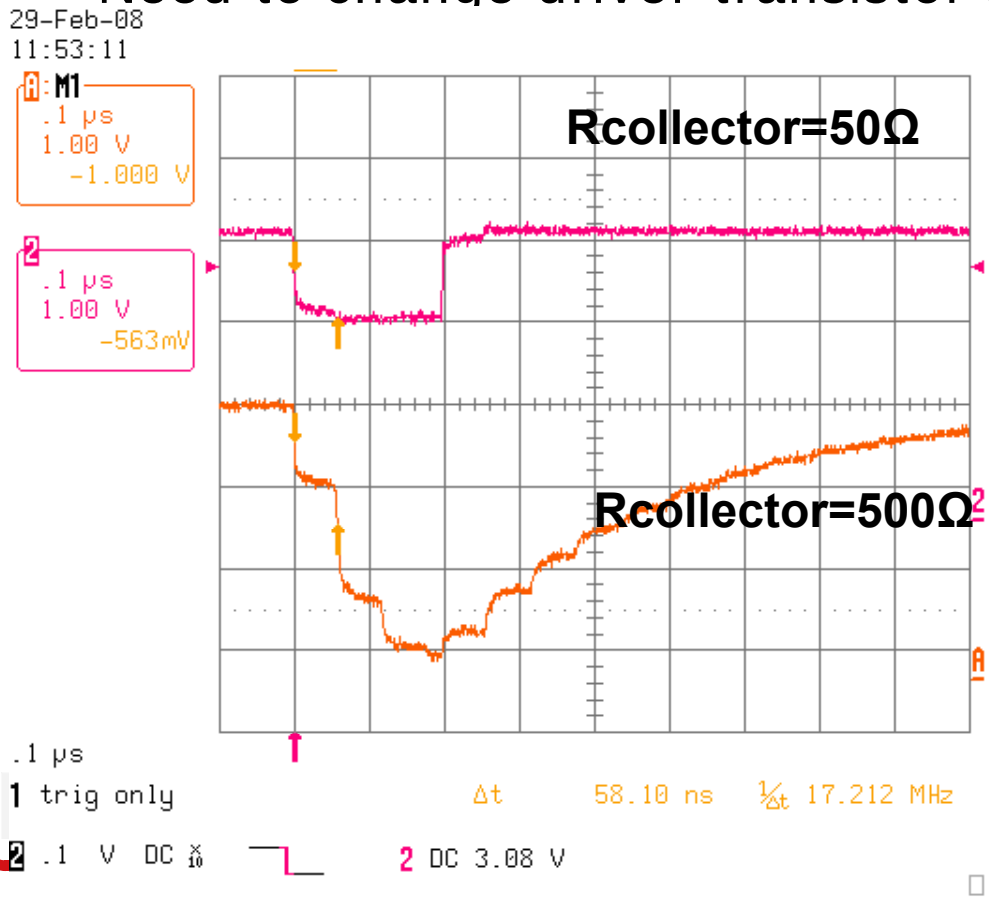


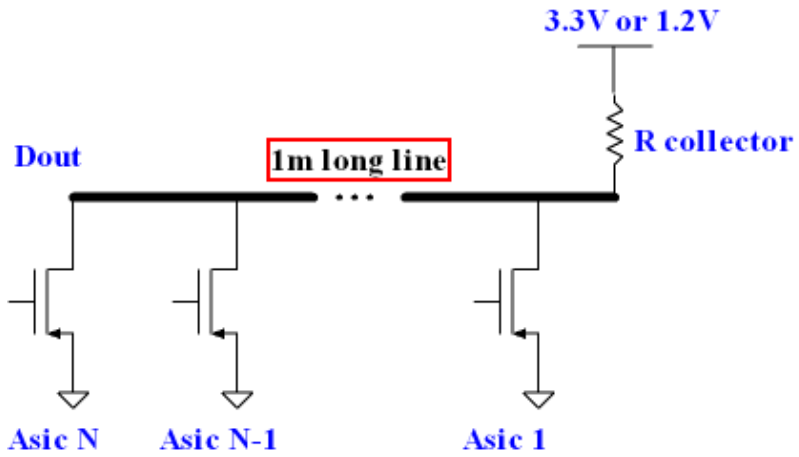
Digital part

- Digital part validated on hardroc
- VHDL code available
- Still many small changes coming up [see F. Dulucq]
  - Many improvements on Slow Control
  - Default mode
  - Last FF for daisy chain timing requirements
  - Reduce PAD number
  - Increase reliability:
  - Double some drivers
  - Possibility to disconnect bus drivers
  - Add bypass on critical signals
  - Remove “dummy frame” and improve digital operation
  - Management of PowerON for digital part
  - Start / Stop clocks
  - Start / Stop LVDS receivers...

Open collector signals after 1m long line

- 5 m data line / slab -> 500 pF
- Multiple reflections when unterminated : 1 MHz max
- 50 ohm termination => clean, 10 MHz R/O possible, power dissipation 10 mW/slab in DIF
- Need to change driver transistor size in ASICs



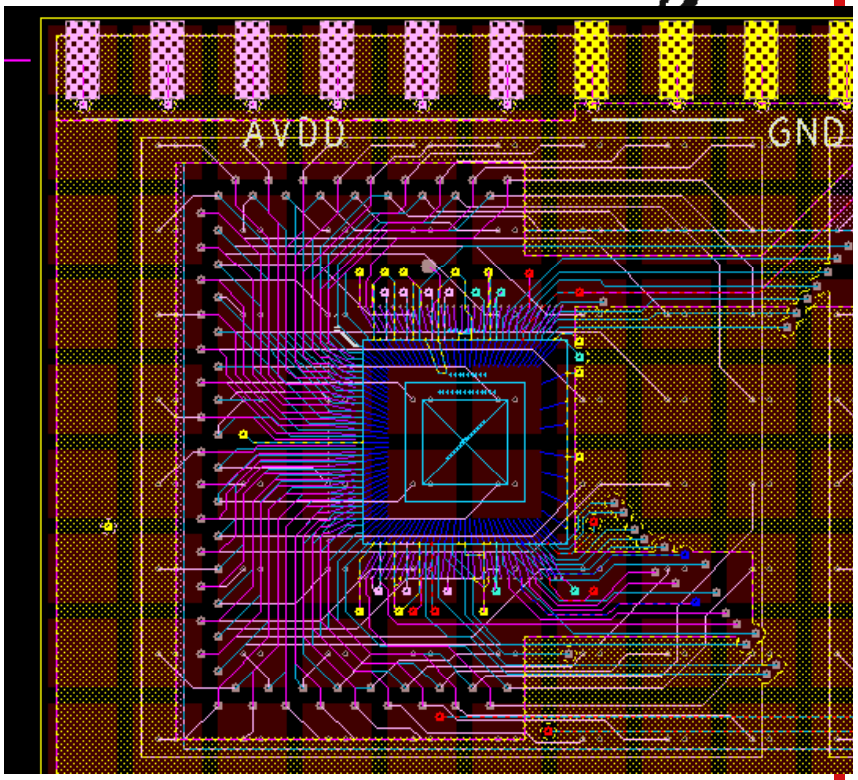


Tentative schedule

- June 08 : submission of HaRDROC2 and SPIROC2
- Sept 08 : chips in hand and for standalone tests
- March 09 : production run with HaRDROC2, SPIROC2 and (challenging) SKIROC2 (64ch)
- June 09 chips available for ASUs

PCB developments

- ECAL : ASU prototype
  - FEV5 expected soon
  - Uses 4 HArdroc chips
  - Can test stitching
  - Connects to proto DIF



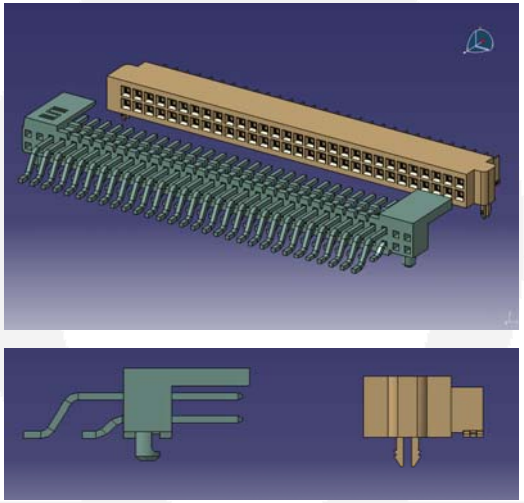
- AHCAL : HBU
  - First prototype with Spiroc

- DHCAL : m2 prototype boards
  - For RPCs and µMEGAS : different sizes and connections

DIF issues

- Common connector specification
- 90 pins
- Thanks to DIF task force

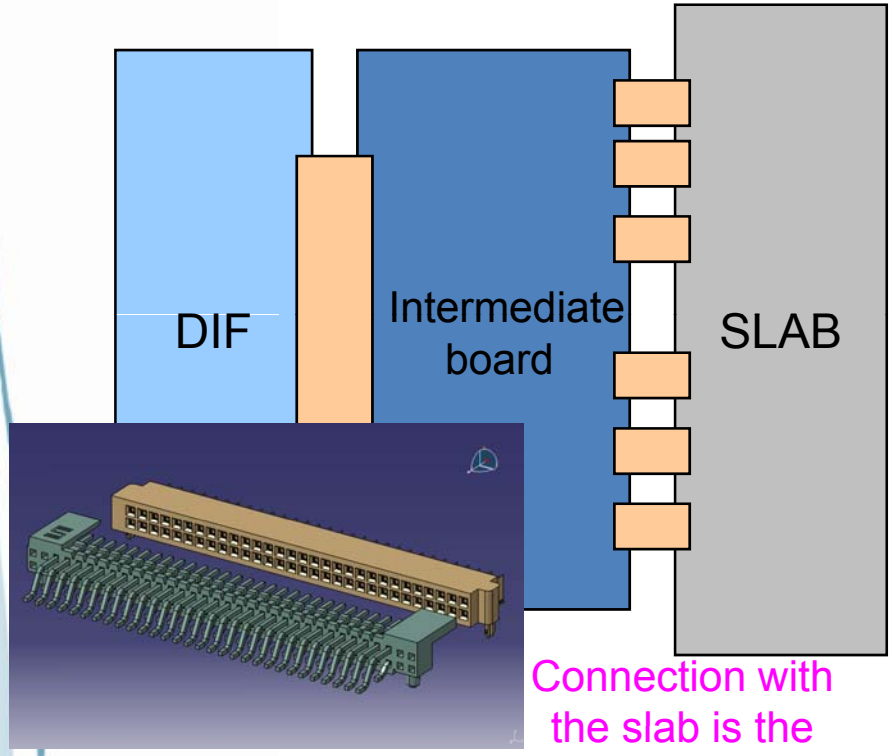
	N pins
Analog	3
User Single Ended	22
Controls Single Ended	5
Digital Readout	12
Power pulsing controls	5
LVDS signals	16
Slow controls signals	8
POWER pins	6
GND	13
TOTAL	**90**

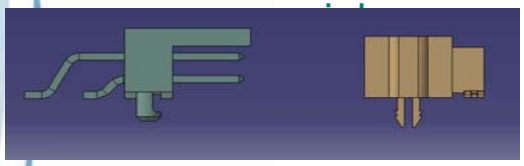


Samtec FSH/ SFMH ?

GND	1	2	GND
MUX3_CSn	3	4	Analog_0
MUX2_CSn	5	6	GND
MUX1_CSn	7	8	Analog_1
spare1	9	10	GND
MUX_ENN	11	12	C_test
MUX_WRN	13	14	GND
spare2	15	16	MUX_A4
en_otaq	17	18	MUX_A3
GND	19	20	MUX_A2
SR_reset	21	22	MUX_A1
hold	23	24	MUX_A0
spare3	25	26	Ramfullext
SR_IN	27	28	Reset_BCID
spare4	29	30	GND
SR_OUT	31	32	Resetn
spare5	33	34	Start_Conv_daqb
SR_clk	35	36	End_Readout
GND	37	38	Start_acq
TransmitOn_3	39	40	RamFull
Pwr_analog	41	42	Dout_3
TransmitOn_2	43	44	GND
Pwr_dac	45	46	Dout_2
Pwr_ss/Pwr_sca	47	48	Start_Readout
GND	49	50	Trig_ext
TransmitOn_1	51	52	Start_Readout_Bypass
Pwr_digital	53	54	Dout_1
TransmitOn_0	55	56	GND
Pwr_adc	57	58	Dout_0
SC_SROUT	59	60	SC_SRIN_BYPASS
SC_SROUT_BYPASS	61	62	SC_SRIN
SC_select	63	64	SC_reset
SC_clk	65	66	SC_load
User_LVDS_P	67	68	User_LVDS_N
Trig_Ext_P	69	70	Trig_Ext_N
DVDD	71	72	AVDD
Clk_5MHz_0_P	73	74	Clk_5MHz_0_N
Clk_5MHz_1_P	75	76	Clk_5MHz_1_N
GND	77	78	GND
Clk_40MHz_0_P	79	80	Clk_40MHz_0_N
Clk_40MHz_1_P	81	82	Clk_40MHz_1_N
DVDD	83	84	AVDD
Raz_Chn_P	85	86	Raz_Chn_N
Val_Evt_P	87	88	Val_Evt_N
AVDD	89	90	AVDD

Interface with the SLAB





Samtec FSH/ SFMH ?

Connection with the slab is the same as the one between 2 ASUs.

0 Ω resistor, …

- Use of a small intermediate board, which is specific to the FE ASIC and ASU.
- The DIF can be used :
  - Whatever the FE ASIC.
  - Whatever the slab (RPC, uM)
  - Whatever the slab to slab connection.
- 1^{rst} ASU is the same as the others.

Power supplies

- A very critical issue !!!
- Power supplies won't be dimensionned for continuous operation, but for 1/100 of the load.
- Need local storage (capacitors, even a battery!) on power board and regulators to accomodate large voltage swing
- Simple calculation (ECAL)
  - Slab = 24 000 channels
  - 1 mA/channel unpulsed => 24 A/slab
  - With a 24 000µF capacitor dV/dt = 1V/ms => acceptable

Done and to do list

- DONE
  - Second generation ASICs prototypes
  - Auto-trigger
  - Daisy-chain readout

- TO BE DONE :
  - PCB stitching (in progress)
  - Tests of bonding chip on board for ECAL (in progress)
  - DIF prototypes (in progress)
  - Tests of power budget with existing chips and boards
  - Tests of power pulsing with Imad's boards
  - Integration issues (in progress)
  - Design of Power distribution (no one' s looking)
  - HV distribution and robustness
  - Testbeam with 2nd generation detectors
  - MEASUREMENTS, MEASUREMENTS, MEASUREMENTS