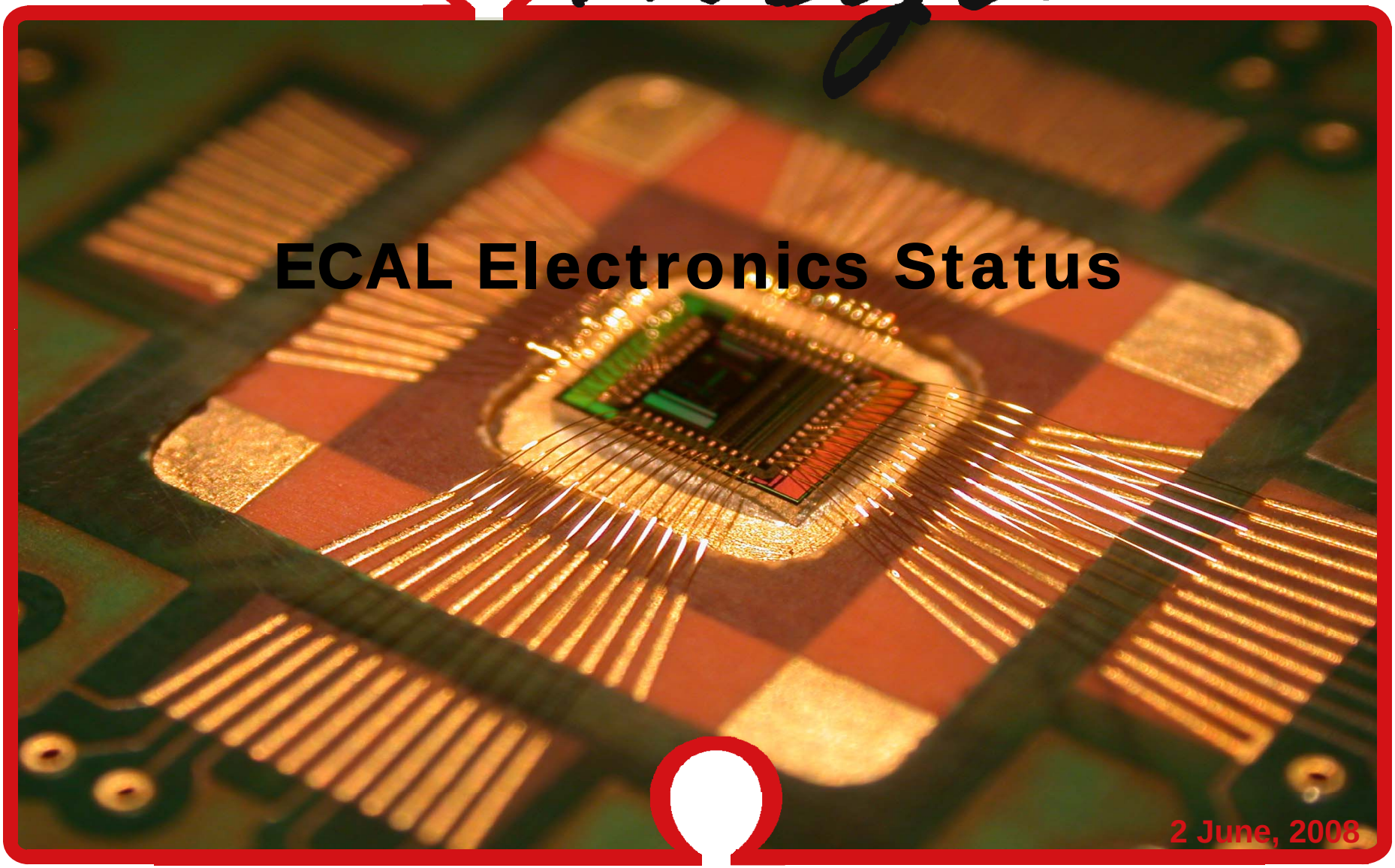
IN2P3 CSNSM LAL LPNHE IPN Orsay

Omega



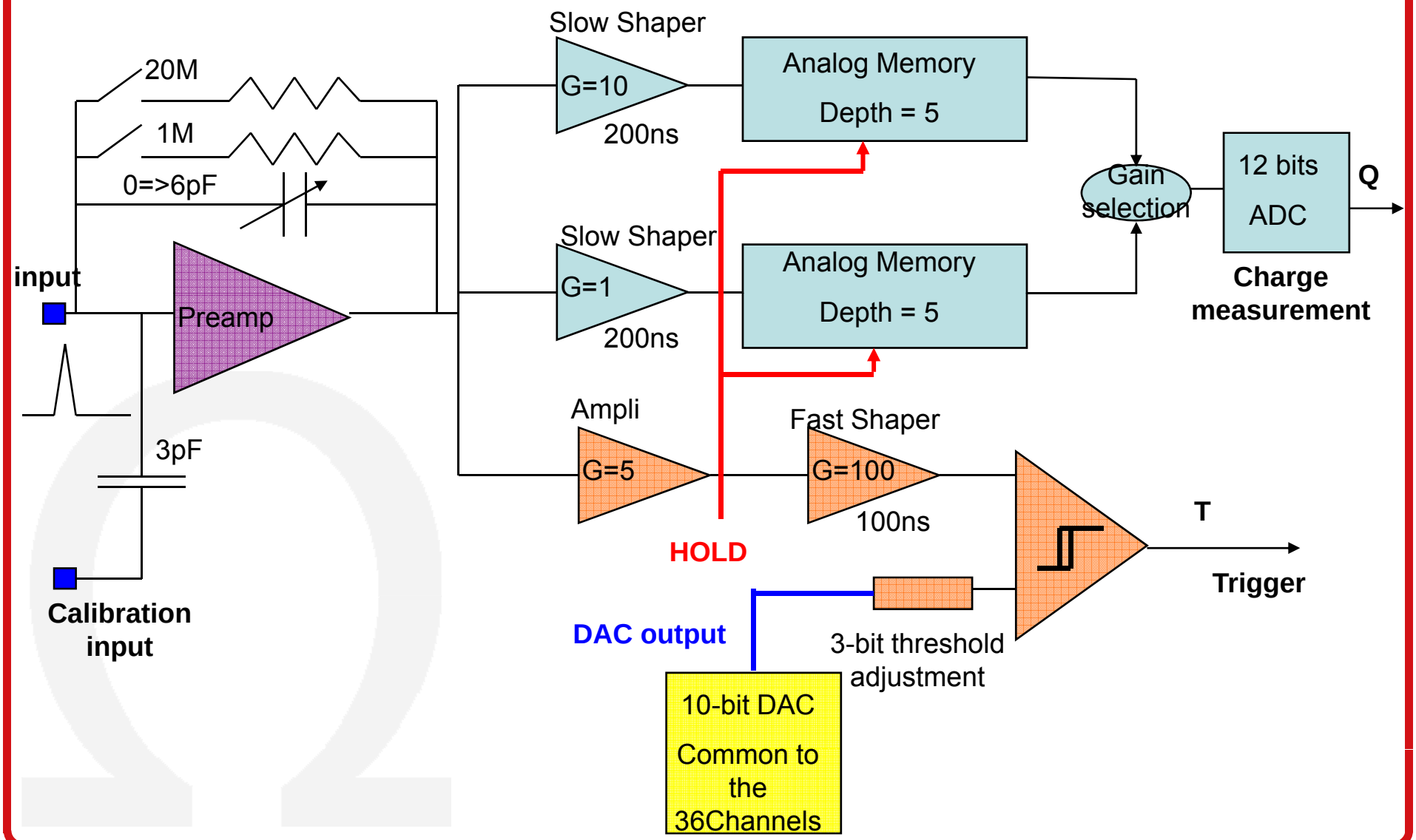
ECAL Electronics Status

2 June, 2008

Orsay MicroElectronics Group Associated

SKIROC measurement

Reminder : One channel



Pedestal dispersion

The pedestal measurement is coherent with what we expect :
-No pedestal pattern (random values according to statistical dispersion)
-Statistical dispersion equivalent to what we get with that technology

Standard deviation :

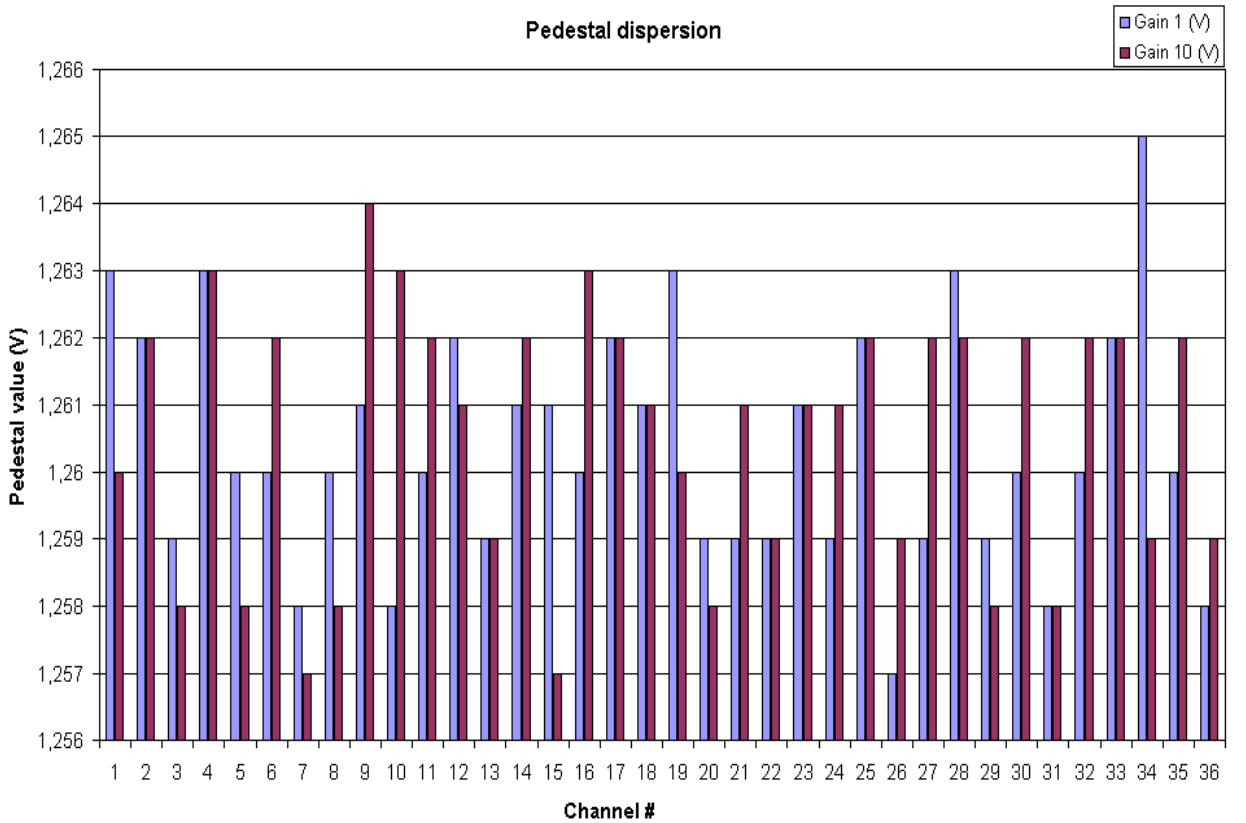
$\sigma_{Gain\ 1}$= 1.8mV

$\sigma_{Gain\ 10}$= 1.95mV

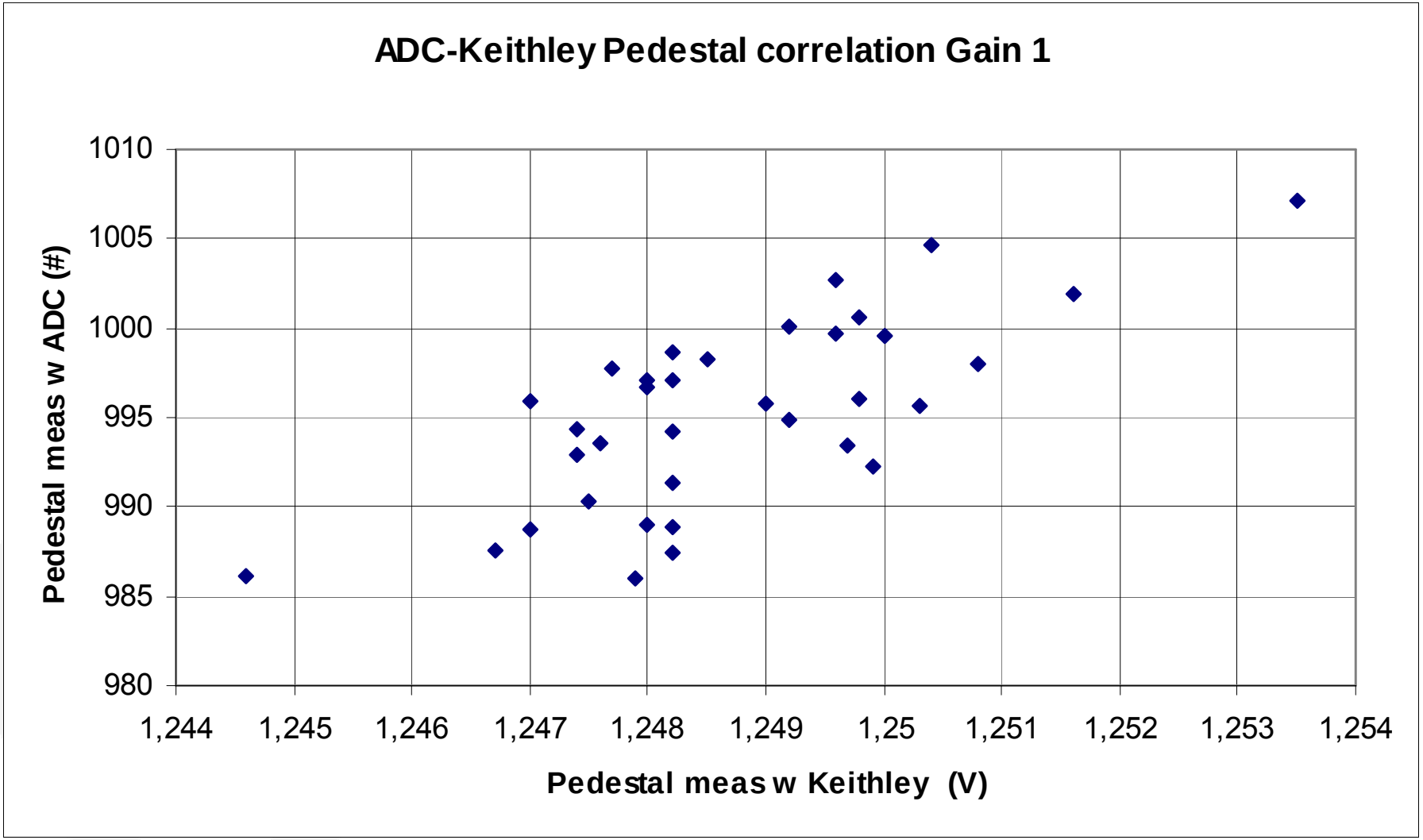
Standard deviation ADC

$\sigma_{Gain\ 1}$= 1.84mV

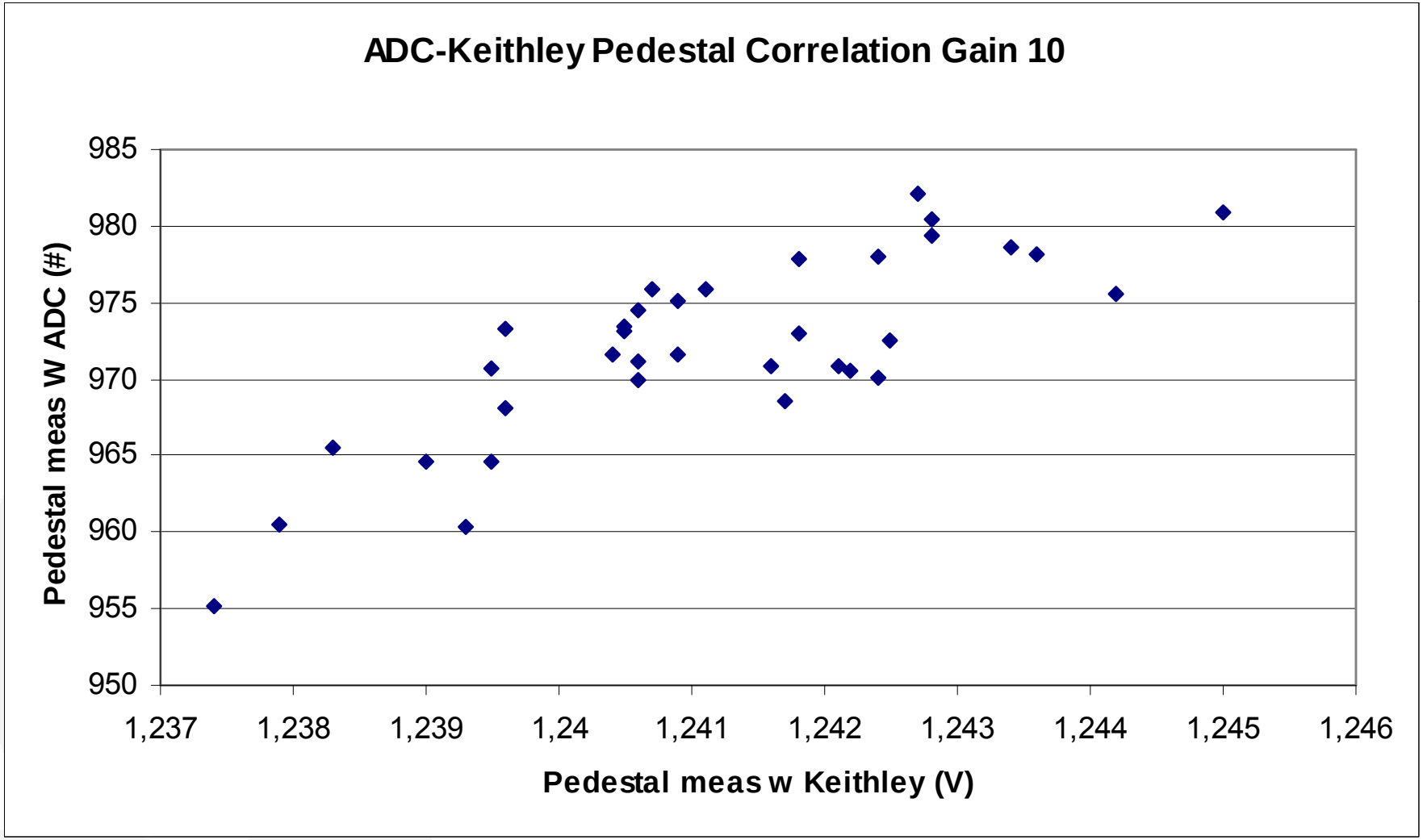
$\sigma_{Gain\ 10}$= 2.1mV



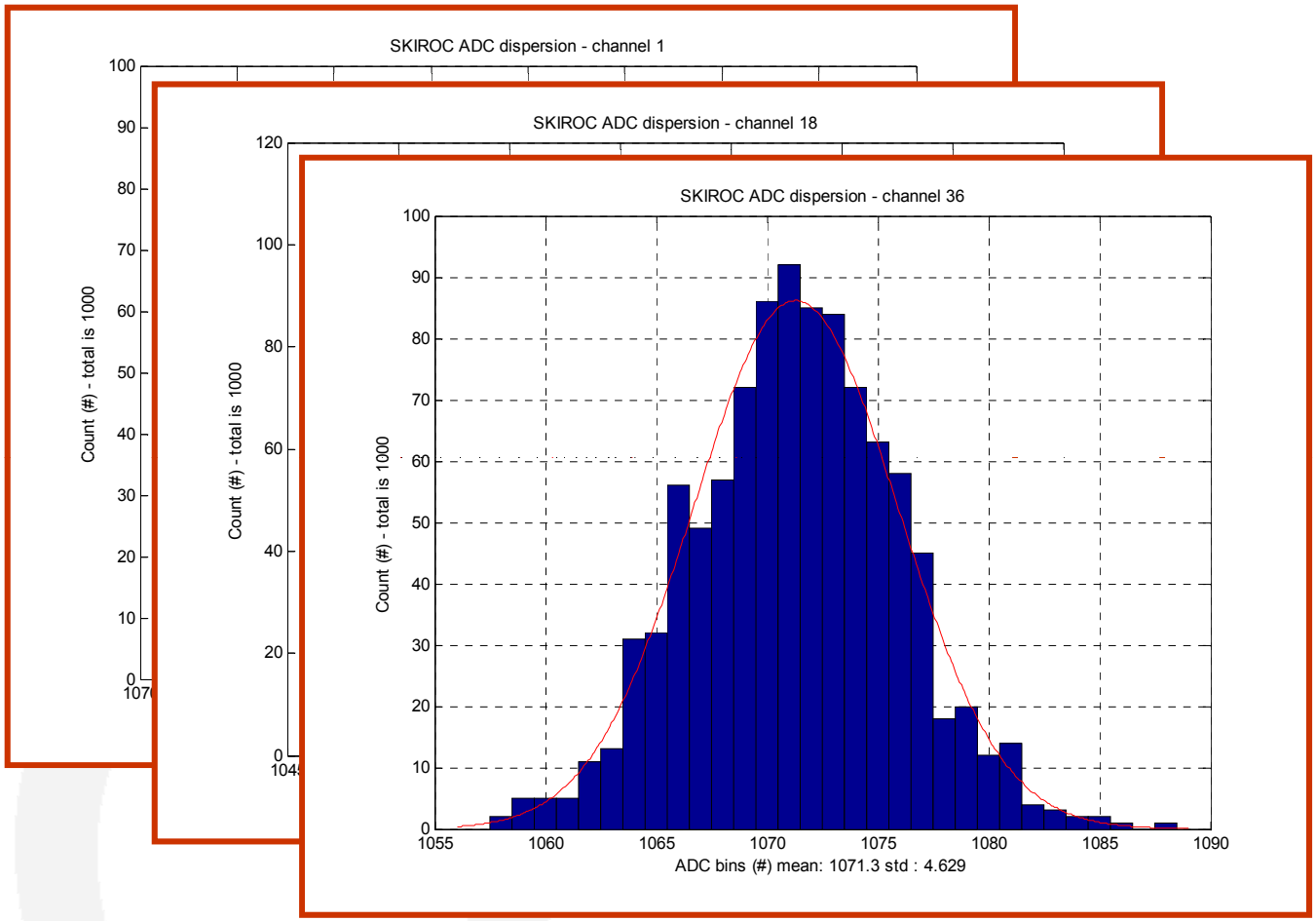
ADC meas


ADC-Keithley Pedestal correlation Gain 1
Pedestal meas w ADC (#)
1010
1005
1000
995
990
985
980
1,244
1,245
1,246
1,247
1,248
1,249
1,25
1,251
1,252
1,253
1,254
Pedestal meas w Keithley (V)

ADC meas

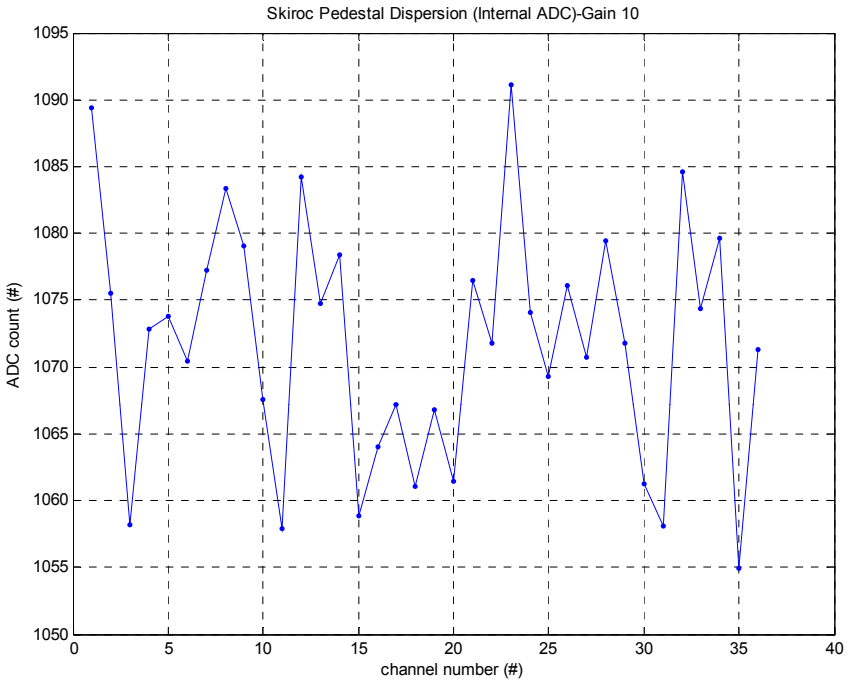

ADC-Keithley Pedestal Correlation Gain 10
Pedestal meas W ADC (#)
985
980
975
970
965
960
955
950
1,237
1,238
1,239
1,24
1,241
1,242
1,243
1,244
1,245
1,246
Pedestal meas w Keithley (V)

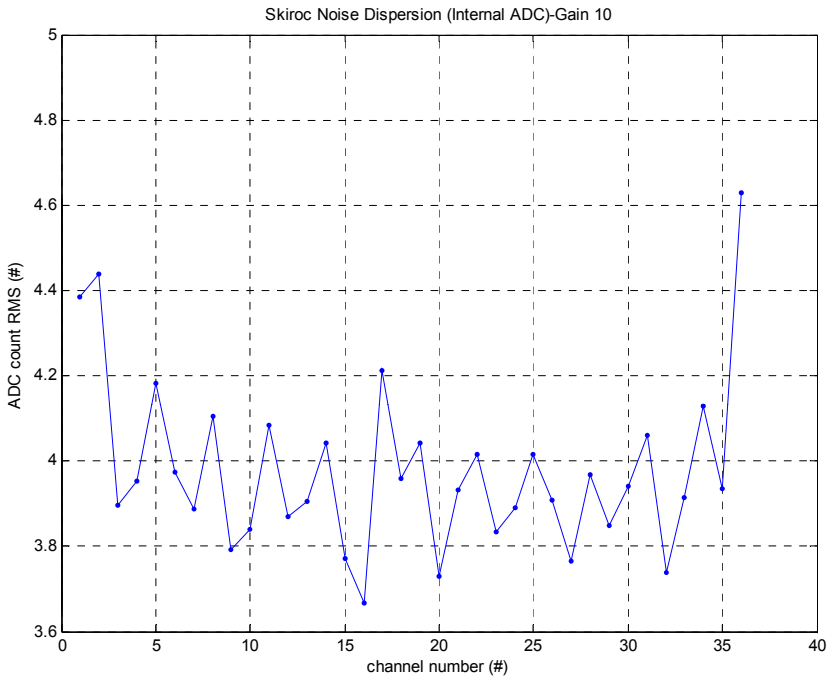
ADC noise – Gain 10



ADC bin = 350µV
Noise is gaussian

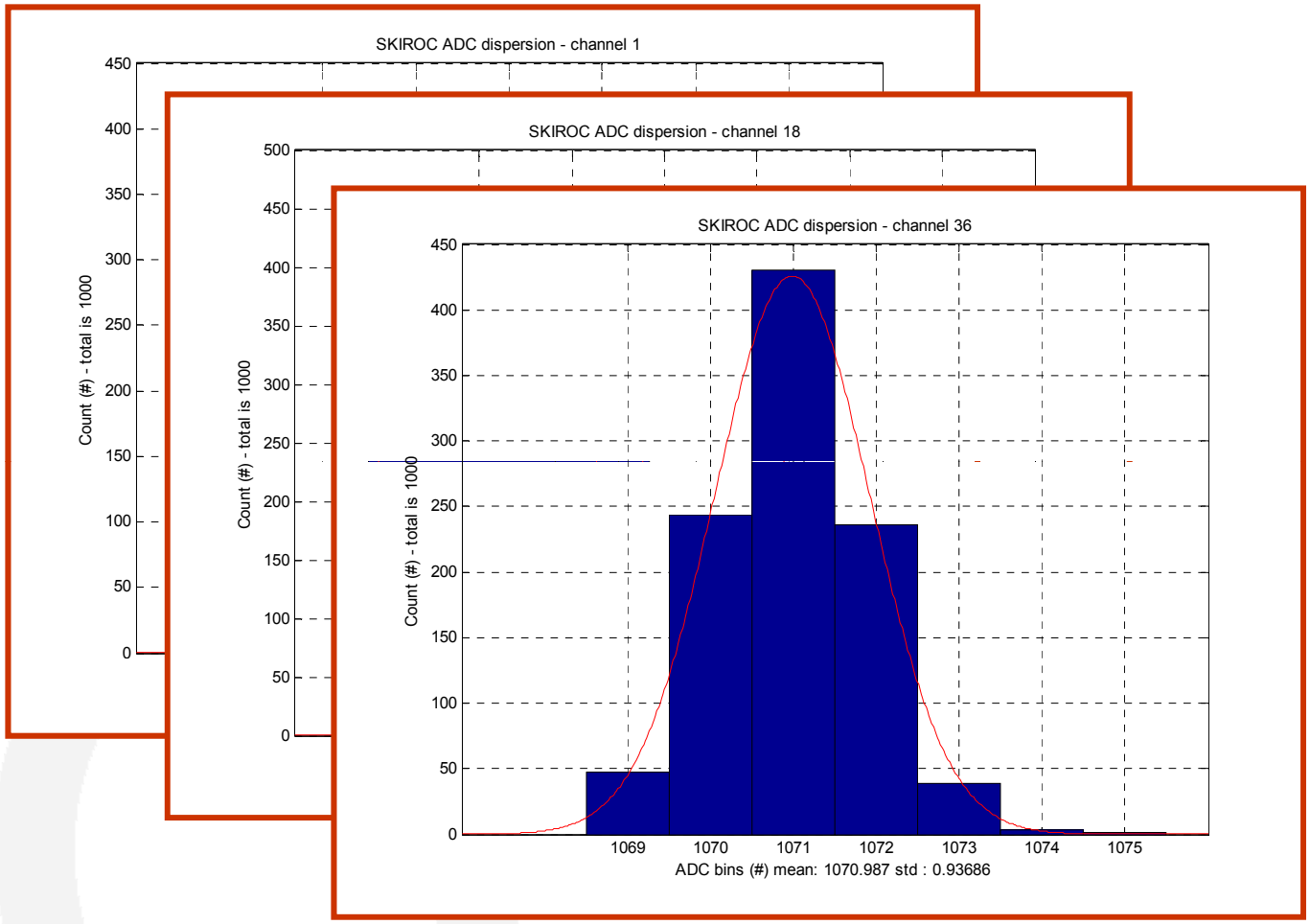
ADC noise – gain 10





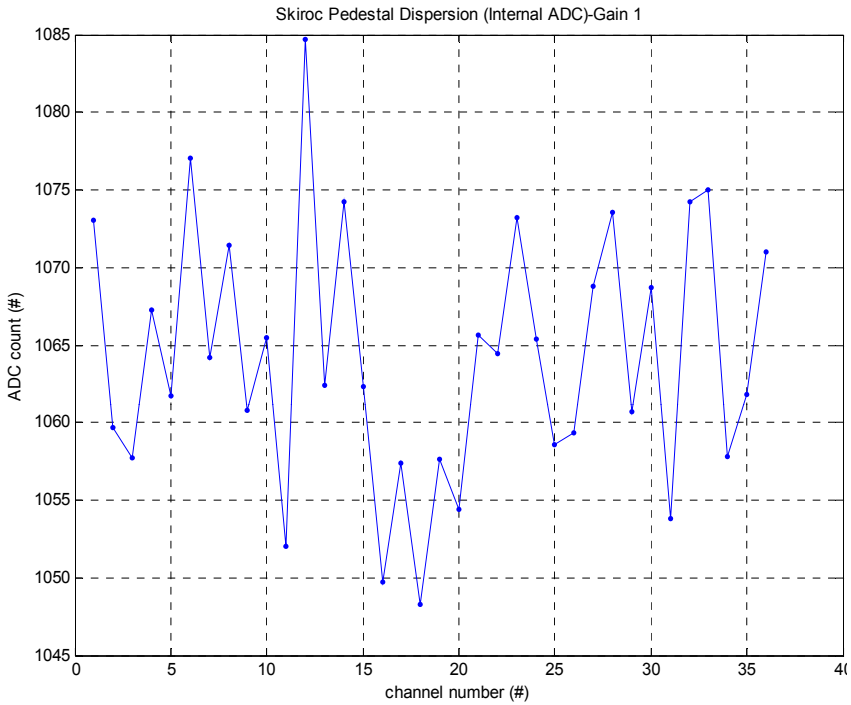
- Pedestal is nicely random – no pattern
- Noise is a bit higher on the border channels → side effect to be understood
- Mean noise is 4 ADC count (1.4mV) – MIP/Noise ~8 → to be improved
- Same results with analogue measurement → ADC noise contribution OK

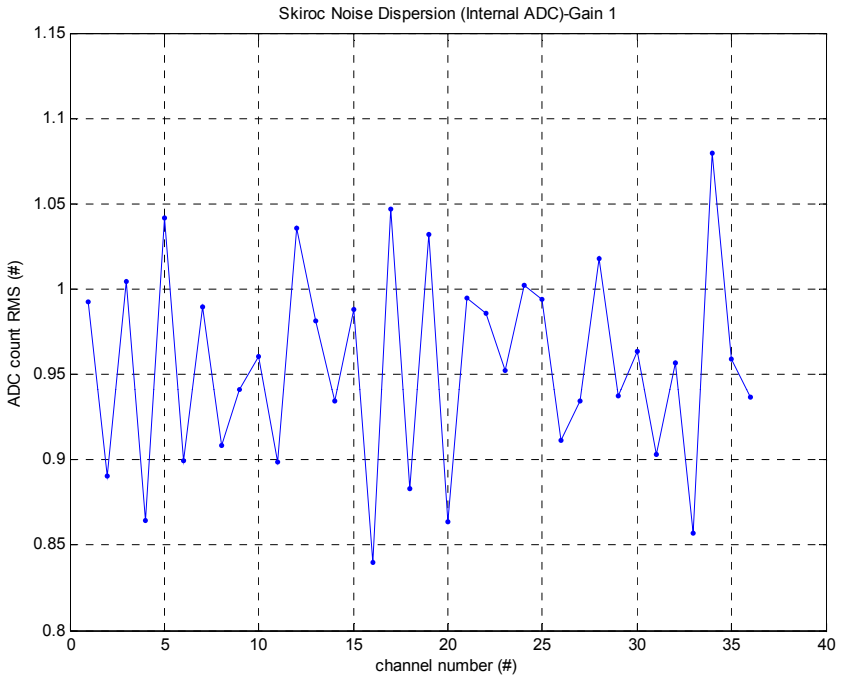
ADC noise – Gain 1



ADC bin = 350µV
Noise is gaussian

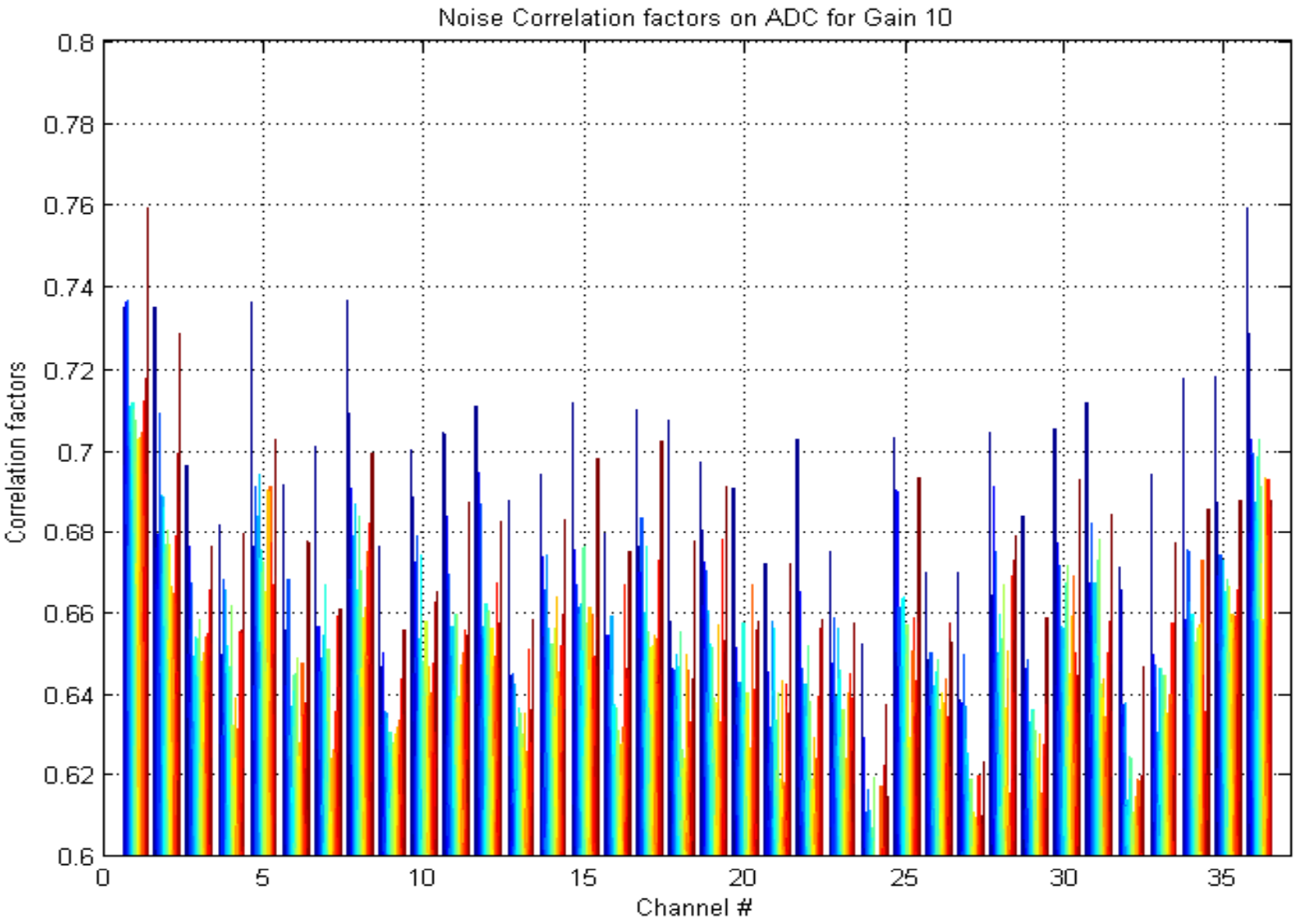
ADC Noise – Gain 1



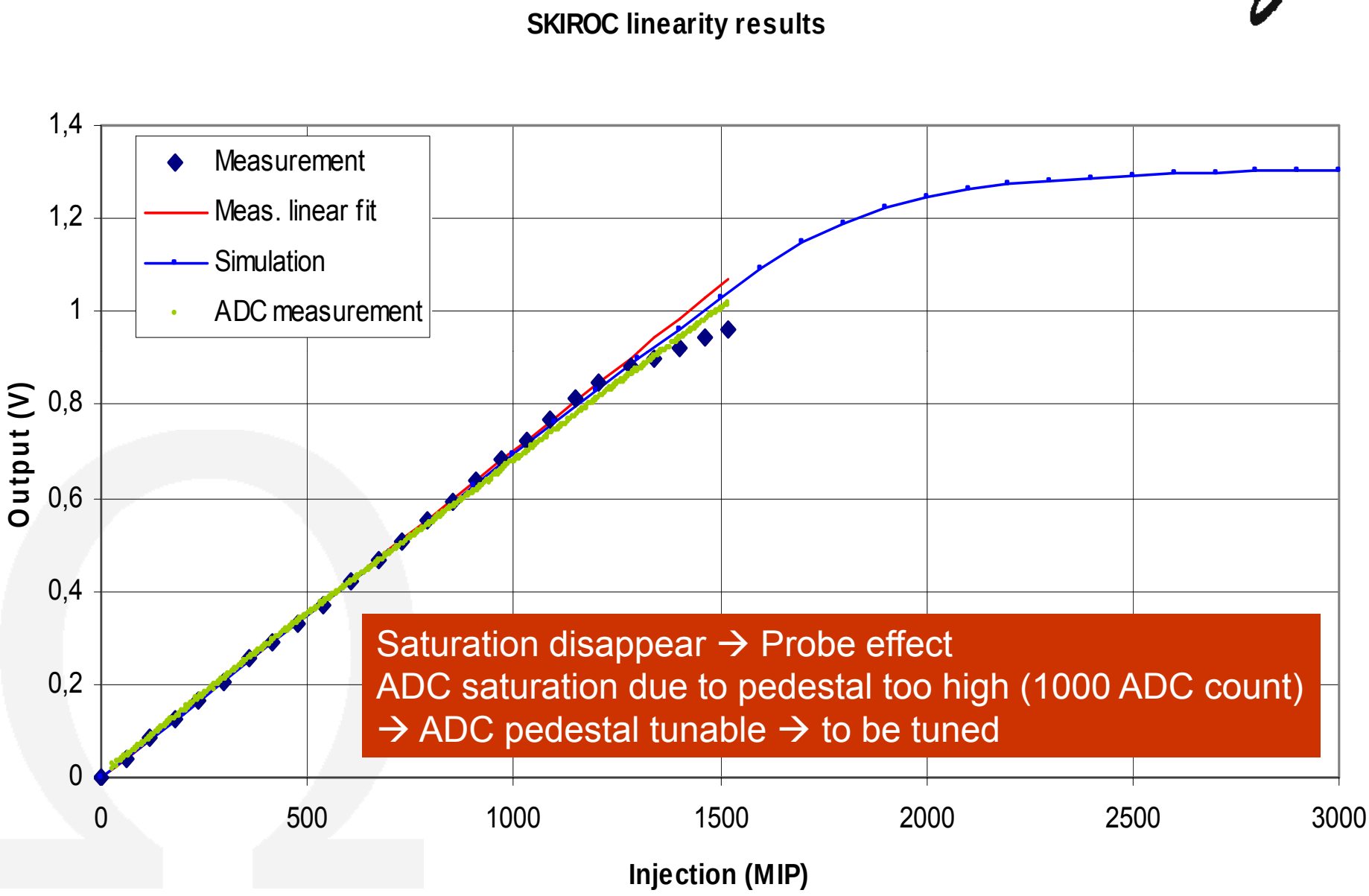


- Pedestal is nicely random – no pattern
- Noise is random → side effect comes from FE electronics, not ADC
- Mean noise is 0.95 ADC count RMS (330µV) - Good
- Results with analogue measurement is 250µV → a few ADC noise seen

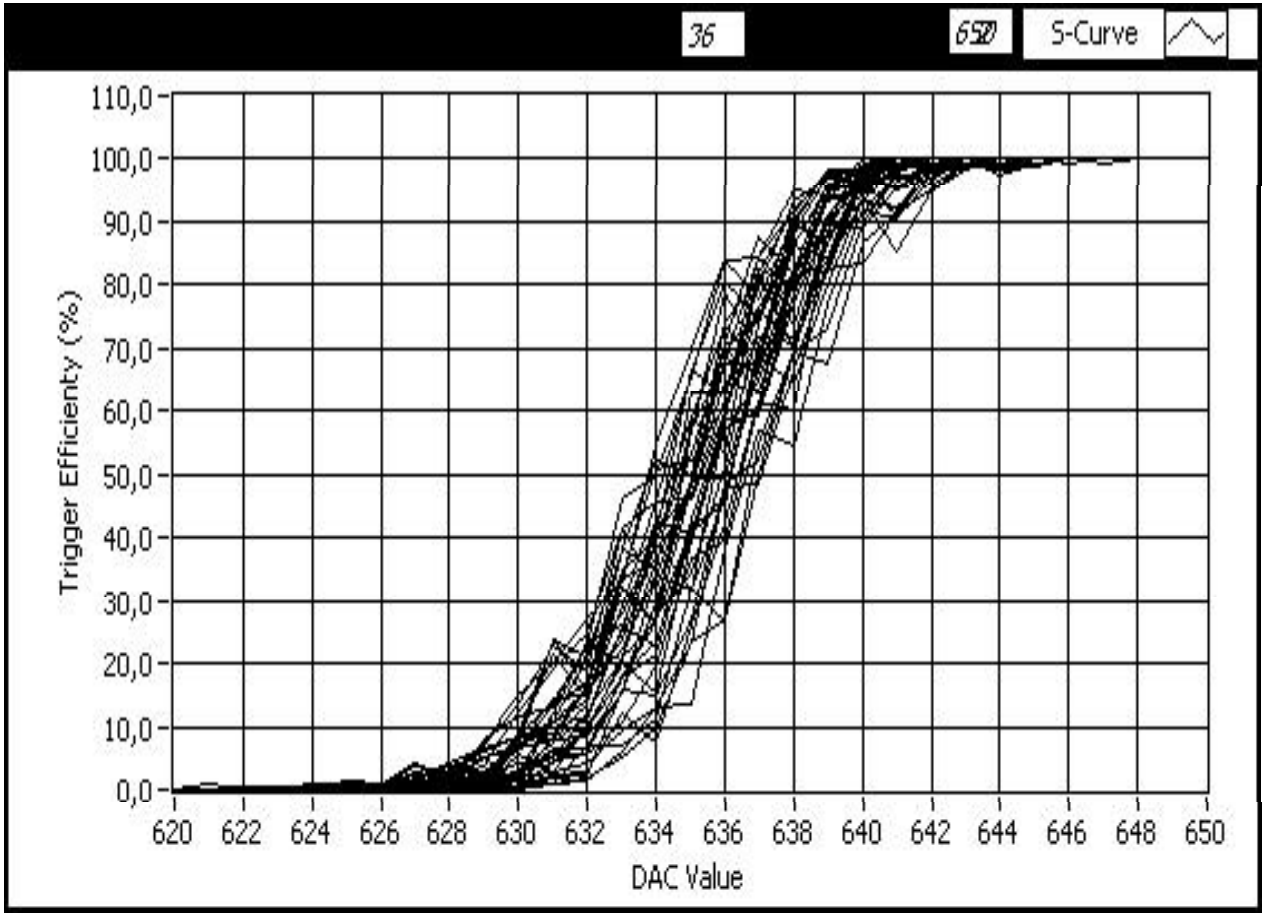
Noise correlation



Linearity with ADC



First S-curves

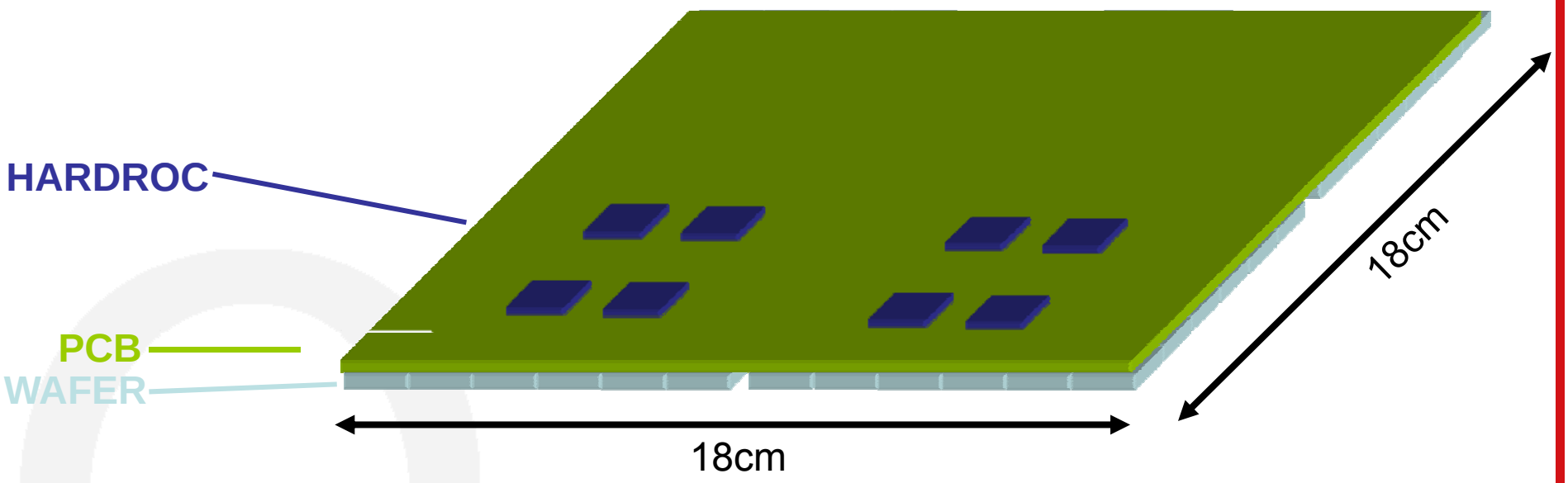


PCB design
FEV 5 presentation

Characteristics of FEV5

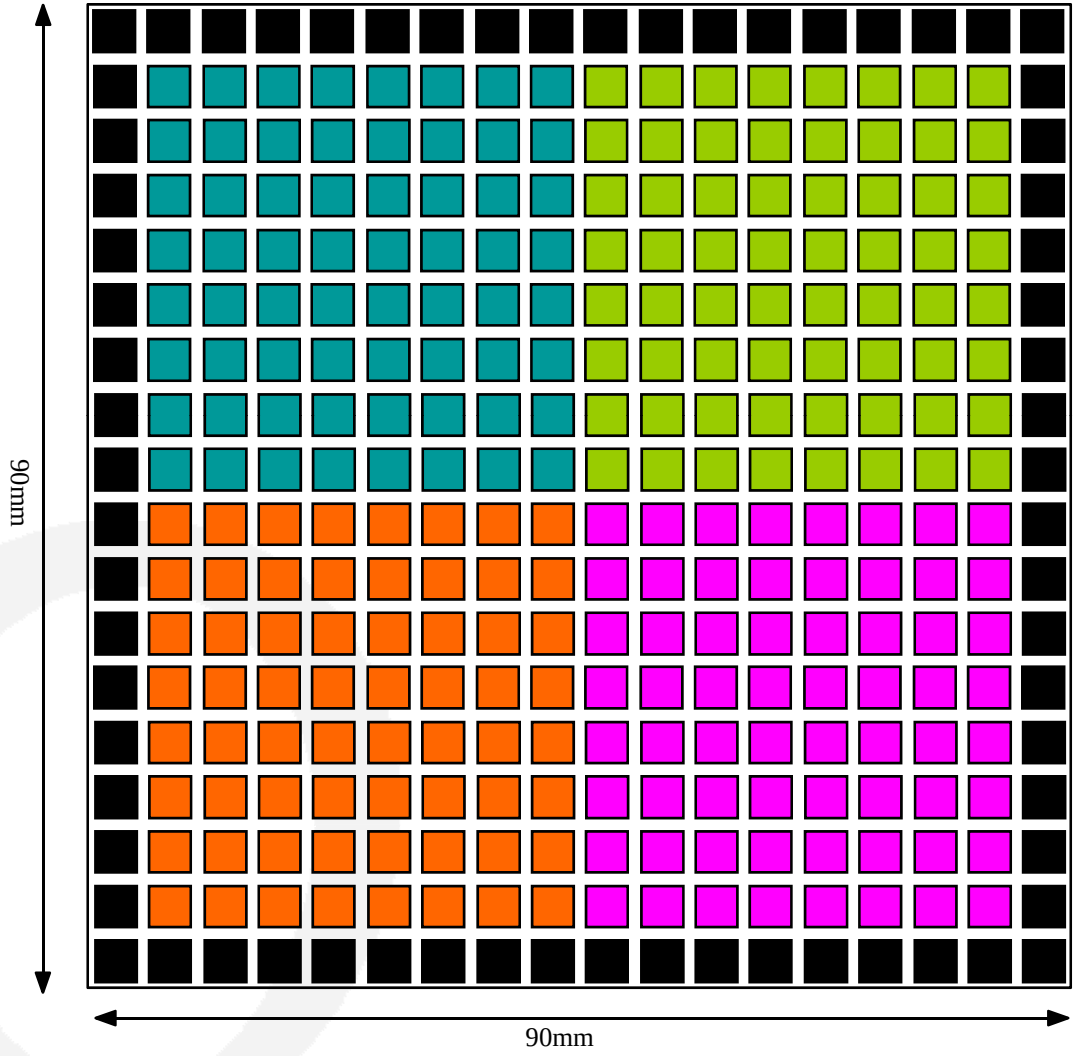
- Designed for :
  - 6-inch wafers (4 wafers of 9*9cm)
  - 0.5*0.5cm² pads → 324 pads/wafer → 1296 channels/PCB
  - Only 512 equipped with 8 Hardroc Chips
- New stitching :
  - No step, solder pins on top layer
  - Exact solder procedure to be defined (Patrick, Maurice, etc.)
- In fab : expected end of January

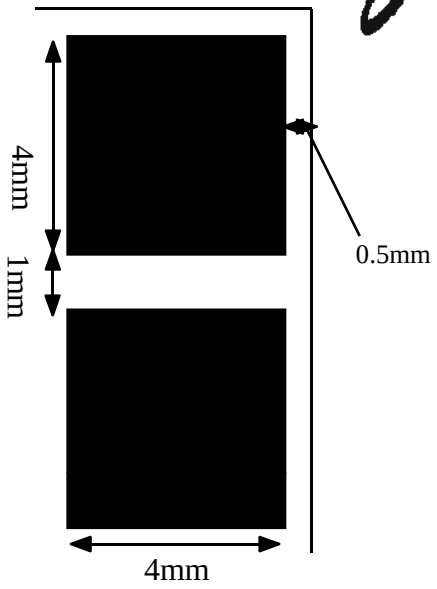
FEV5 : designed



1296 channels. 8 HARDROC (512 channels equipped)

Wafer : channel equipped





Chip 1

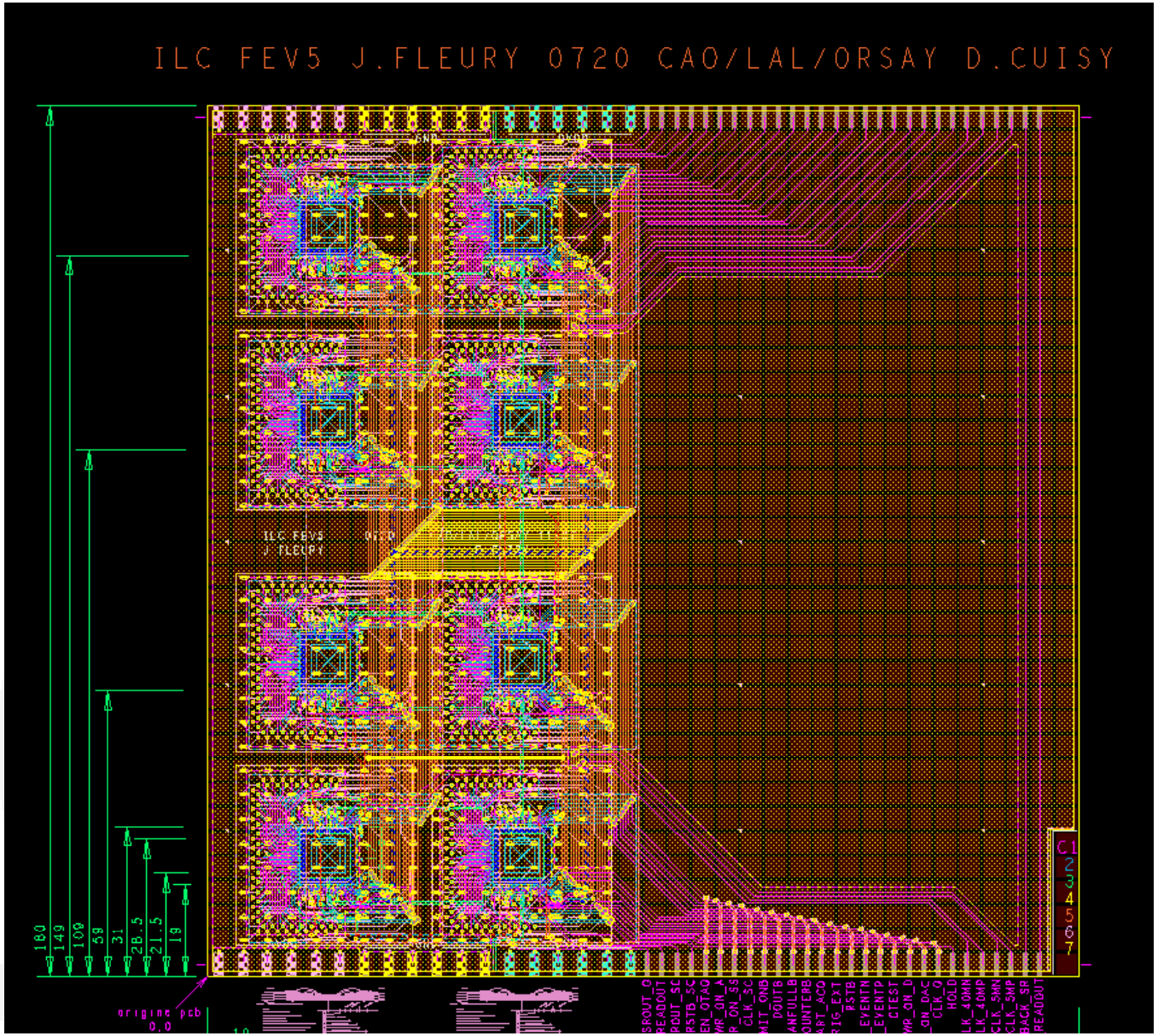
Chip 2

Chip 3

Chip 4

NC

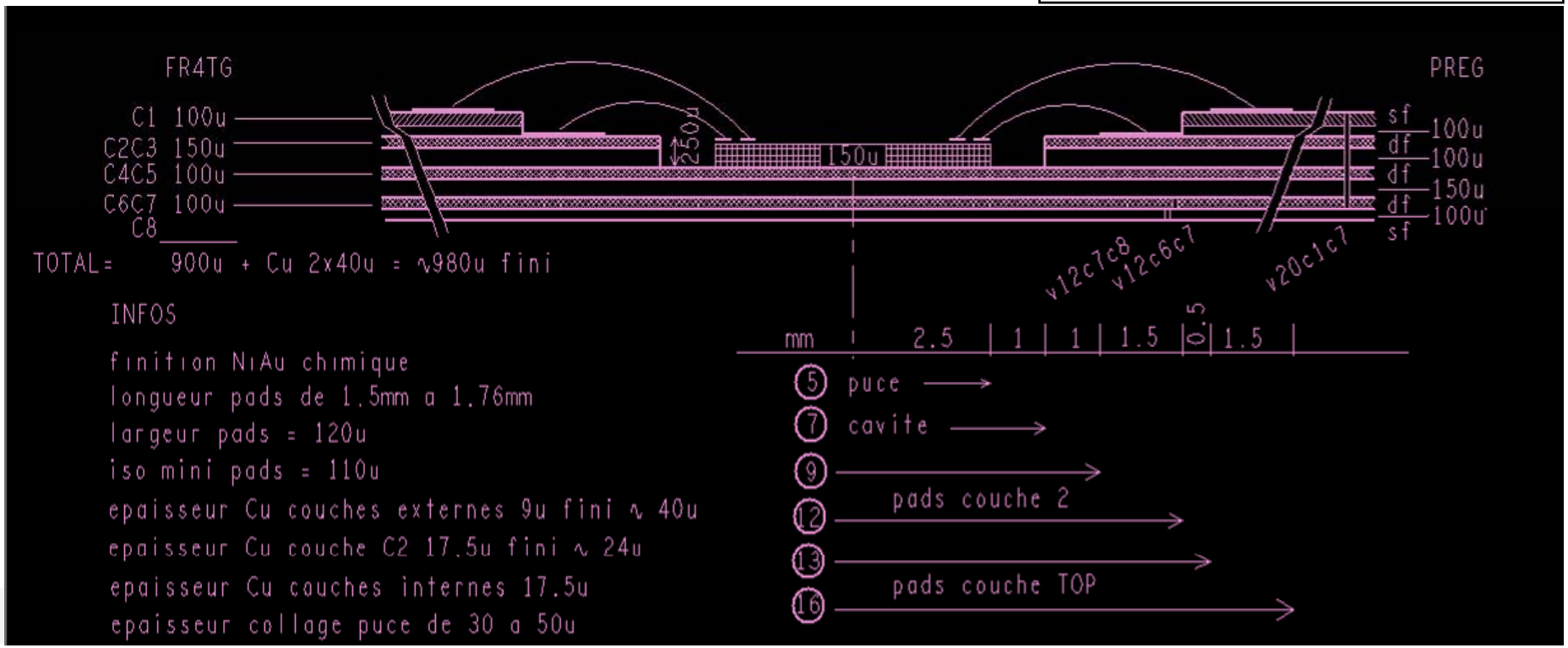
Layout : general



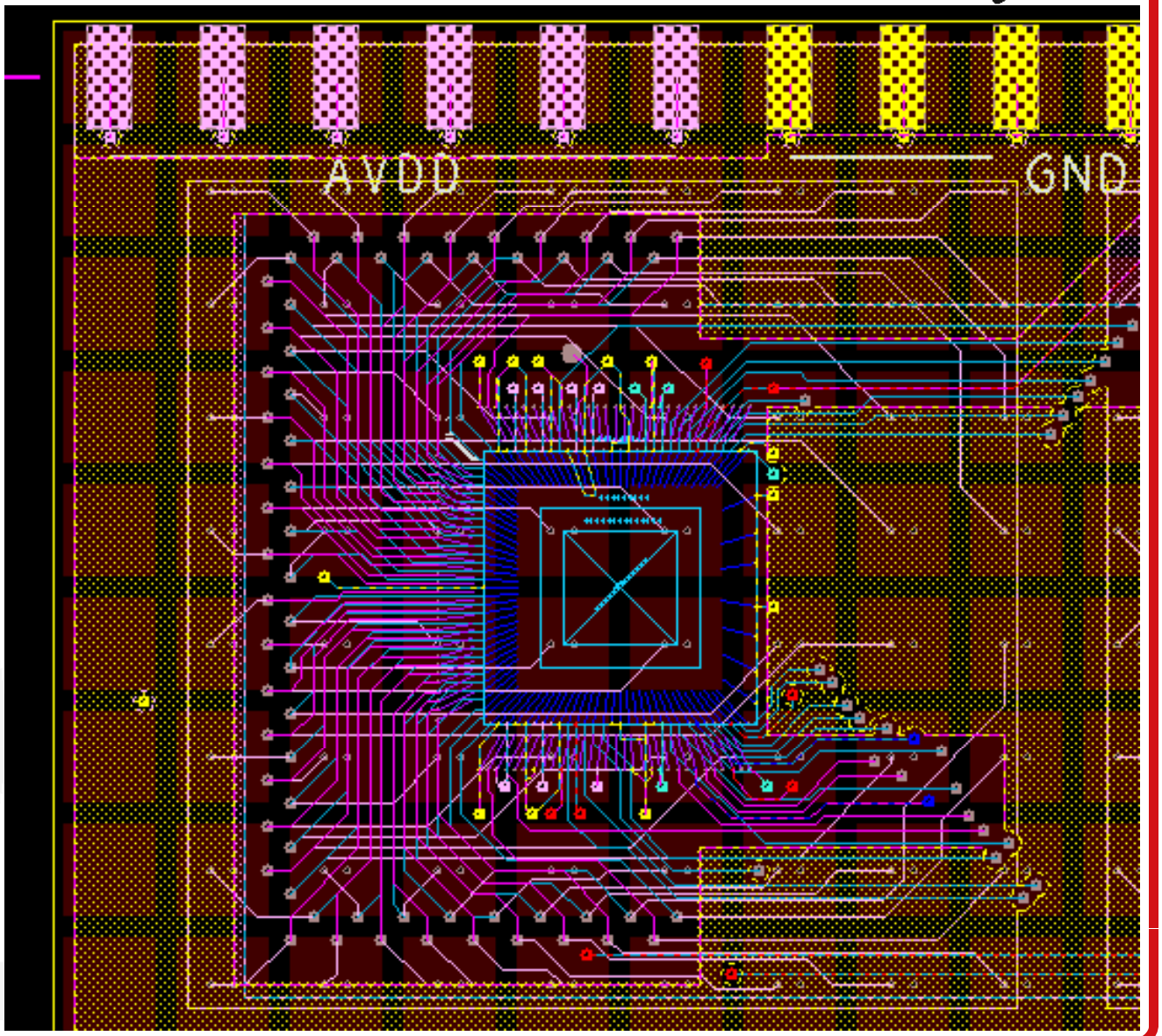
Chip Embedding + PCB Pile-up

Pile-up	
TOP	GND+routing
C2	AVDD+routing
C3	AVDD+DVDD
C4	GND + horizontal routing
C5	AVDD+ vertical routing
C6	GND+pads routing
C7	GND (pads shielding)
BOT	PADS

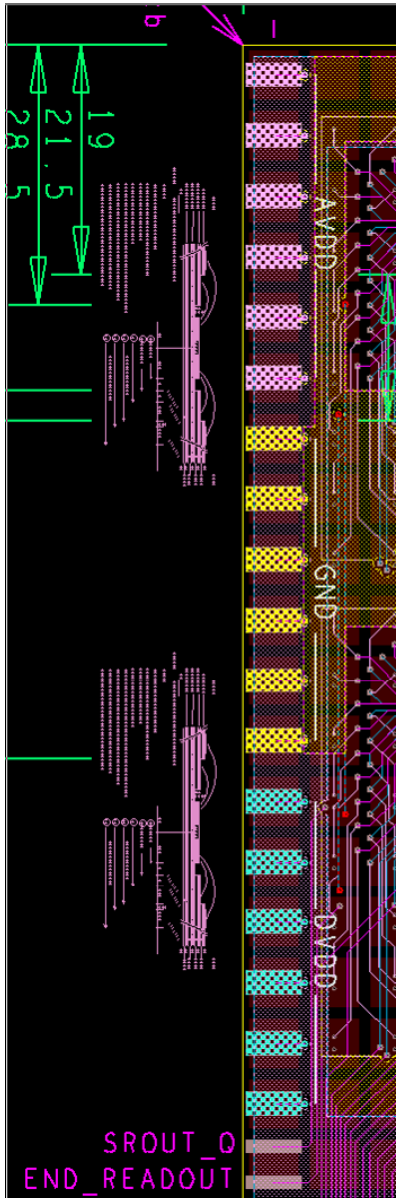
3 drilling sequences :
- Laser C7-C8 120µ filled
- Laser C6-C7 120µ
- Mechanical C1-C7

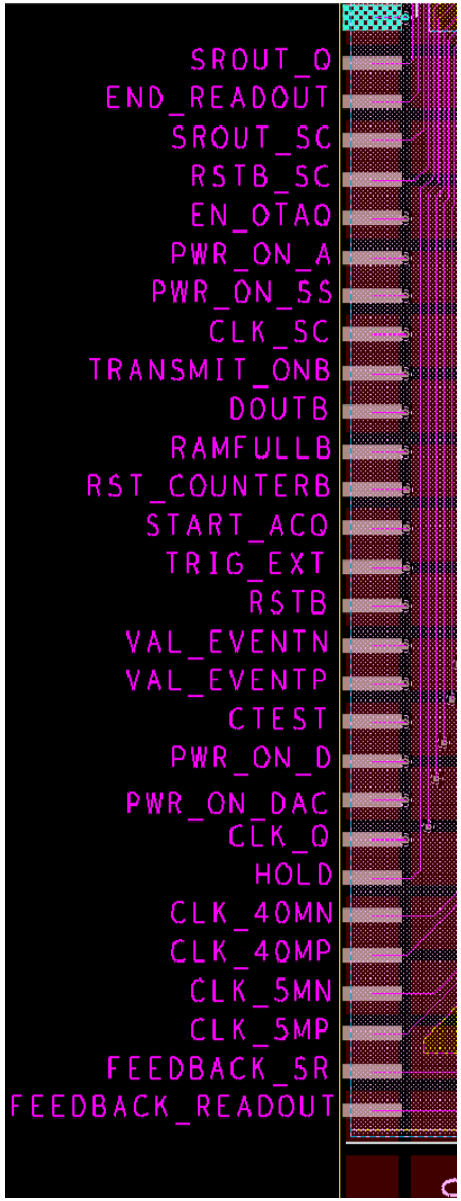


Pads tu Hardroc connection



I / O list


19
21.5
28.5
AVDD
GND
DVDD
SROUT_O
END_READOUT


SROUT_O
END_READOUT
SROUT_SC
RSTB_SC
EN_OTAQ
PWR_ON_A
PWR_ON_SS
CLK_SC
TRANSMIT_ONB
DOUTB
RAMFULLB
RST_COUNTERB
START_ACQ
TRIG_EXT
RSTB
VAL_EVENTN
VAL_EVENTP
CTEST
PWR_ON_D
PWR_ON_DAC
CLK_Q
HOLD
CLK_40MN
CLK_40MP
CLK_5MN
CLK_5MP
FEEDBACK_SR
FEEDBACK_READOUT

Conclusion

- PCB design
  - FEV5 engineering done
  - NOT SO EASY TO BUILD → 4 months delayed !
  - Need a DIF to connect and test
    - No way to test without a DIF
    - First 8-hardroc chain
  - Opportunity to have 256 ch. Wafers (5.5mm pads)
  - FEV6 designed and produced (mechanical and gluing test)
  - FEV7 to be designed this summer (Hamamatsu wafer test)
- SKIROC measurement
  - First backup ADC measurement showing encouraging results
  - Digital operationnal, SCA management working fine
  - Some more measurement
    - Self trigger to be characterized
    - Improve a bit MIP/noise ratio on charge meas. path