IN2P3

Omega

LAL LPNO

Status of SPIROC

Michel Bouchel, Stéphane Callier, Frédéric Dulucq, Julien Fleury, Gisèle Martin-Chassard, Christophe de La Taille, Ludovic Raux

lundi 2 juin 2008

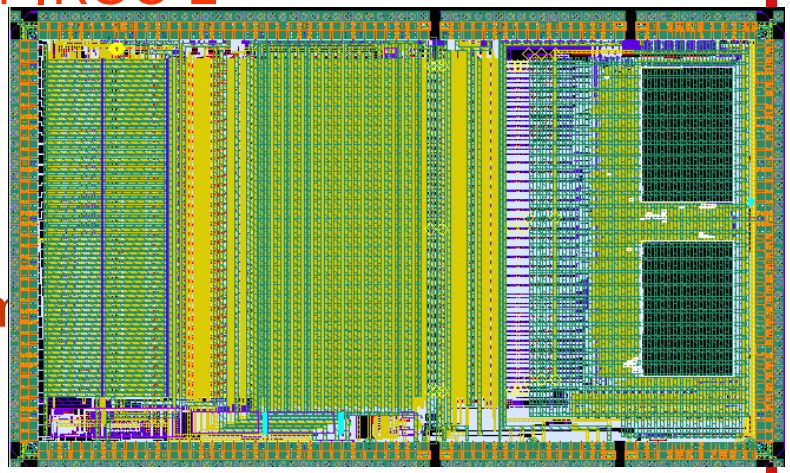
Orsay MicroElectronic Group Associated

SPIROC 2

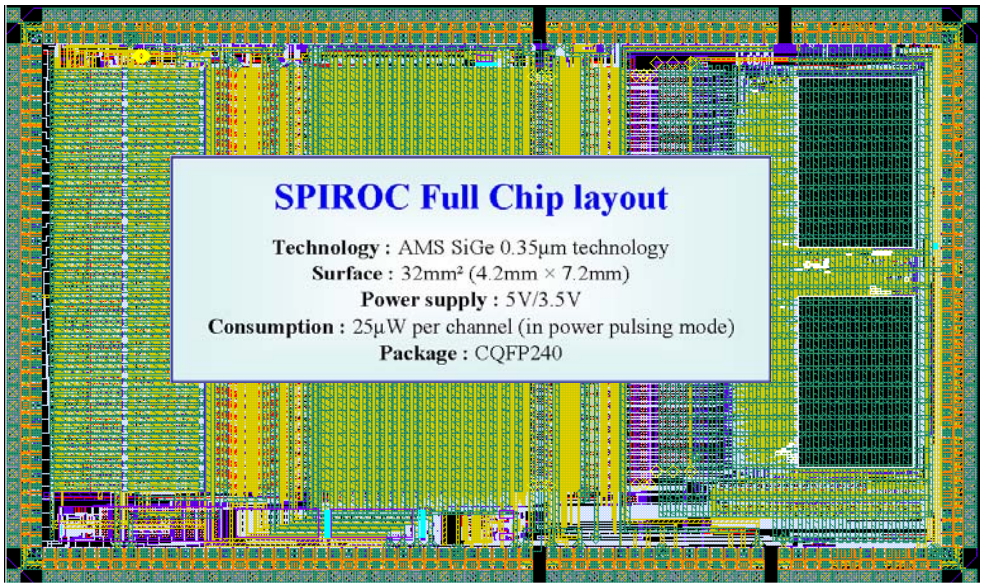
- Status of SPIROC1
  - 2 major bugs which need to be corrected : probe, ADC
  - Analog part so far OK, can be used to replace FLC_SiPM
  - Autotrigger at ~50-100 fC
  - Could be tested with existing detector and DAQ
  - Possibly SKIROC compatible
  - Many more measurements to be done : complex chip

A second iteration is necessary : SPIROC 2

- SPIROC2 could be prototyped
  - If no major change
  - TQFP208 package : 28x28x1.4 m



SPIROC 2



SPIROC 2 Layout in progress

submitted on 9th june 2008

Delivery expected in September-october 2008

Very conservative prototype which corrects the bugs of the first version and adds light modifications

SPIROC 2 : High priority modifications

1. Slow control and probe register to fix (ok)
   - « Data » and « clock » signals to repair to have good timing

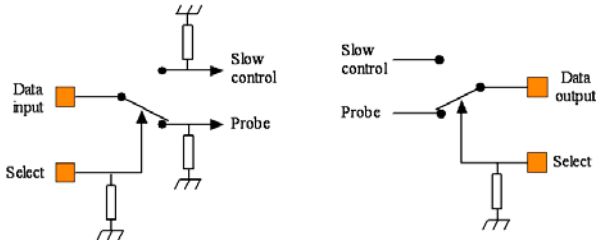
2. Wilkinson ADC to modify (ok)
   - ADC Discrimitors to invert
   - Ramp generator to change

3. TDC bug to fix (ok)
   - Voltage reference value to change

SPIROC 2 : intermediate priority modifications

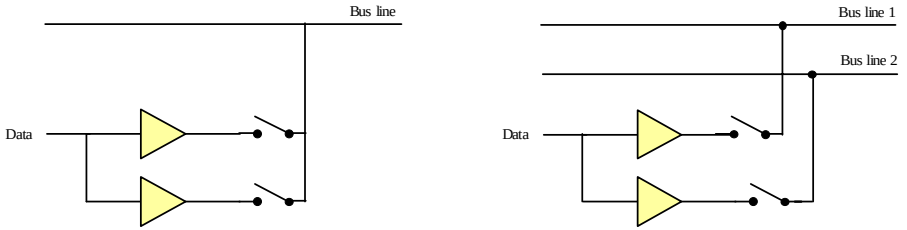
1. Probe on the 16 « read » signals (ok)

2. Dual 10-bit DAC
   - Resistance values to correct (ok)
   - DAC current to stabilize with temperature



3. Bandgap
   - Extinction in idle mode to fix (ok)
   - Performance improvement (ok)

4. 8-bit DAC
   - Extinction to fix (ok)
   - Bias resistance value to correct (ok)

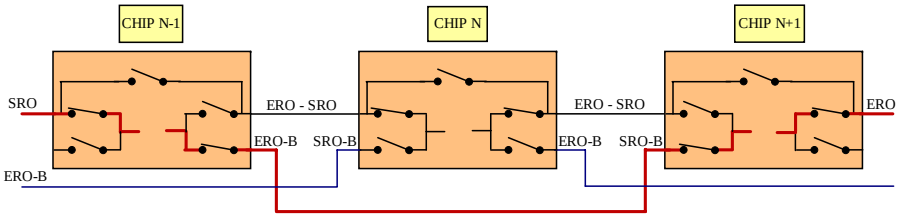


5. LVDS receivers (ok)
   - Extinction in idle mode to fix

6. Open collectors to improve to have better reliability (ok) (cf 2nd schematic)
   - Open collectors to double
   - Open collectors transistor width to increase

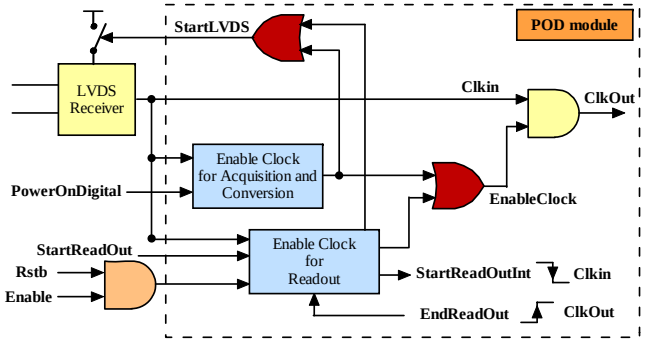
7. « Probe » and « slow control » registers to multiplex (ok)(cf 1st schematic)

8. Add bypass for these 2 signals (SRO, ERO ➔ SRO-B, ERO-B) (ok) (cf 3rd schematic)



SPIROC 2 : Low priority modifications

1. Power pulsing signal management (in progress)
   - POD module inserted for the 2 clock (5 and 40HHz) LVDS receivers (see talk F.Dulucq)



- Slow control
  - Default parameters to implement (ok, only in digital part)
  - Improve shift registers daisy chain between ASICs: (ok)
    - Add opposite edge Flip-Flop at the end of shift registers

1. Discriminator 4-bits DAC :
   - Accuracy to extend to 8 bits

2. Input 8-bit DAC
   - Precision to extend to 10 bits

3. Compatibility with a 0-2.5V power supply on digital part to have less power consumption

4. CRRC² slow shapers :
   - Resistances to decrease to have less second stage noise

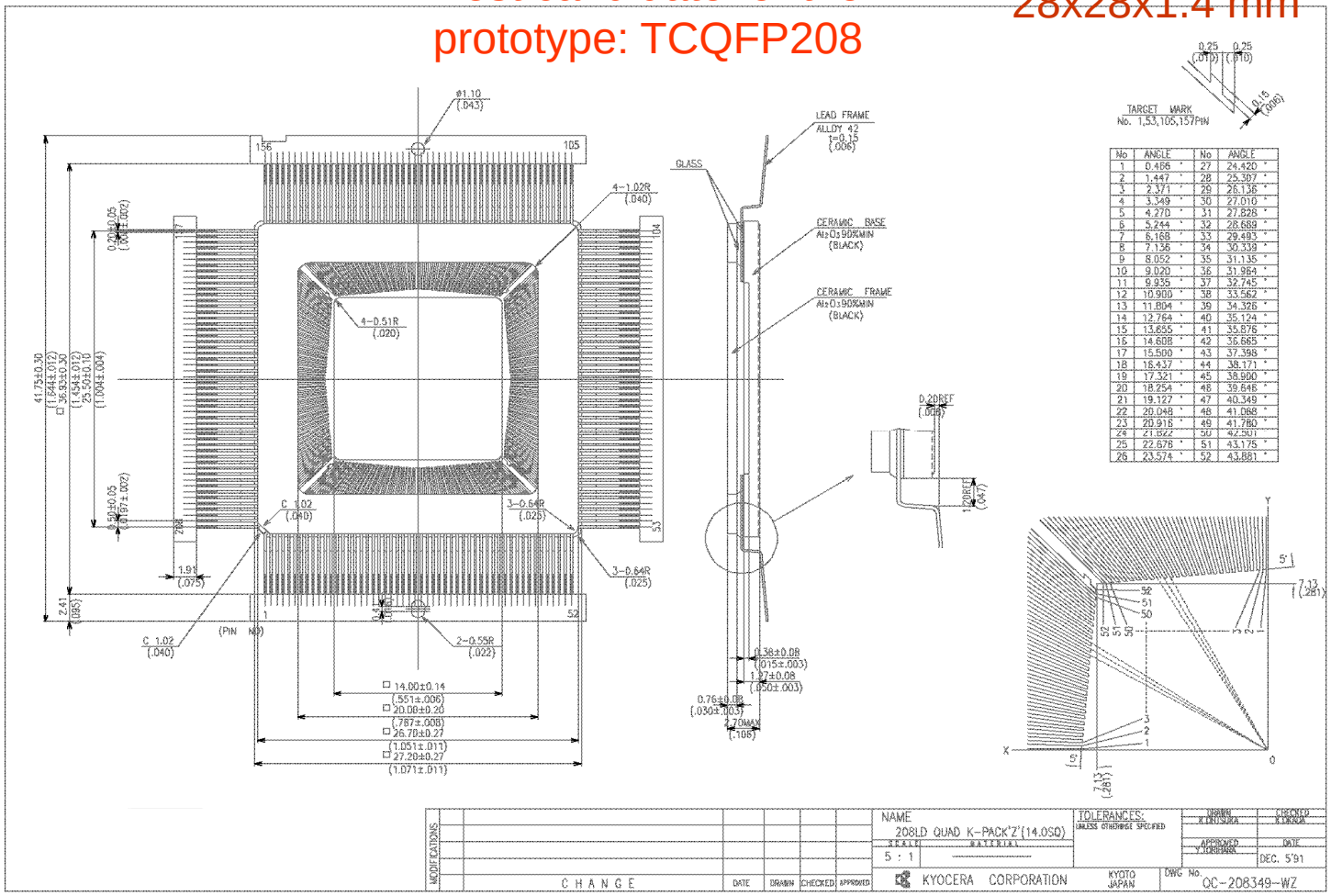
5. Dual 10-bit DAC
   - DAC current to stabilize with temperature

6. TDC:
   - Ramp current to stabilize with temperature

206 pads to connect

Best candidate for the prototype: TCQFP208

Dimensions: 28x28x1.4 mm



Conclusion

- Status of SPIROC1
  - 2 major bugs which need to be corrected : probe, ADC
  - Analog part so far OK
  - Autotrigger at ~50-100 fC
  - Could be tested with existing detector and DAQ
  - Many more measurements to be done : complex chip
  - SPIROC 1 needs one more prototype before production
- SPIROC 2 layout chip in progress
  - Very conservative prototype
  - Correction of the first version bugs
  - Add some light improvements (in digital part)
  - Packaging: TQFP 208