EUDET module – Status AHCAL

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for the AHCAL developers
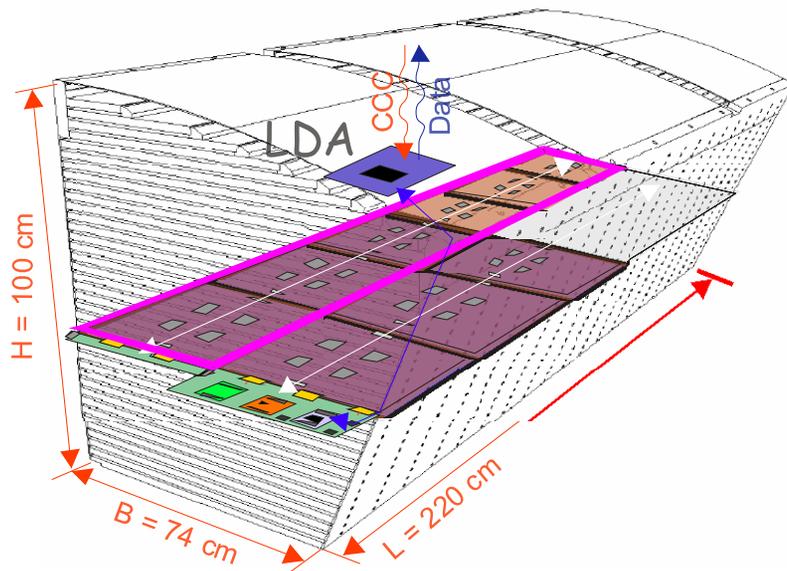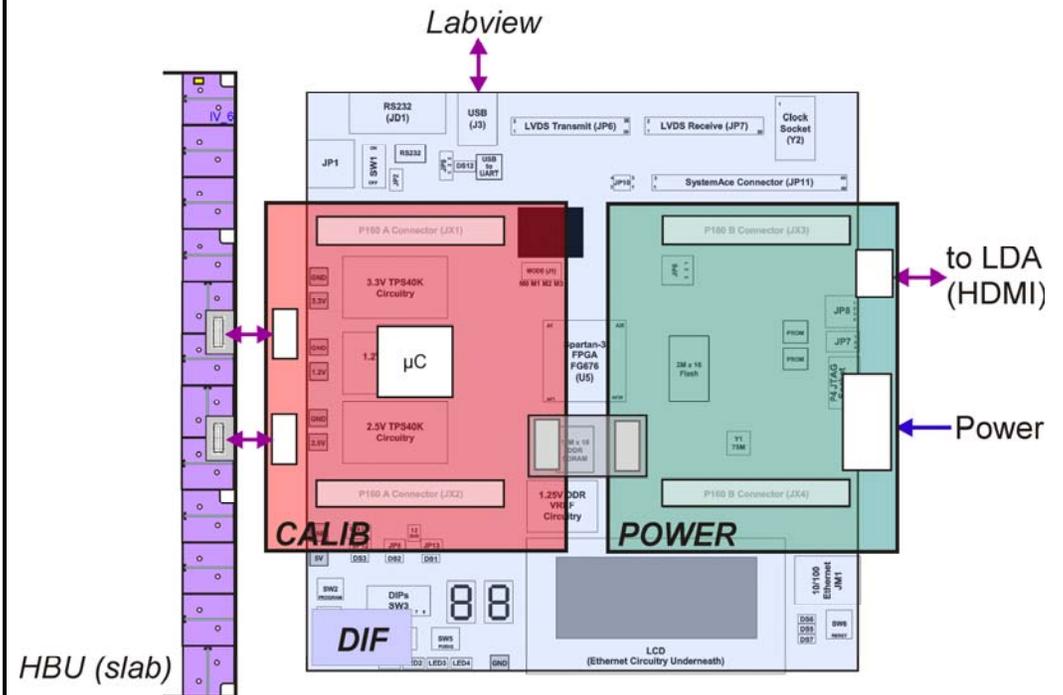
DESY

FE

Maybe the future …

1st EUDET Prototype (**1st step**)

Commercial DIF, new mezzan. (CALIB, POWER), 1HBU (later: 6)

Prototype Tile for HBU0

(30;30)

SiPM
(0;15)

Mirror

(0;0)

(mm;mm)   WLS

Alignment Pins
(22.5;7.5)
(7.5;22.5)

Mechanics Tile for HBU0
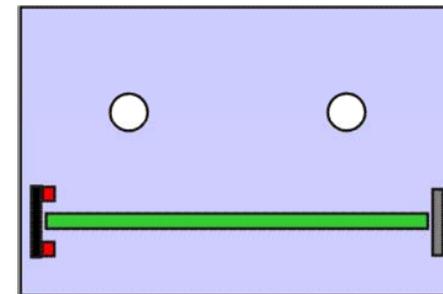
Cutout (~8mm) for
cassette construction
(done by „drilling")
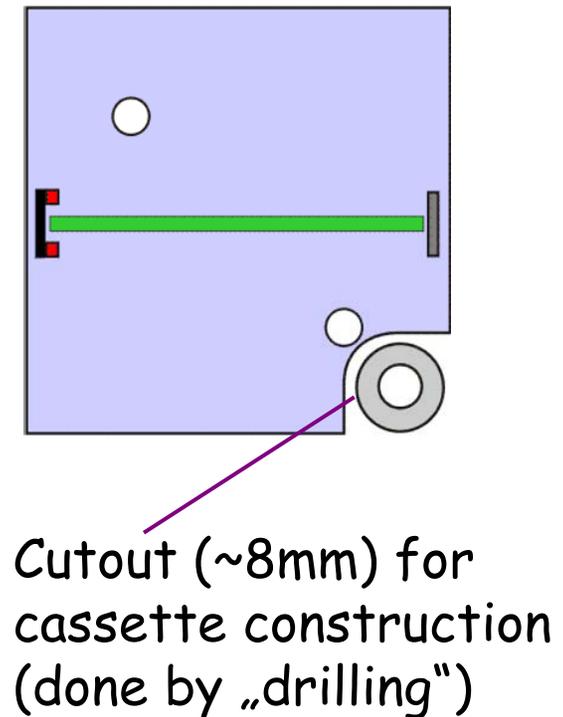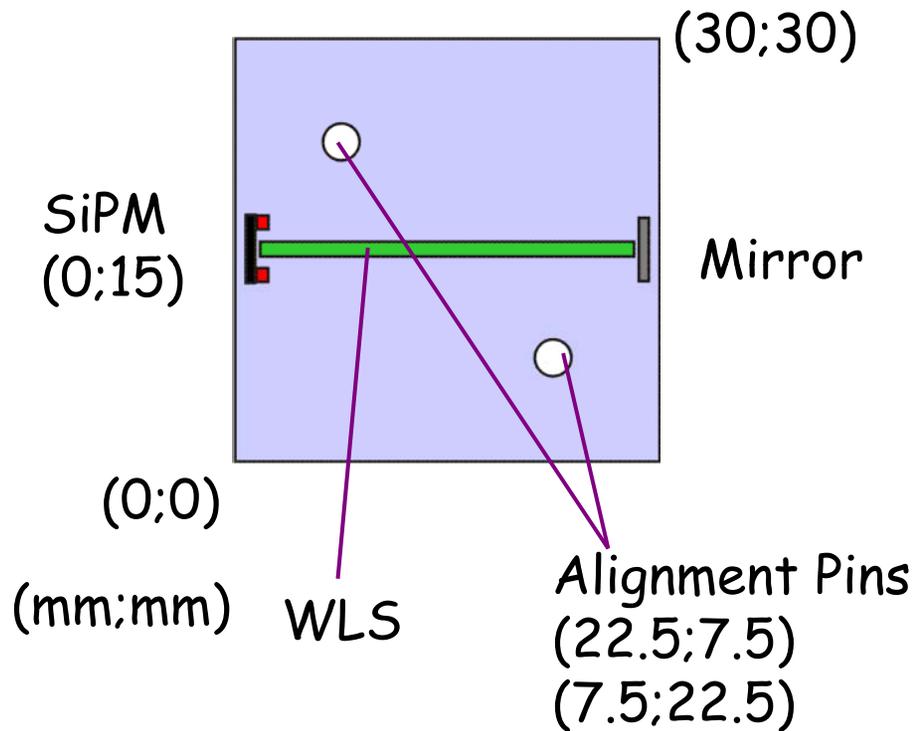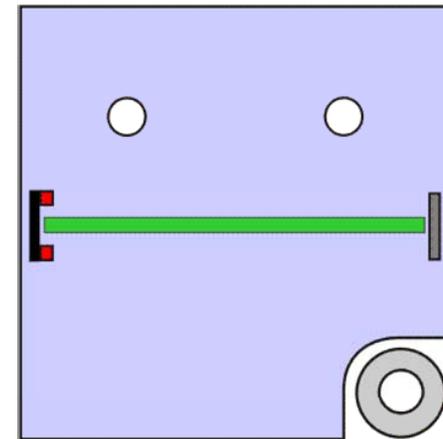
100-150 prototype tiles (structures machined, not moulded)
expected end of June.

Tiles for EUDET module

Standard Tile (moulded)

SiPM
(0;15)

(30;30)

Mirror

(0;0)

(mm;mm)   WLS

Alignment Pins
(7.5;22.5)
(22.5;22.5)
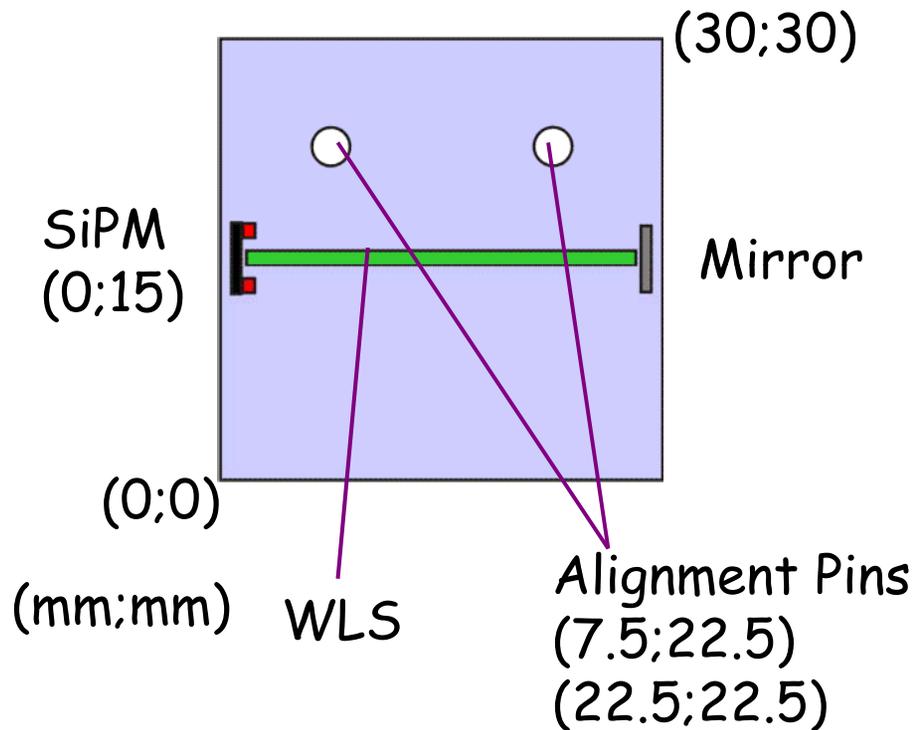
Shorted (by 1cm) tile
for inter-layer sizes

Time schedule for moulded tiles not completely
clear (end of 2008?).

HBU – SPIROC assembly

SPIROC on HBU PCB cannot be placed above SiPM and
alignment pins of the tiles (=> Tile grouping)

next tile geometry   HBU0, tile prototypes

SPIROC2 package
(3 x 3 cm²)
in PCB cutout
(5mm surrounding)

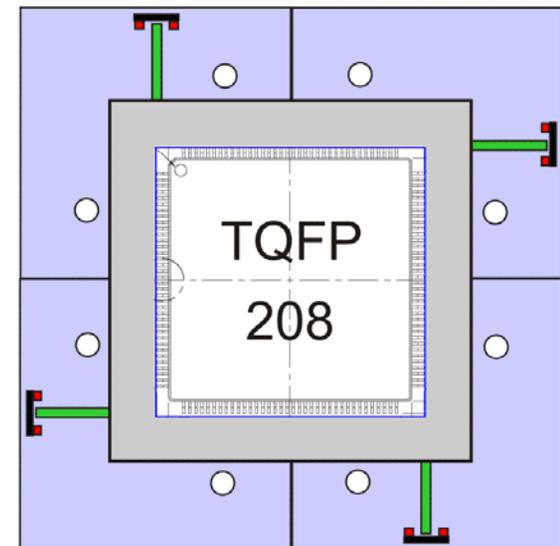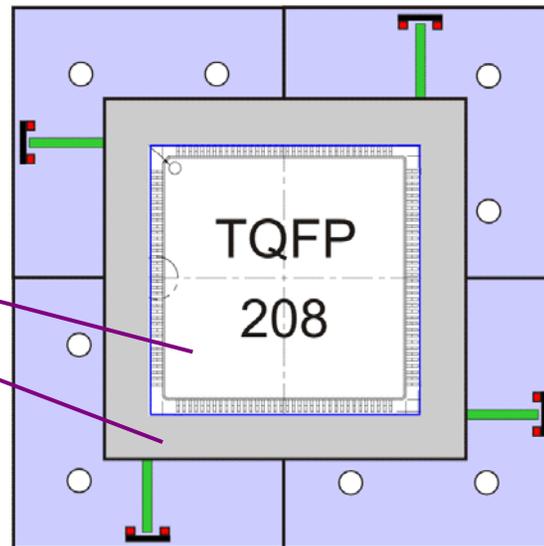Cassette fixation

Mechanics Tile

Temp. Sensor

SPIROC1

Debug Conn.

Signal IN

Flexlead Conn.

Power IN

Two signal paths

SPIROC2

Prototype Tile

Calibration Electr.
(LED + Charge Inj)

Flexlead

14.50

1.20

5.50

0.5

in mm,
not in scale
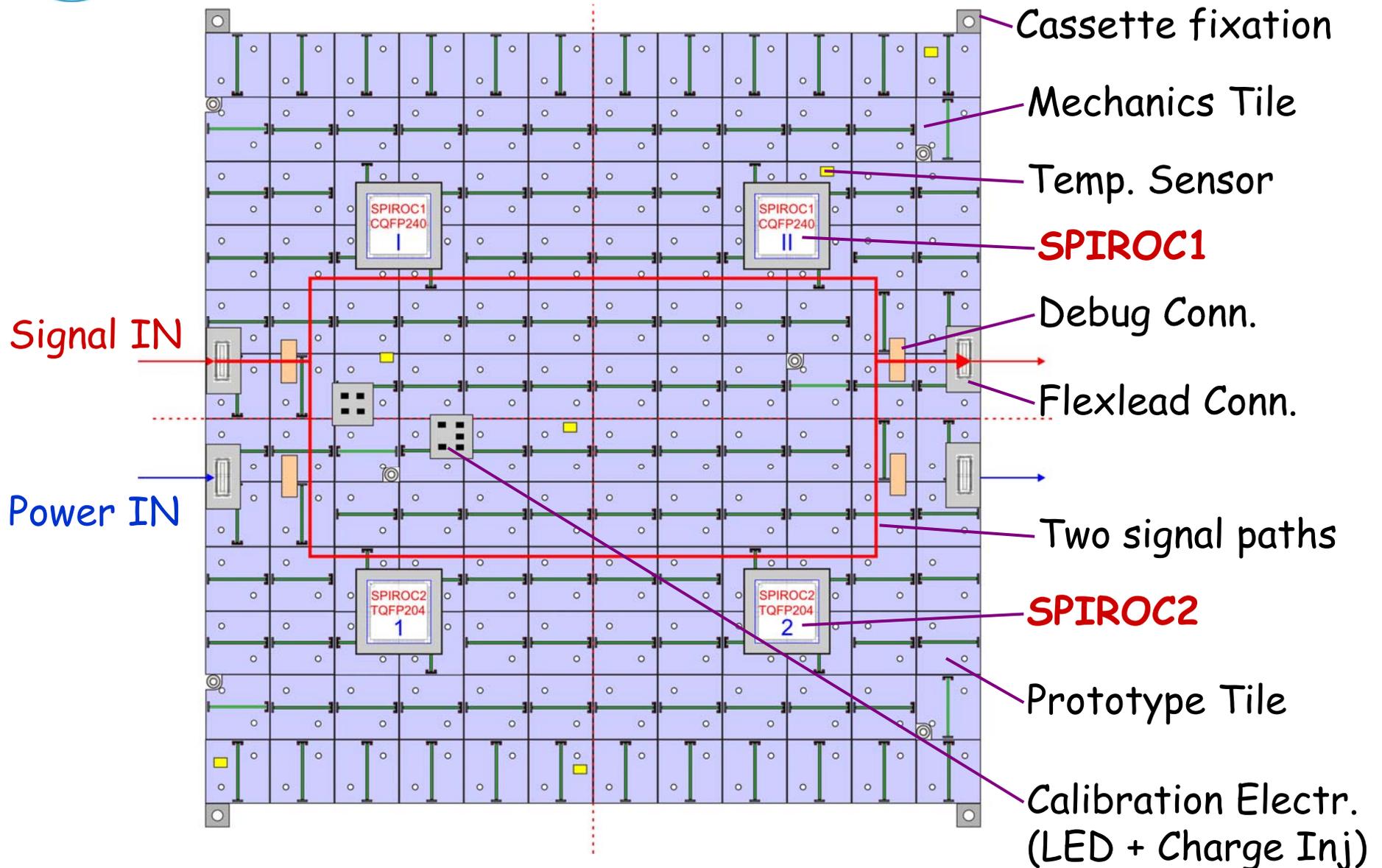
Rigid, 40-pin conn. prototype
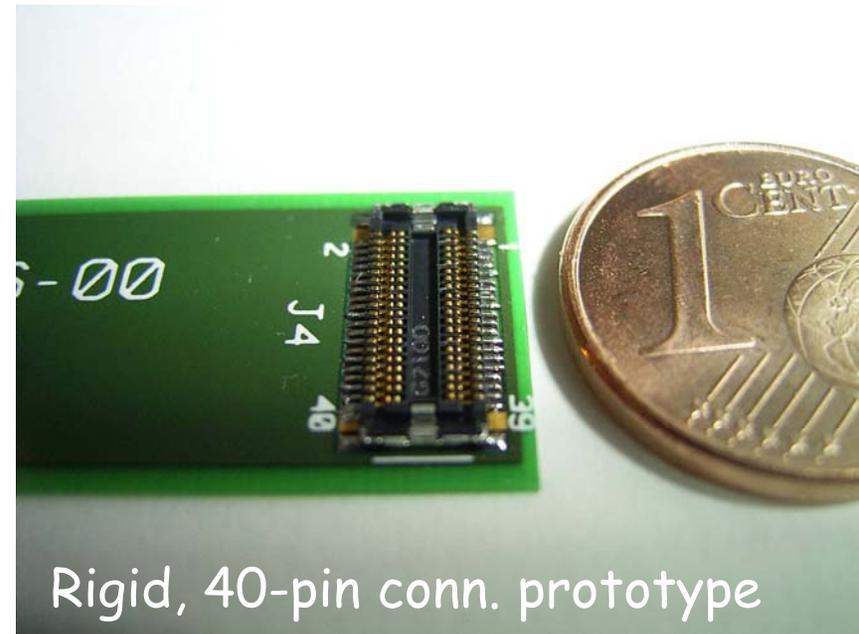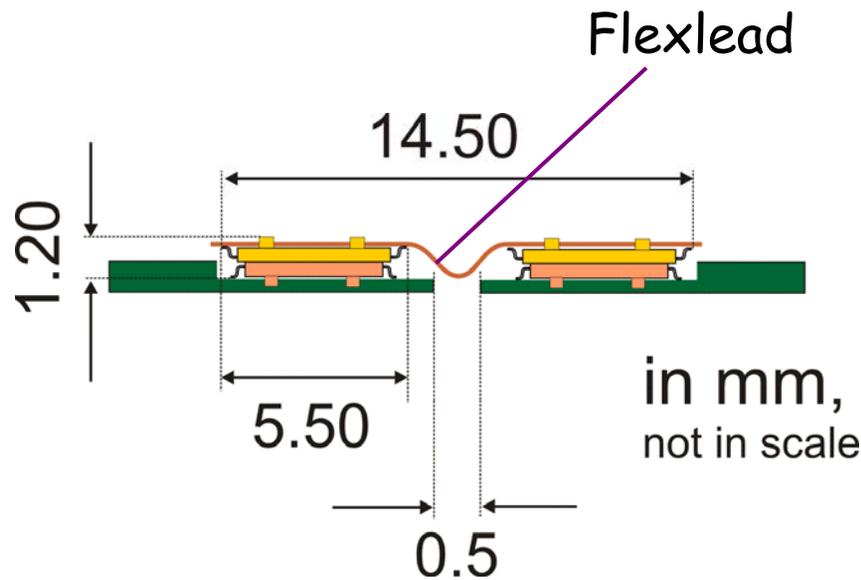
Flexlead: Rigid below connectors, 4 layers,
flexible (polyimide) in between, 2 layers
80-pin connectors

Bended flexlead allows HBU-HBU displacement of ±100μm.
Concern: Bending forces (tension) might disconnect one connector.
Expected cost relation flexlead/connector: ~1.5
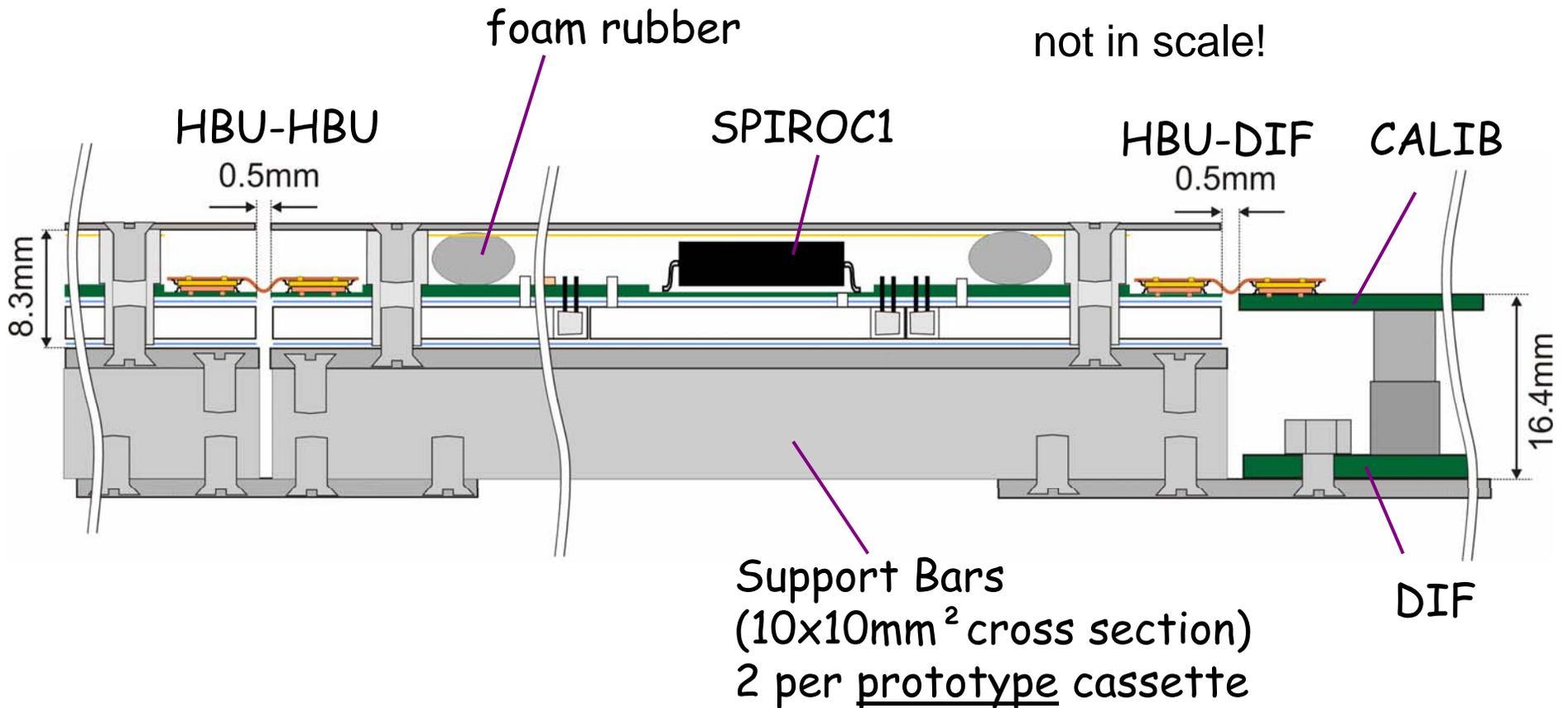
foam rubber

not in scale!

HBU-HBU   SPIROC1   HBU-DIF   CALIB

0.5mm   0.5mm

8.3mm   16.4mm

Support Bars
(10x10mm² cross section)
2 per prototype cassette

DIF

Bended flexlead allows HBU-HBU displacement of ±100µm.

Detector electronics (Load) is switched between „off" (no current) and „on" (full current) with 1% duty cycle.
=> Oscillations on 2.20m-long power-ground system?

Test Setup 1
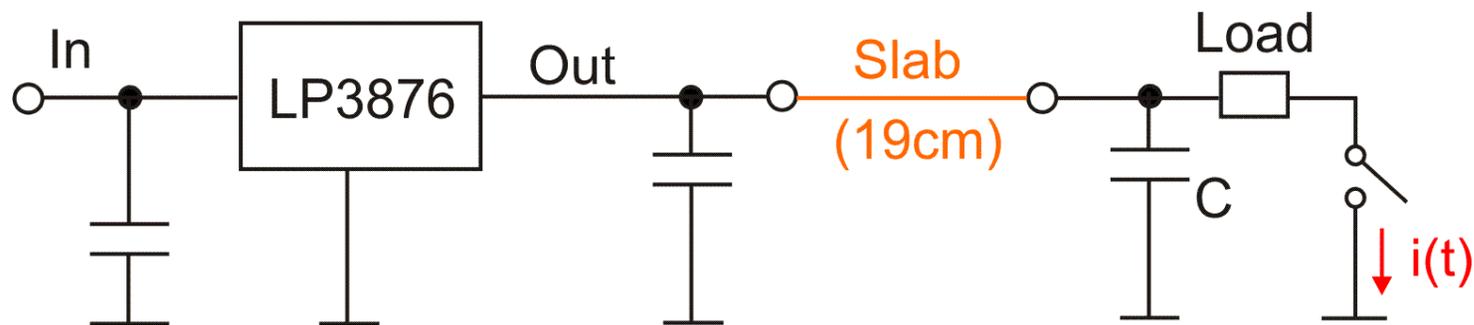
Test Setup 2 (input)

Tested:

Switched Current: 0.7...3A
Load Block Caps   : 0...10μF

Settling Time / Overshoot = ??

Test Setup
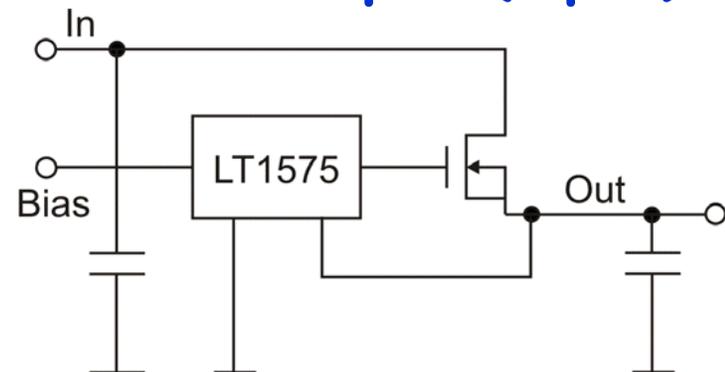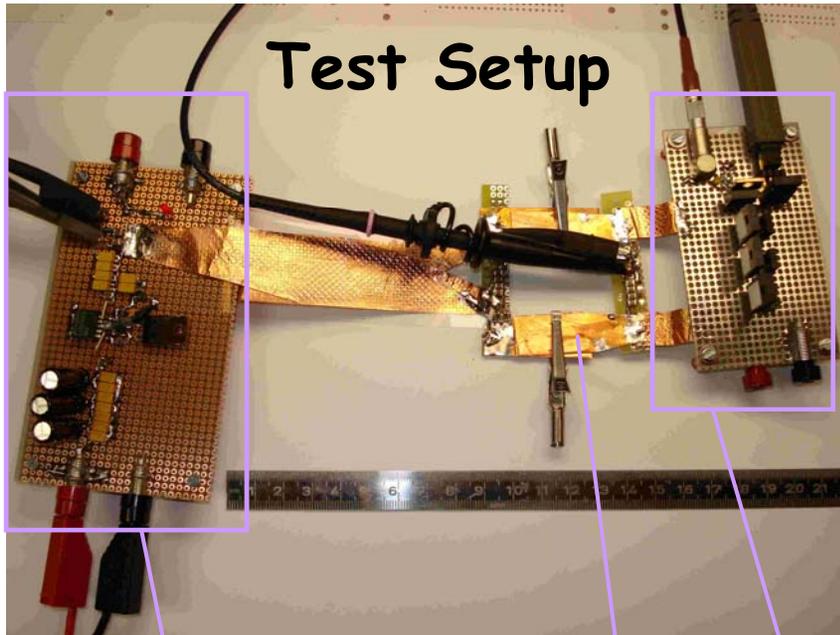
<u>Settling time (Load side):</u>
Voltage within 50mV of final value.
Aim: reasonable values for efficient power cycling (< 50µs)

<u>Overshoot</u> shown here for switch-off case (worst-case).
Aim: Protection of devices, stable register settings.
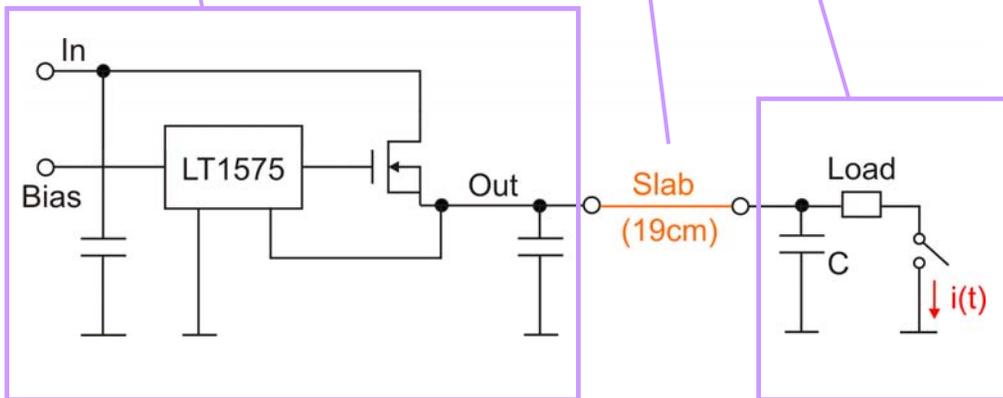
Later: Stability test for 2.20m slabs

Typical results for overshoot (loadside), similar for both setups.
Overshoot on regulator side: <150mV.
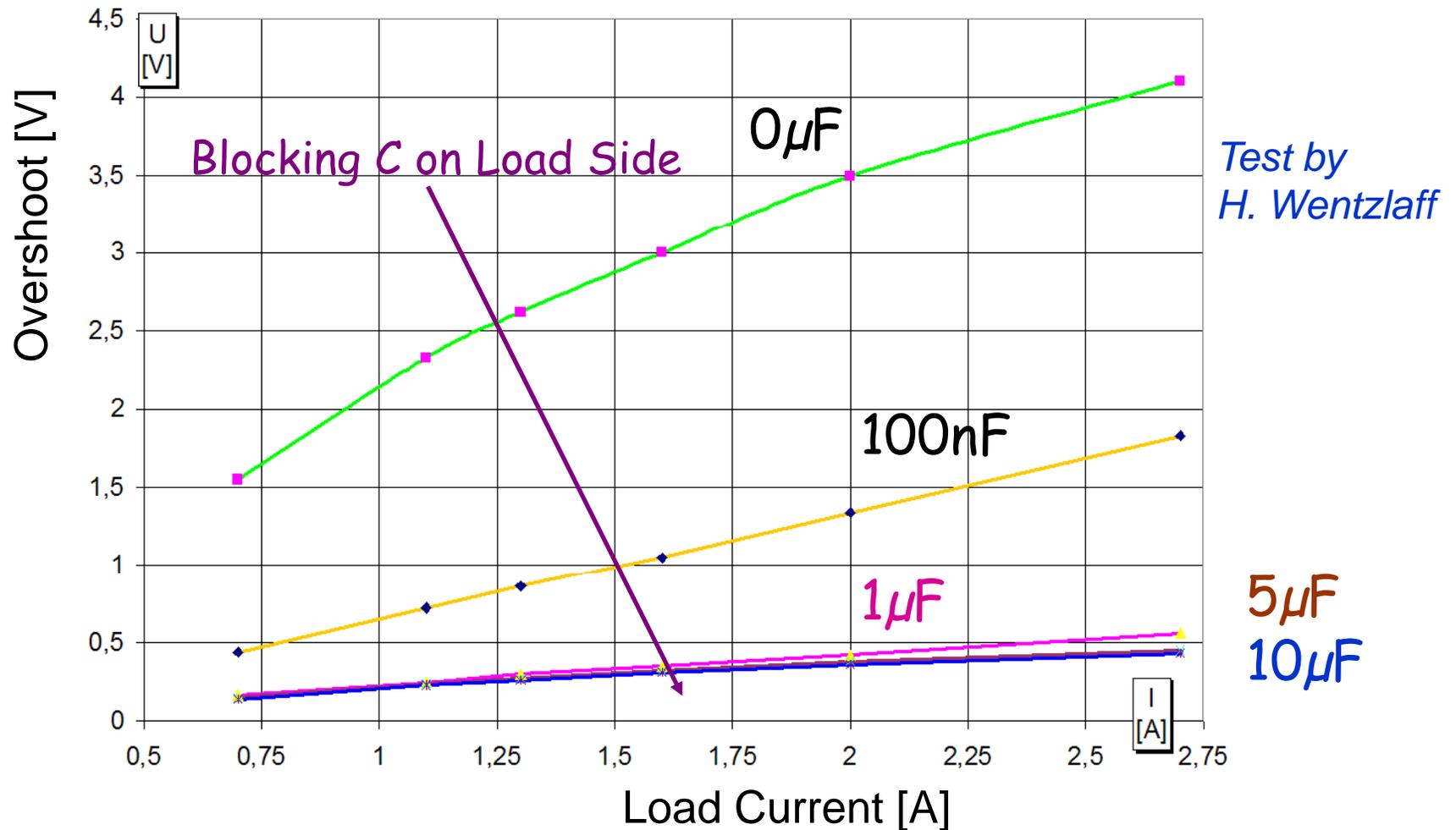
FE

Typical results for settling time (loadside), setup 1 (LP3876)

Settling to <50mV

10μF
5μF

Test by
H. Wentzlaff

Blocking C on Load Side

100nF

1μF

0μF
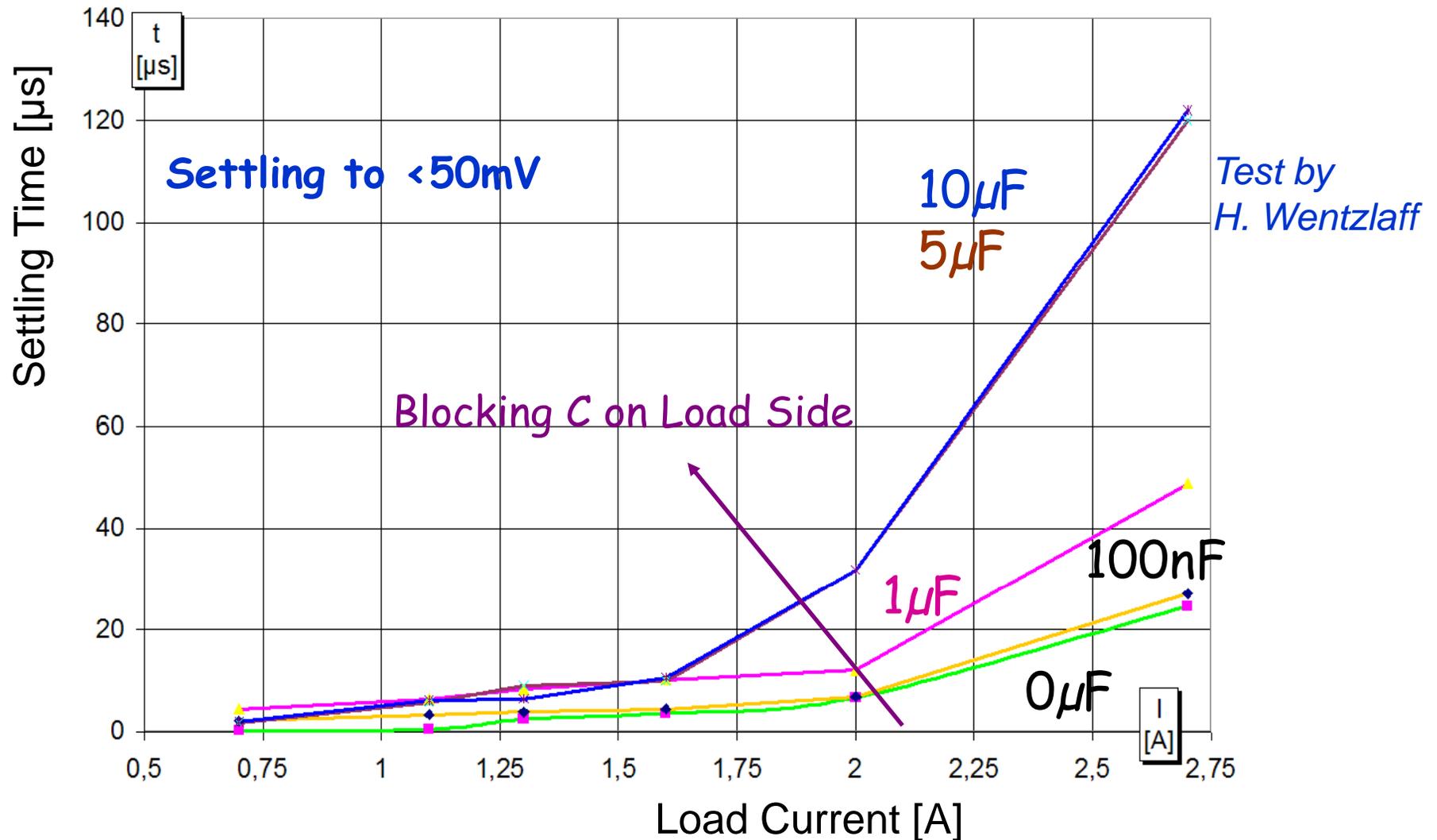
Typical results for settling time (loadside), setup 2 (LT1575)
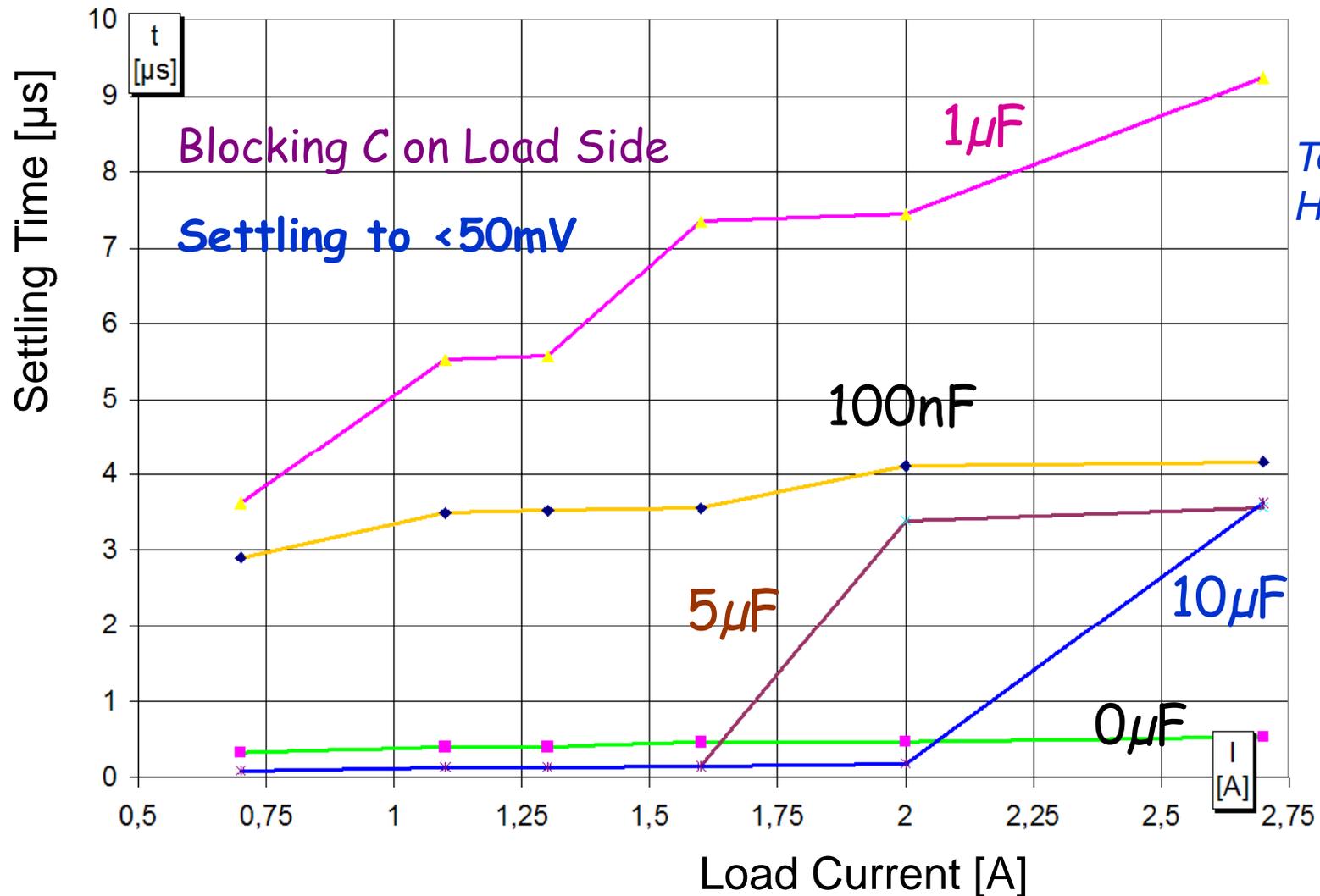
Overshoot, settling-time good on regulator side.

Setup 2 (with transistor): better settling time (factor 10),
in the order of 5..10μs.

Overshoot is still about 0.2-0.5V (~150ns spikes) for large blocking
caps on load side. Trade-off settling time - overshoot.

Dependency on load-switch transition (5-10ns now)?

Influence of the 2.20m-long slab is analyzed now.

AHCAL - Status Modules

<u>DIF (AHCAL):</u>

-Two commercial FPGA boards have arrived.
-VHDL development should start now.
 => DIF common block implementation needs closer coordination.
    Maybe starting with the basics (=>timeline?)?:
    Fixing of timing specs for DIF-ASIC's communication,
    VHDL block architecture,
    clock speed of DIF FPGA,
    LDA-DIF data rate and frame size (or start with USB?).

<u>CALIB (LED system and charge-injection)</u>

-Module's duties fixed, schematic almost finished.
-Layout generation when we fix HBU interface (and design).
-Microcontroller programming starts now (SPI to DIF, LVDS)

POWER (supply of AHCAL electronics)

-Components and architecture fixed in principal, but:
-Regulator setup has to be checked for 2.20m slabs

HBU0 (defines timelines for all other parts)

-Schematic needs information about SPIROC2 and tiles.
-Initial setup only has 2 HBU0s (no full slab test).
-Prototype cassette design waiting (flexlead impl., tile size)
-SPIROC1 and SPIROC2 in independent signal chains.
-Latest results from Wuppertal LED and
  SPIROC digital part tests should go into design.

Timeline (Rev. 1)

FE AHCAL Timeline		2008							2009				
Month	Mar/Apr	May/June	July/Aug	Sept	Oct	Nov	Dec	Jan/Feb	Mar/Apr	May/June	July/Aug	Sept/Oct
Task						Milestone				Milestone		
Scint. Tiles												
Definition of architecture				Moulded Tiles			Dimensions					
Production												
SPIROC		SPIROC2		SPIROC3			Pinout					
Hcal Base Unit (HBU)												
Circuit Design/Layout												
PCB Production/Assembly												
Detector Interface (DIF)												
Common Block Firmware												
AHCAL Block Firmware												
Circuit Design/Layout												
PCB Production/Assembly												
CALIB, POWER												
Circuit Design/Layout												
PCB Production/Assembly												
System Tests												
DAQ Software, LDA												
Component Ordering												
Prototype												
EUDET Mod. (Final)	28.05.08											

Milestone shifted now by 1 month to Nov. 08.
Full slab not available before mid 2009.

DESY SPIROC1 tests

Tests and all the work done by **B. Lutz, R. Fabbri, Wei Shen**

DESY SPIROC1 tests

from B. Lutz

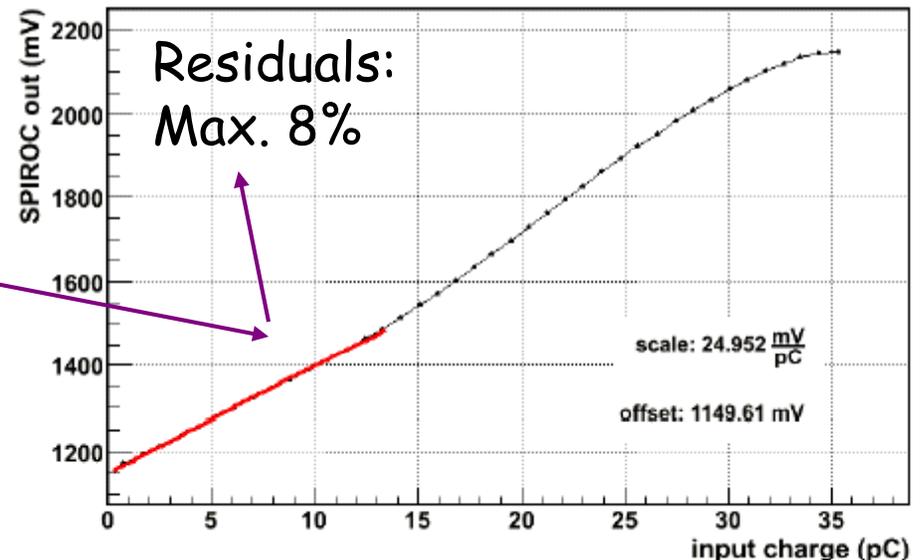SPIROC HG 1000fF 50ns hold: 80ns

<u>Linearity tests (charge injection)</u>

- -Hold <u>fixed</u> for full dynamic range. => non-linearity

- -<u>optimized Hold</u> still shows non-linearity (shift up to 30ns!!).

- -gain setting for low-gain pre-amp influences response from high-gain input. Charge division?

What is the optimum Hold position (conc. response ⇔ linearity)?

Residuals: Max. 8%

scale: 24.952 $\frac{mV}{pC}$

offset: 1149.61 mV

FE

Autotrigger tests (ongoing):

-Single-photon peak spectrum / MIP signals
 (radiactive source)

-Jitter and delay tests of auto-trigger:
 „large signals trigger faster than small signals".

Digital Part tests (pending):

-Probe-register / ADC ramp problems.
 Is the second testboard with external ramp available?
 Results important for **DIF** (and HBU) setup!

Conclusions

-AHCAL techn. prototype (TP) does not cover a full slab,
  but ~150 channels (2 HBU0s, tile-prototypes).

-Eudet module (detector layer) requires HBU redesign (mid 2009).

-timeline for TP is defined by HBU0 (input SPIROC2, tile geometry).

-DIF VHDL programming and DIF hardware interface to detector
  needs closer coordination (ECAL, DHCAL, AHCAL) soon.
  (=> hardware round-table meeting?)