DIRAC: DIgital Readout Asic for hadronic Calorimeter
R&D Status

EUDET/CALICE Electronic Meeting
LAL Orsay

Renaud Gaglione

IN2P3 Institut de Physique Nucléaire de Lyon
Bâtiment Paul Dirac
4 rue Enrico Fermi
69 622 VILLEURBANNE Cedex

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Plan

Introduction

Architecture

ASIC Tests

Tests results overview (MicroMegas mode)

Tests with detectors

MicroMegas protections

Next ASIC

Plan

Requirements

In order to build a DHCAL with high granularity near the ILC, FE ASIC must match different gaseous detectors. . .

	GRPC	MicroMegas	GEM
Charge	0.1∼10 pC	1∼100 fC	1∼100 fC
C_{det} (1 cm^2)	60 pF	60 pF	60 pF
t_r	2 ns	<2 ns	<2 ns
width	20 ns	complex form	20 ns

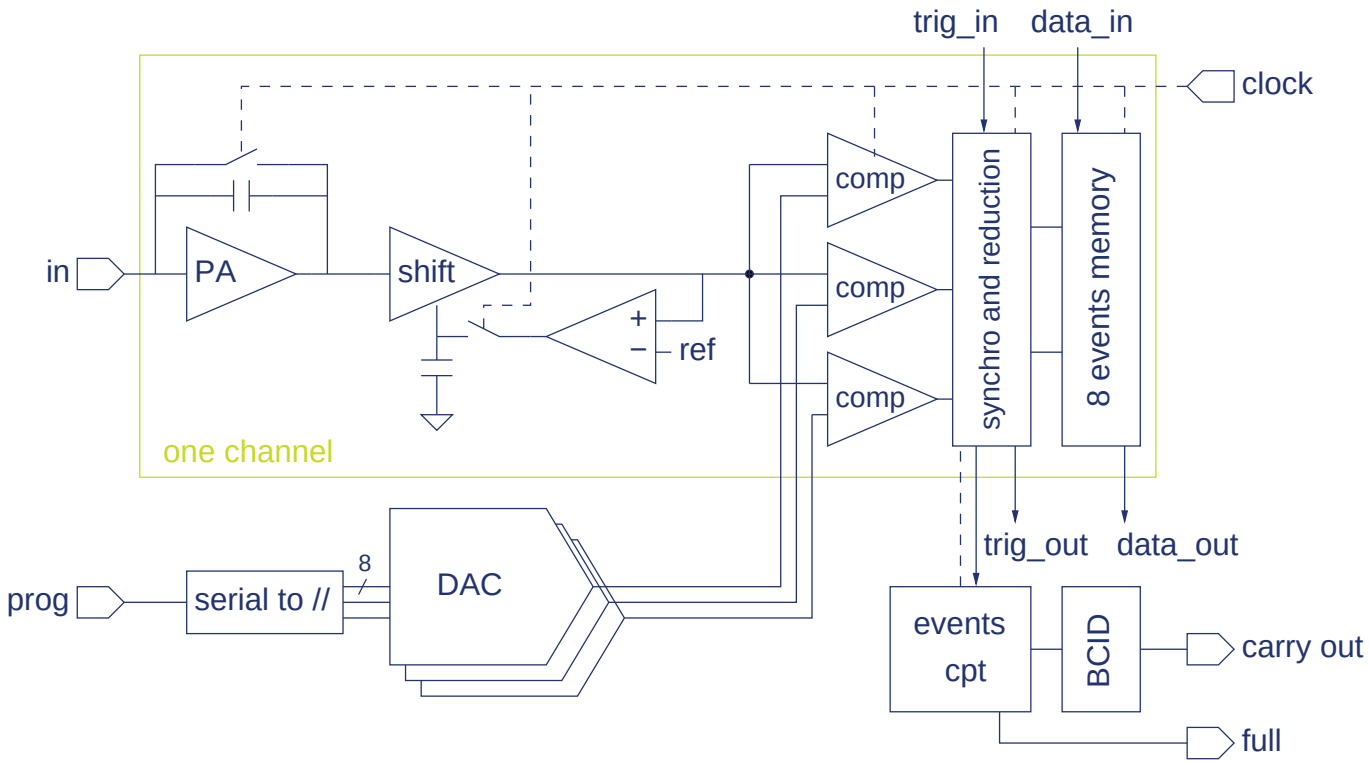
. . . and respect beam clock characteritics:

	Minimum	Nominal	Maximum
Bunchs #	1320	2625	5120
Period (ns)	189	369	480
Rate (Hz)		5	

Plan

Synoptic

Compare input charge to 3 thresholds (set by 3 DACs) and store the 2 bits energy information.



Operation

Synchronous architecture on beam clock (trains and bunchs):

During trains:

- Beam on: analog charge integration;
- Beam off: comparisons to thresholds, store results.

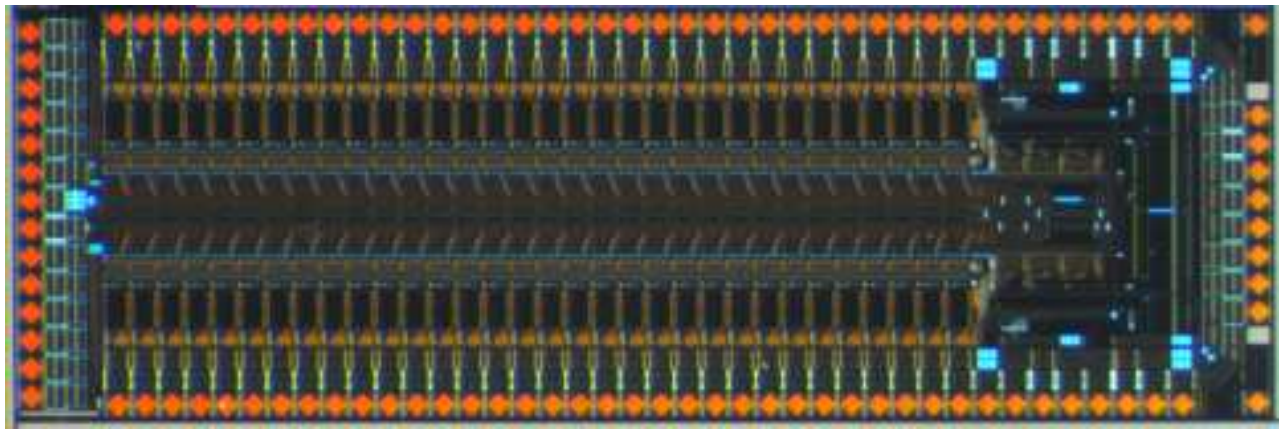
Outside trains:

- Standby;
- Digital data readout;
- Slow control.

Main features

- 64 channels;
- Low-cost AMS CMOS 0.35 µm process technology;
- Power consumption $<$1 mW per channel + 1% power pulsing:
  $\rightarrow$ $<$10 µW per channel
- 2 gains: 100 mV/pC and 5 mV/fC;
- 3 thresholds, each on 8 bits for 1 V, *i.e.* 3.9 mV/DAC:
  $\rightarrow$ 40 fC/DAC and 0.8 fC/DAC
- 12 bits BCID counter;
- Internal memory of 8 events (2 bits per event);
- Analog input on each sides: easy PCB routing.

Photography



Only 1.5×4.7 mm^2

- Top and bottom: analog inputs;
- Right: analog power supply and bias;
- Left: digital I/O.

Plan

ASIC Tests

For each input charge:

- Measure trigger efficiency *vs* thresholds;
- *S-Curves*: fit with a Fermi-Dirac distribution:

$$S(x) = \frac{max}{1 + e^{\frac{x-\mu}{w}}}$$

max : maximum efficiency
μ : inflexion point abcisse
w : inflexion slope

Next:

- μ *vs* input charge for each channel;
- Linear fit:

$$F(x) = 1/g \cdot x + b$$

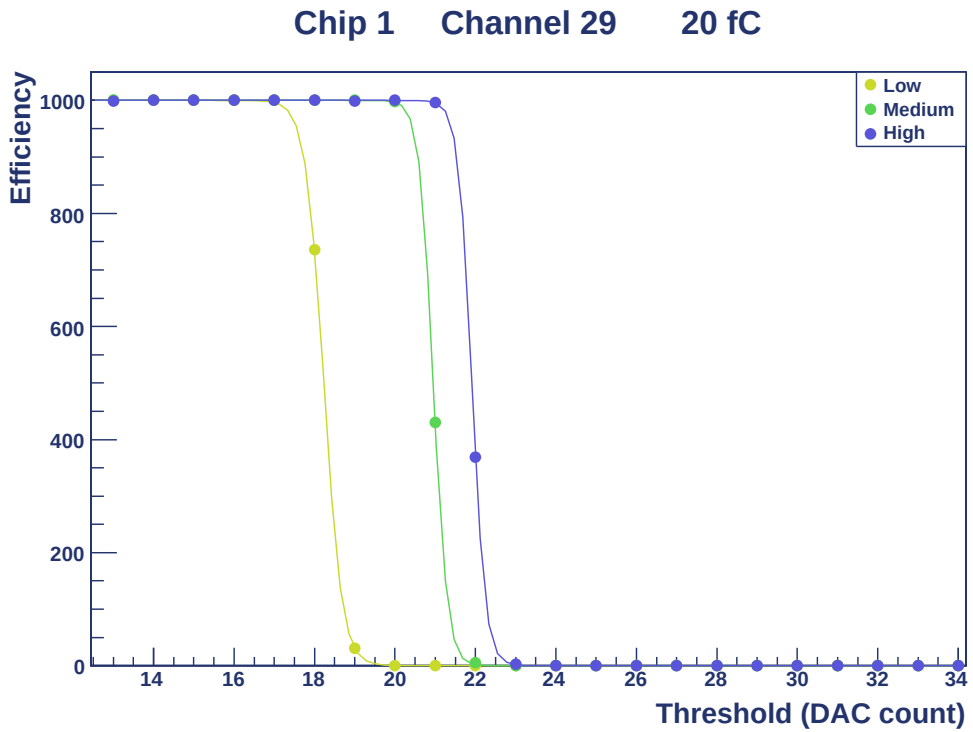
g : gain
b : pedestal

- Non-linearity: difference between fit and measures.

Plan

S-Curve example

Trigger efficiency + fit (1 channel: 3 comparators):

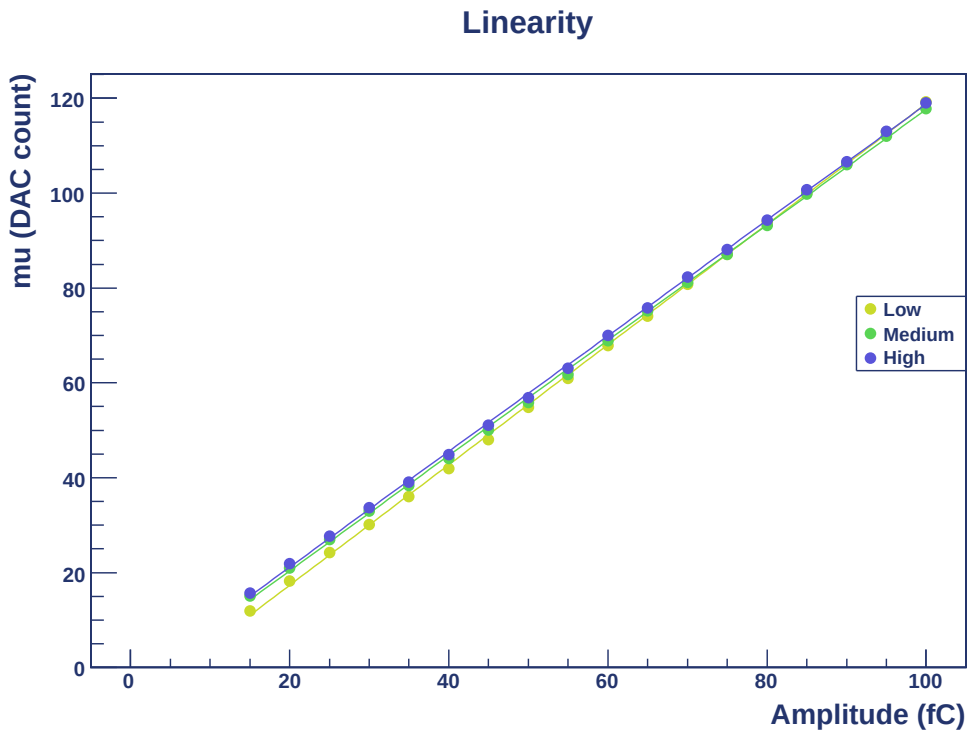


From 100% to 0% <2.4 fC

Worst dispersion among 3 comparators: 2.5 LSB, *i.e.* 2 fC.

Linearity

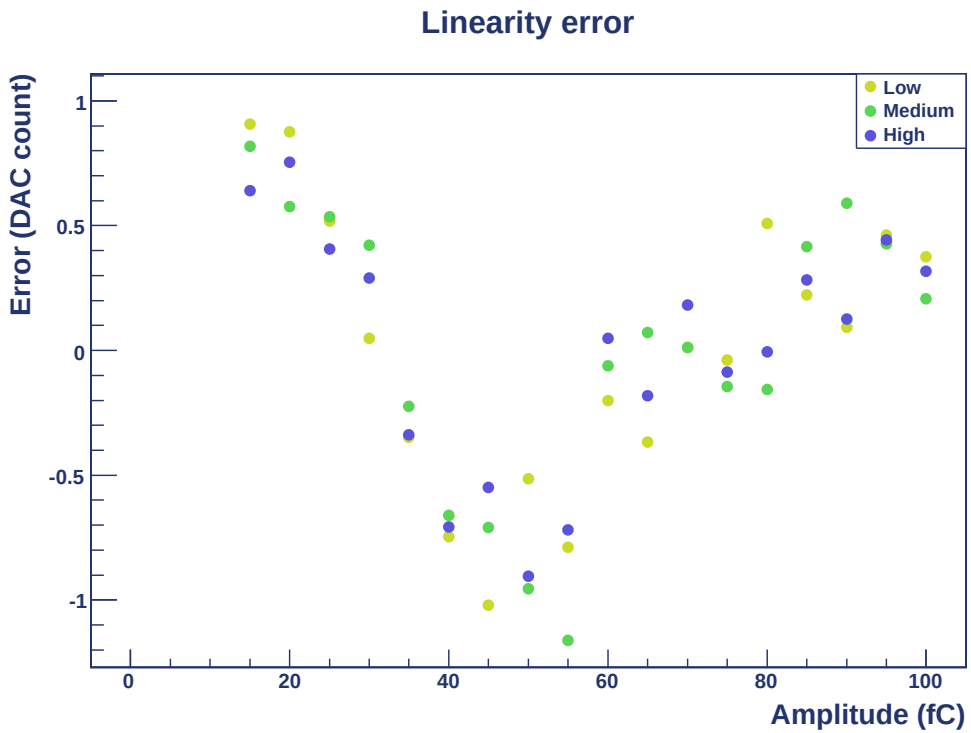
μ versus input charge + fit (1 channel):



More reliable information: non-linearity !

Non-linearity

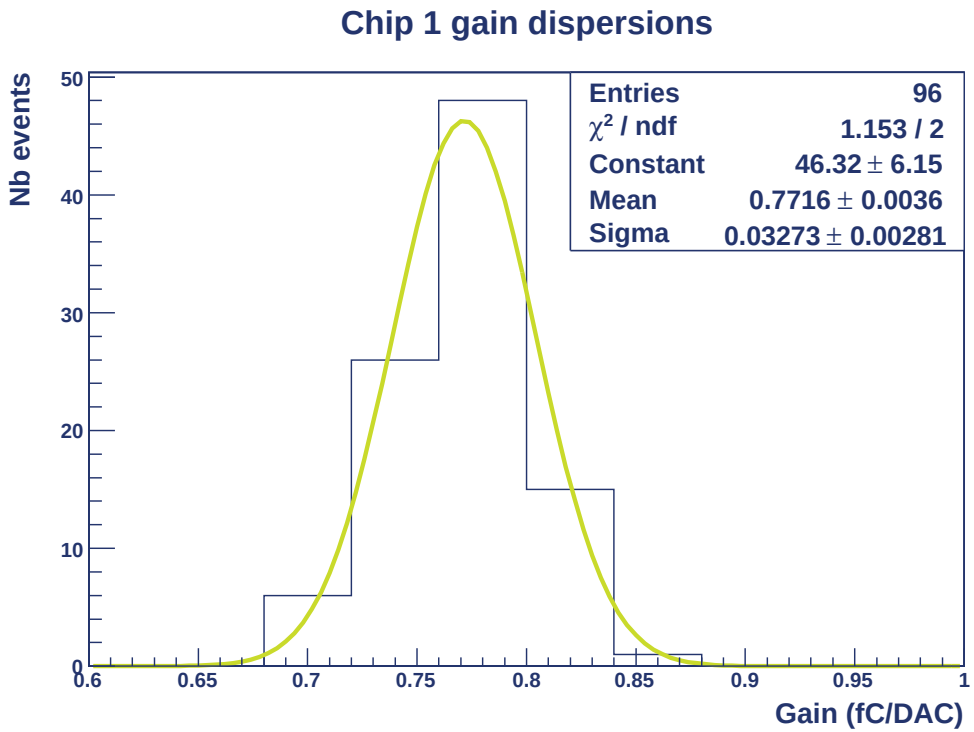
Difference between linear fit and measures (1 channel):



The non-linearity is typically in ± 1 LSB, *i.e.* ± 0.8 fC.

Gain dispersions

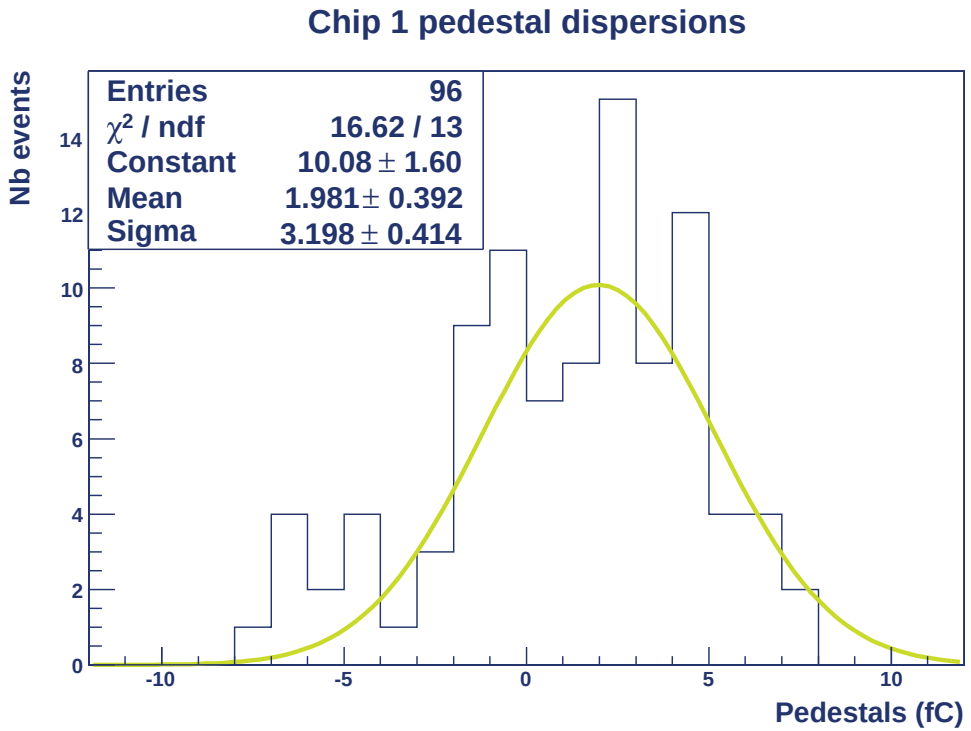
g distribution for all channels (1 ASIC):



Mean value of g: 0.77 fC/DAC.

Pedestals dispersion

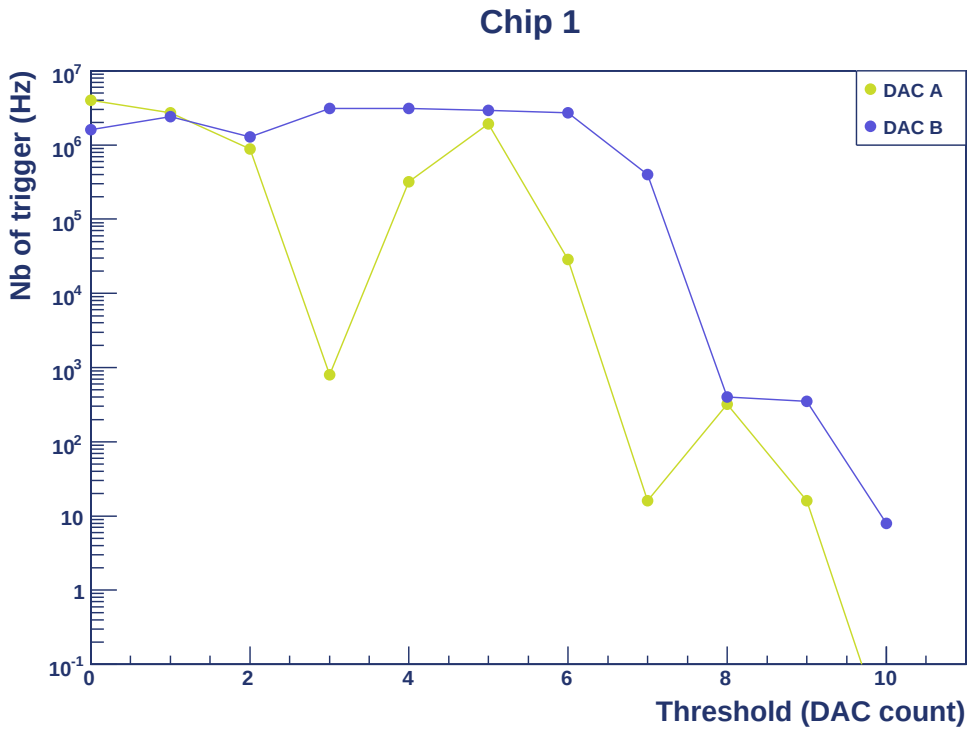
$b \cdot g$ distribution for all channels (1 ASIC):



Monte-Carlo Simulation : gaussian with σ=1 DAC;
Measure : non-gaussian, total dispertion ± 10 DAC : must be improved !

Auto-triggering

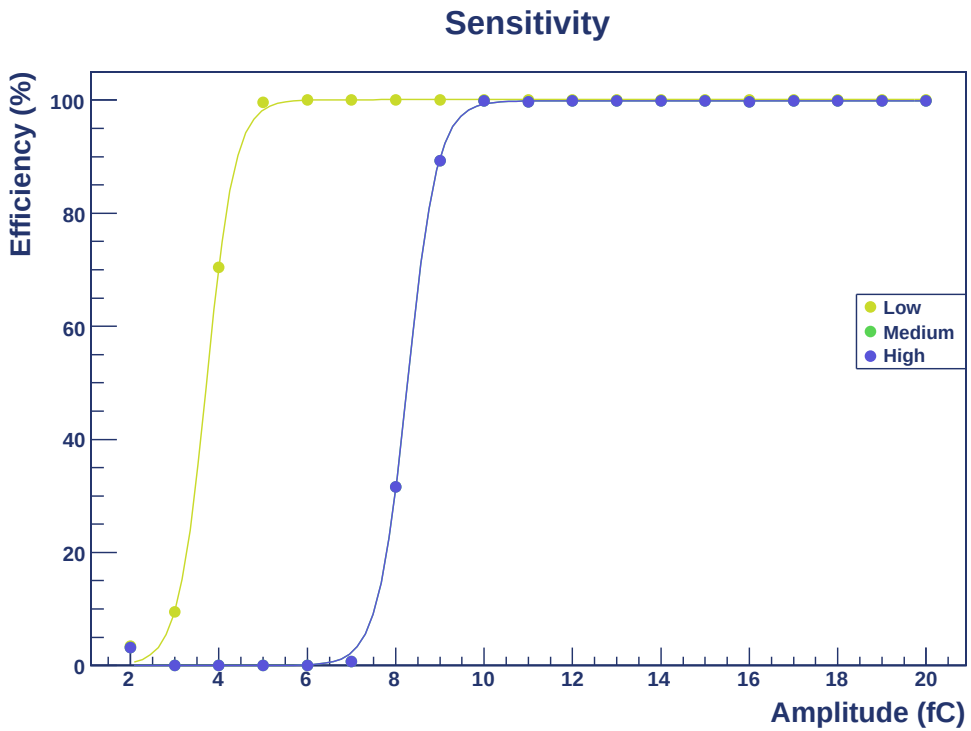
No input charge. False trigger rate versus threshold.



Channels with high pedestals stop to auto-trig @ threshold near 10 DAC (8 fC).

Sensitivity

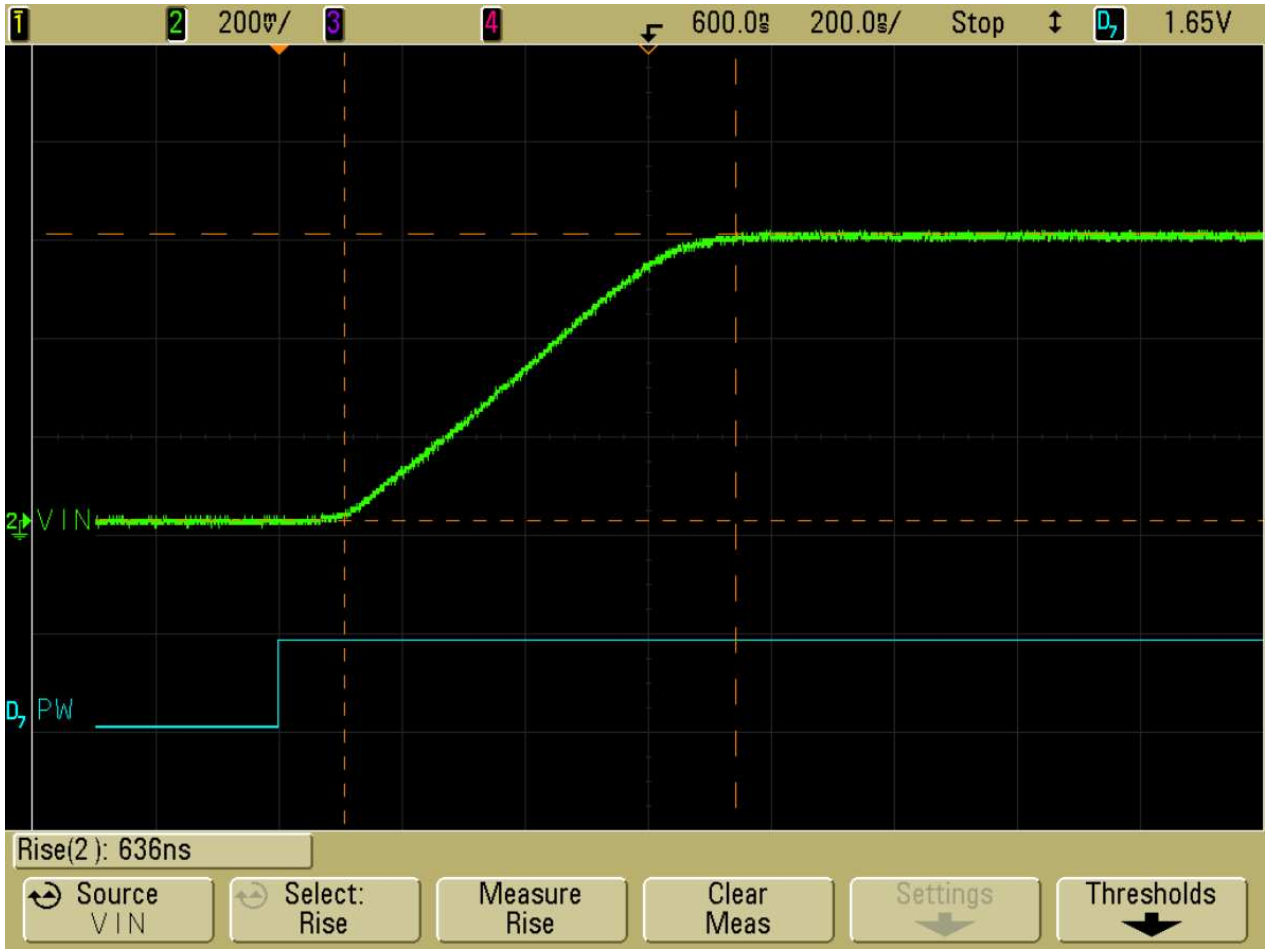
DAC code : 14 (above auto-triggering threshold). Trigger efficiency *vs* input charge.



Best 50% efficiency: 3.5 fC.

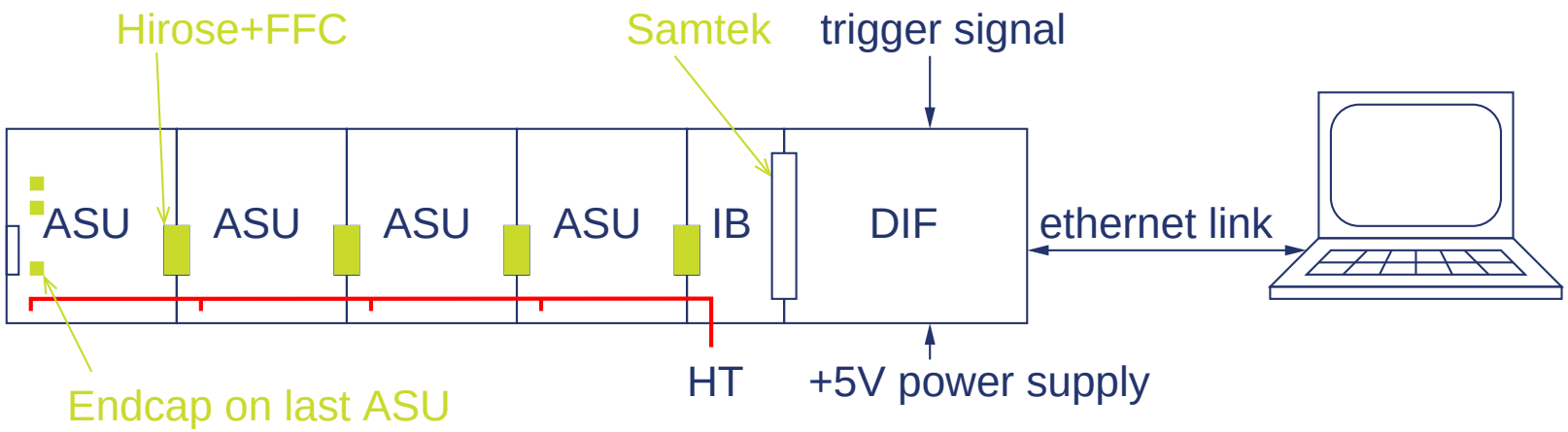
Power pulsing

Power on time <800 ns.



Plan

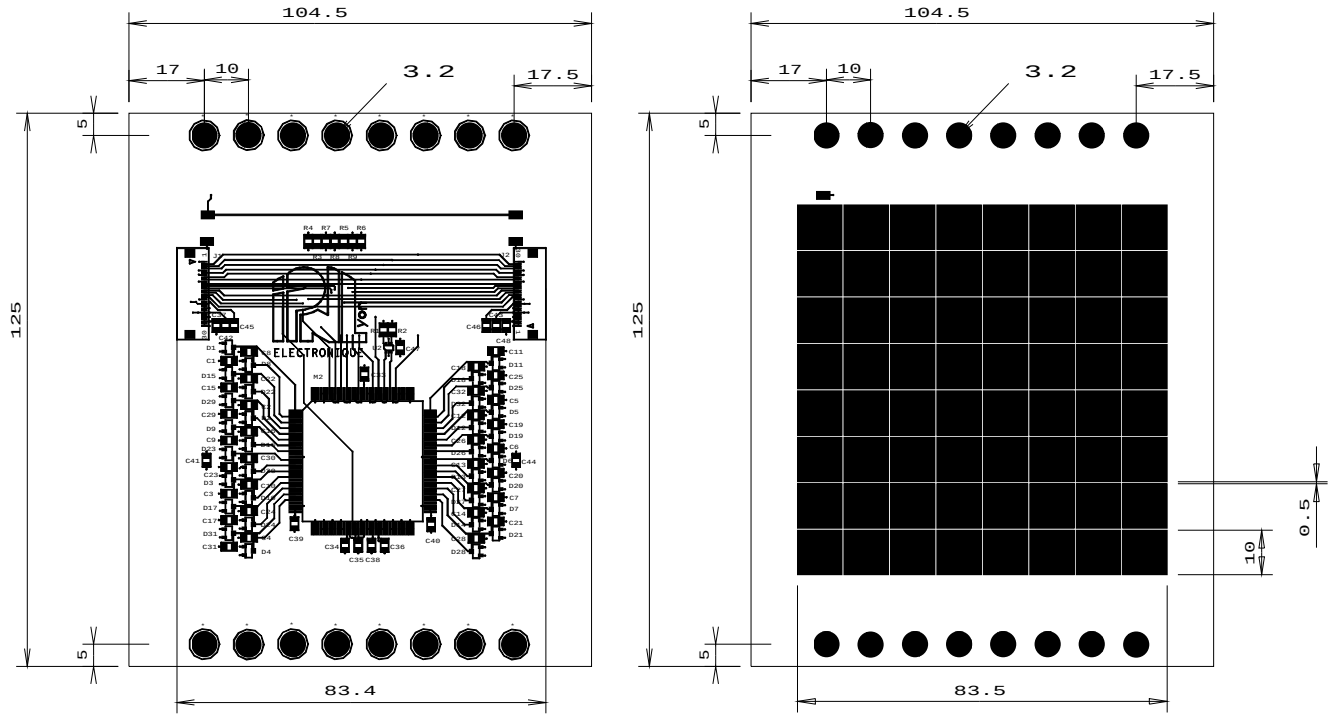
Assembly schematic



First: custom DAQ with ethernet for tests;
Next: connection to the DHCAL DIF (see Julie Prast's talk).

Active Sensor Unit cards

6 layers. Burried and blind vias for anode connection.



(a) top (b) bottom

No components outside pad area to test MicroMegas assembly.
Possibility to solder MicroMegas sparks protections.

Status

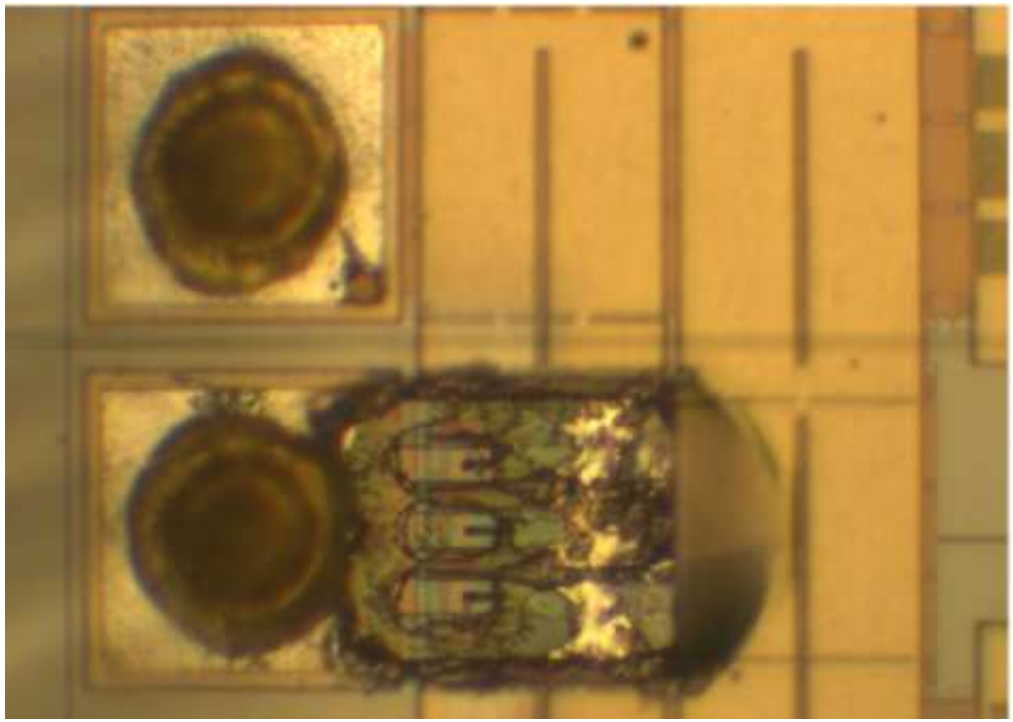
- DAQ and intermediate board ready;
- 6 ASU are on the way;
- VHDL near to be ready (synchronisation on cosmic ray to finalyse);
- Acquisition software to be finished (manpower needed !);
- ROOT C++ event class definition on the way (LAPP+LLR+IPNL);
- MicroMegas: bulks will be realized at CERN;
- RPC: detector OK, mechanics on the way.

We will be ready for august beam test !

Plan

Protection necessity

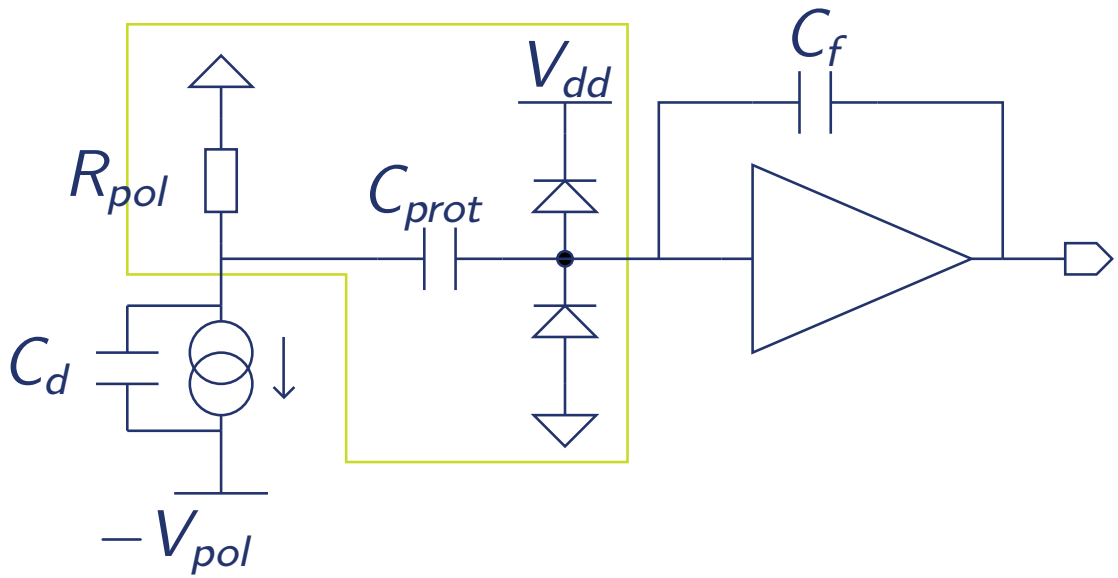
When sparks occurs, anode are short-cicuited with mesh. Example @ 650 V:



ESD protection included in I/O pad not sufficient !

Proposition

cf. CAST and COMPASS:



$C_{prot} > C_d \Rightarrow C_{prot} = 470$ pF. $R_{pol} = 1..100$ MΩ
Similar problems for ILC TPC (mechanical integration of discrete components difficult) !
Possibility to work with CEA for a protective ASIC ?

Plan

Improvements

- Internal trigger bug correction: OK;
- Add trigger masking feature (in slow control): OK;
- Add internal test cicuitry: OK;
- Add multiplexed analog readout: on the way;
- Add 2 MicroMegas gain (in slow control): OK;
- Minimum threshold reduction:
  - Lower offset discriminator: OK;
  - Lower offset DC-servo loop: on the way;
- Add LVDS clock: OK : thanks to LAL;
- Power supply pinout simplification: OK;
- Decrease power consumption: on the way;

New foundry submission this summer !

Thank you for your attention !