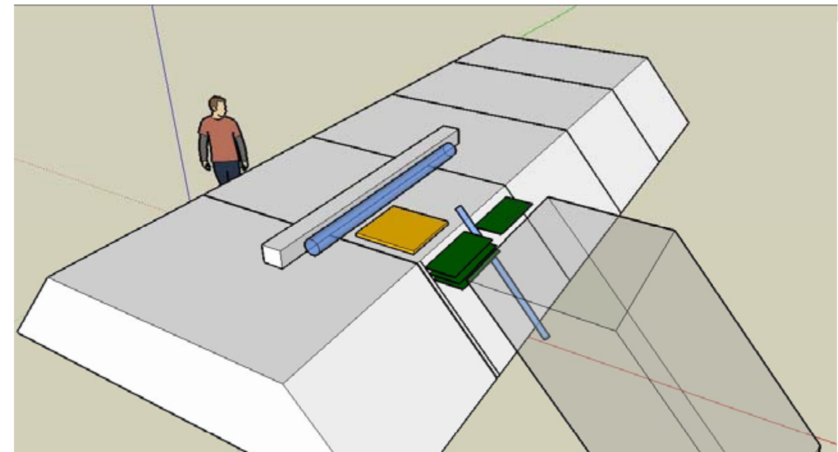
ECAL electronics

- Roadmap
- Mechanics
- LV Power
- HV power
- Data rates
- DIF
- info



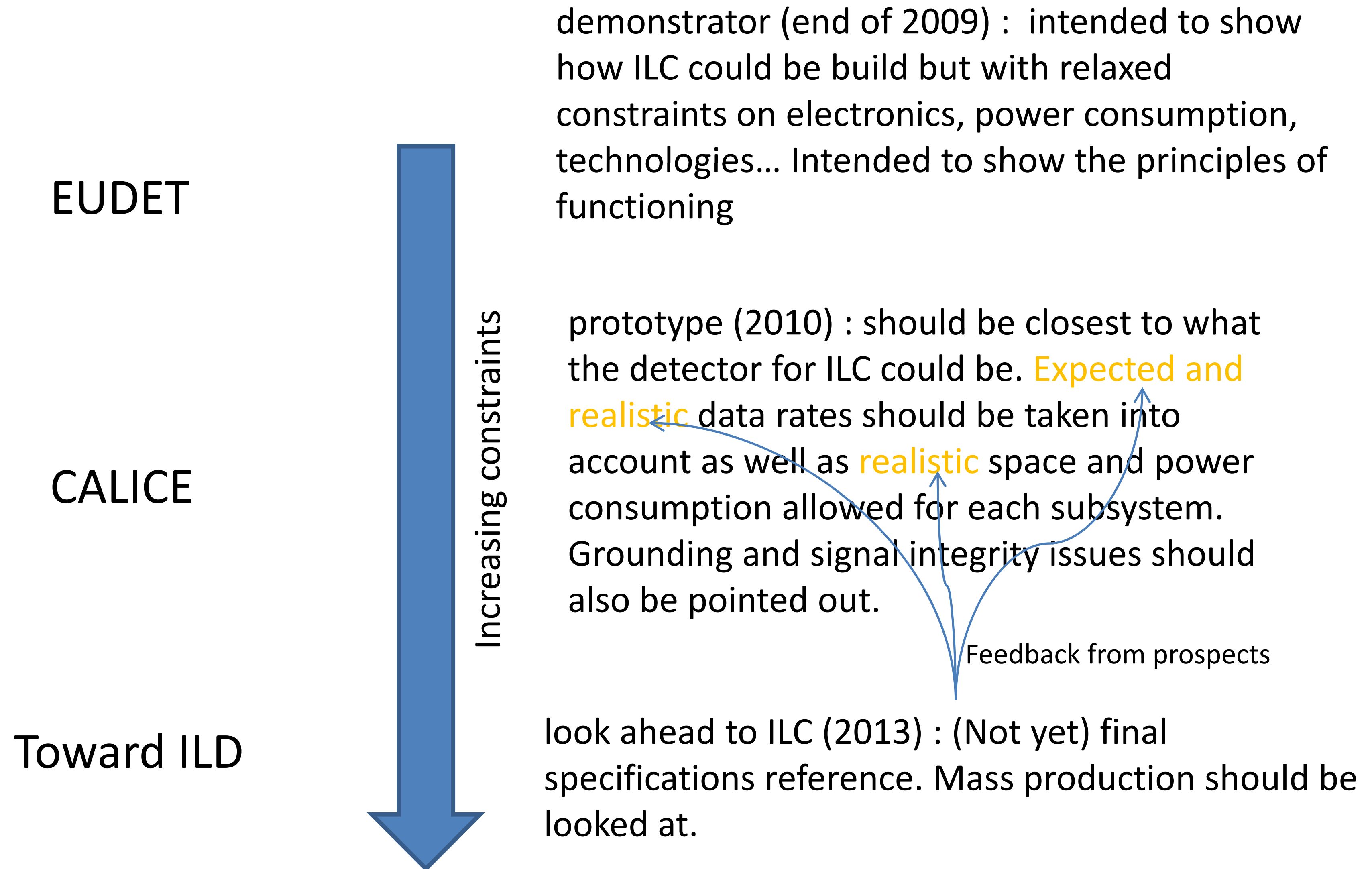
CALICE Electronics meeting at LAL, June 2nd 2008

EUDET ECAL meeting at LAL, June 3rd 2008

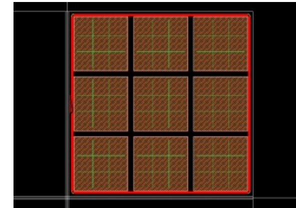
Rémi CORNAT

LLR (CNRS/IN2P3)

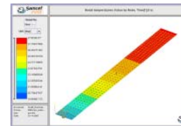
Roadmap

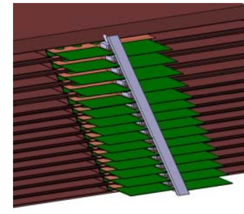


Status on ECAL



- Wafers
  - Hamamatsu lot being tested : OK
  - 3x3 tests wafers being designed (Xtalk measurements at LPC)
- Mechanics
  - First long structure (Marc, LLR)
  - Thermal studies (LPSC)
  - 3 layers prototype
  - ILD prospects
  - Uncertainties about SLAB thickness (glue, foam, …)

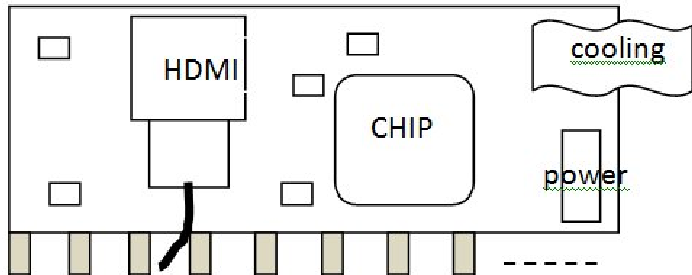




- Electronics
  - Lot of work done in UK (DAQ, gluing tech., DIF,…)
  - SKIROC 2 (Q1'09)
  - 2 DIFs : try to share efforts (USB from DHCAL, SLAB itf)
  - System level thoughts (power, data rates and protocols, CCC, CC,…)
    - To be done together
    - Urgent
  - Web site

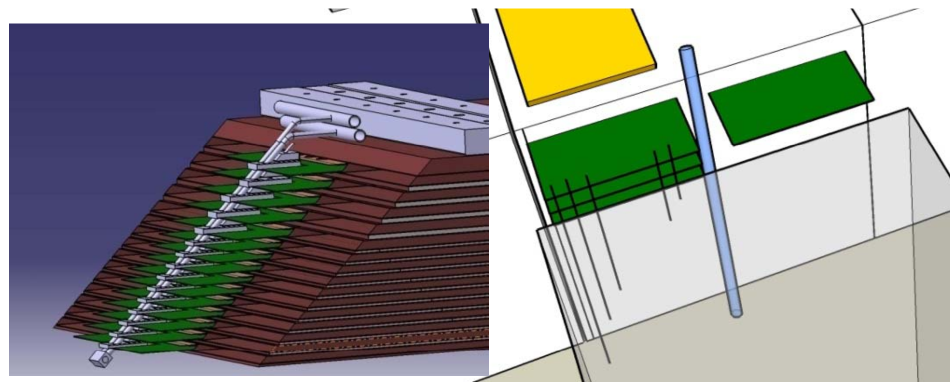
Bottleneck of meetings

ILD !



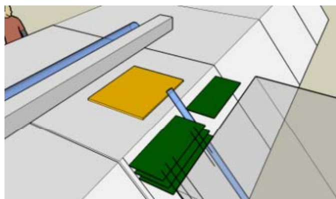
DIF is part of last ASU of the SLAB
Allowed space : 6-7 x 3 x 0.6-0.8 cm3 !
Small amount of components allowed

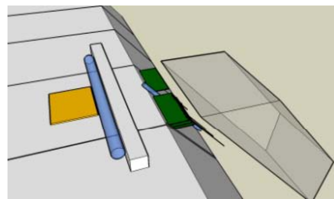
Quite no place for cabling : DAQ + HV + GND
LDA has to receive 30 cables (45 cm linear)
Service space is mostly taken by cooling

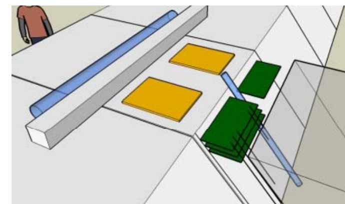


Space for HV and GND is being negotiated

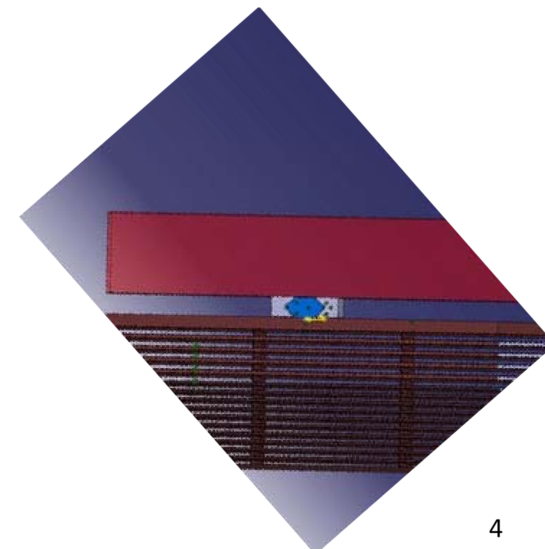
Space for LDA : 10x10 cm2 + connectors and cable curvature, holes (small!) for cables below rails







Outter, inner, divided



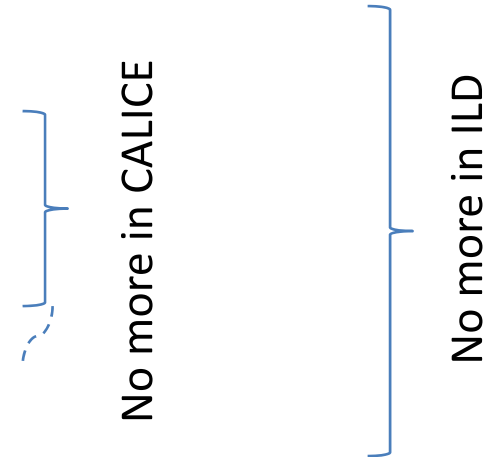
Conclusion on ILD section

- Stringent requirements from ILD
- Relaxed constraints for forthcoming developments (EUDET)
- BUT ILD design have to be kept in mind
  - Provide realistic parts
  - Reusable components (life time of developments)
  - Avoid divergence

So, what about EUDET ?

Developers need to monitor/debug/access their parts : feasibility demonstrator

- Parts can be un-mounted
- Adapter board
- Relatively large DIF (usb, connectors)
- Accessibility
- Not so low data rate (test beam structure)



Not intended for fine physics

But feasibility is a nonsense if it not demonstrate how ILD goal could be reached
ILD functionning mode : power pulsing, etc…

Expected data rates

- Beam structure dependant
  - ILC
  - Forthcoming test beams
- Angular dependence (physics signals)
- Uniform noise both from physics and electronics
- Needs careful detector simulations (first idea yet)
- Different design according to location (ILD)
- Depends on Zero suppression scheme implemented in ROCs
  - Whole chips when 1 channel triggered (current versions)
  - Only triggered channels (next versions)

At the ouput of the DIF, it cannot be more than the read-out clock frequency times the number of partitions of chips : 2 parameters to adapt the system to the actual needs

Without Z suppress

DATA rates	Barrel (mid)	Barrel (end)	End cap
Phys.	0.08-1 Mb/s	1-5 Mb/s	5-10 Mb/s
Noise phys. (1)	1 Mb/s	1 Mb/s	1 Mb/s

To be confirmed

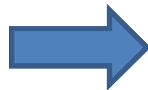
Rate for TB (EUDET)

EUDET case

- Must take as (reasonable) high as possible # of evt (detector calibration)
- TB structure : spill of 5-10s every 2 mn with 10^14 particles or more (1 collision every ns…)
  - Chips must be externally triggered (high number of particle)
  - Chips full will become full quickly
  - Must be read-out immediately after being full
  - Read-out time determine the evnt rate
    - Make read out time small
    - Not the case of ILD…(chips almost empty)

    } contradictory

Avoid to make a specific design but something reusable for CALICE/ILD

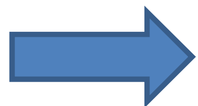


Compromise : ~100 evt/s

100 evt/s ?

- Assuming : 4 chips full every times on the highly occupied layer, 64 ch/chip, 16 evt buffer
  - Data = 4 * (16 ID + 16*16 time + 16 * 64 * 16) = 16656 bits
- Assuming 5 MHz read-out clock and no partitions
  - 16565/5E6 = 3.4 ms (for 16 evt)
- Number of events that could be acquired in one spill
  - 10s/3.4 ms = 2.9 k
  - To be divided by N/4 if **N** chips are full (max is N=16 in the tower)
  - To be multiplied by **P**, the number of partitions read-out in //
- Actual rate : 1 spill every 2 mn (could be 1 mn)
  - 2.9 k / 120s = 24 Hz (50 Hz)

EUDET specific



P=4, data rate at the output of a DIF = 20 Mb/s

ROChips partitions

- ILD
  - Reliability
  - Keep number of SLAB-DIF connection LOW
  - Power consumption
- EUDET/TB
  - Data rate

ILD: P=1-2 typ.
Partitions can be read sequentially

EUDET/TB: P=2-4 typ.
Partitions MUST be read at the same time

For EUDET, the two ways should be implemented in order to
- Be compatible with test beam requirements
- Allow realistic thermal tests, realistic functioning

Comparison to ILD baseline

The noise occupancy of one channel is expected to be at the level of 10^-5 per BX. For a ROC chip of about 100 channels, the occupancy is about 10^-3 per BX. For a bunch train of 5000 bunches, a chip is fired 5 times (mean).

Read-out time for noise : 1.1 ms / chip (no Zsup) 1Mb/s, 40 us (with full Zsup)

In addition, physics signal : 2820 bunch crossings every 200 ms each spaced by 337 ns. It is expected a maximum of **75000 hits per bunch train** (physics) within ILC specifications. It corresponds to about **25** fired channels per bunch (mean number) and channel occupancy of about **0.002** per bunch train (for 1 cm2 pixel area).
For a layer with 7 ASU of 4 wafers of 256 channel each, the number of cell hit would be 15 (0.002*7*4*256) . Assuming that each hit cell is located on a different chip (very pessimistic) it corresponds to 16 kb (15*(16+16+64*16)) of data every 200 ms and then a mean data flow of **80 kb/s**. It is supposed the occupancy does not vary for 0.25 cm2 pixels. (MC simulation from V. Bartch), no Zsup

How far can we be confident in this ?

Security margin : 100 = 10 Mb/s

CCC

- EUDET/TB
  - Externally (to the ROC) managed acquisition
  - Requires TRIG, start, stop signal
  - Global synchronization : feed back from ROC (bufferfull, etc…)
- ILD
  - Stand alone (start/end burst)
  - Locally managed by DIF

Isochronous signals

Distribution path ?

(see Vincent's talk)

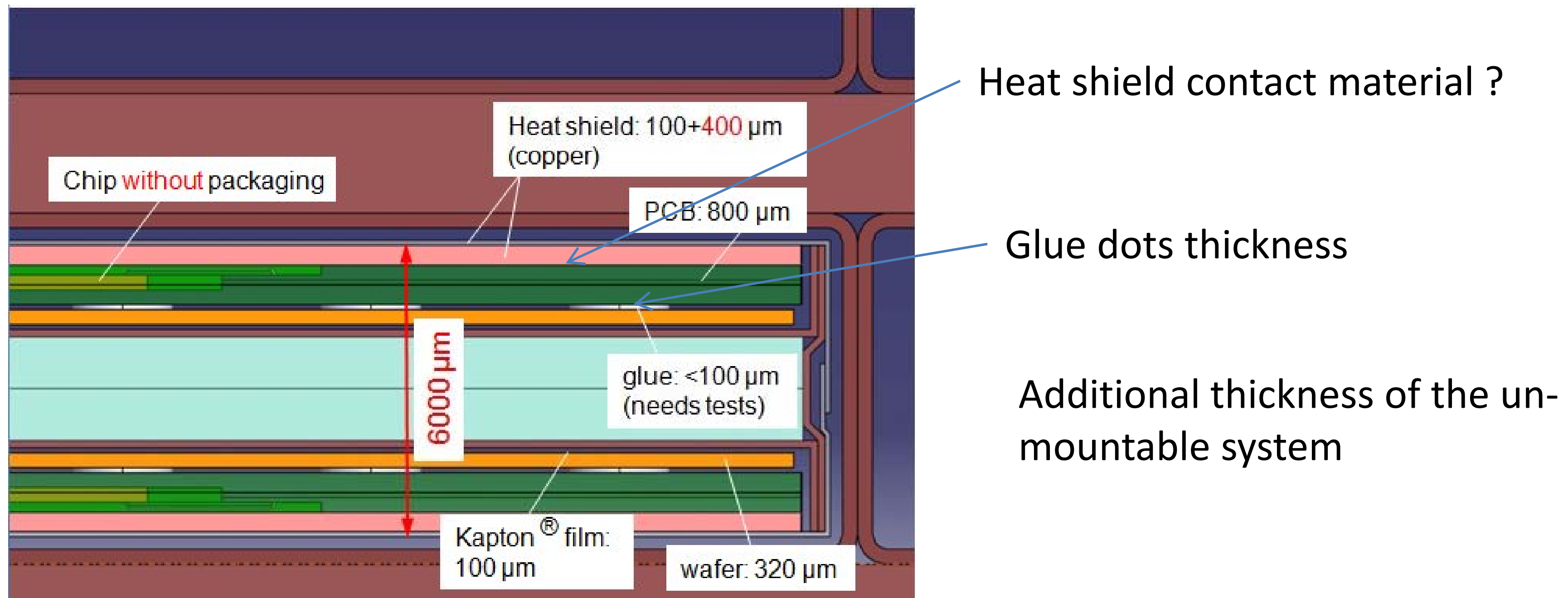
SLAB integration

- Many unknown points
  - Overall thickness
    - Gluing/connection
    - Thermal contacts (foam,…)
  - HV path
  - Cooling outside the structure
    - Dif components placement
      - Place for contacts
      - Thermal dissipation of FPGA
    - Space available for HV, GND (cables & connectors !)
- Longitudinal structure
  - No more adapter board
  - DIF as part of last ASU
  - No un mountable features
- For EUDET, ~don't care of most of these points
  - But need to decide how it is relaxed

CALICE
Calorimeter for ILC

SLAB

- Minimise the thickness of non W materials
- Developpers need to access/replace/debug
- Another compromise to be found



DIF/DAQ (1)

- To optimize DAQ (CALICE/ILD steps)
  - Different systems according to location ---
  - Adaptable architecture +++
    - According to running mode (Cosmic rays, TB or ILC beam structure)
    - According to location

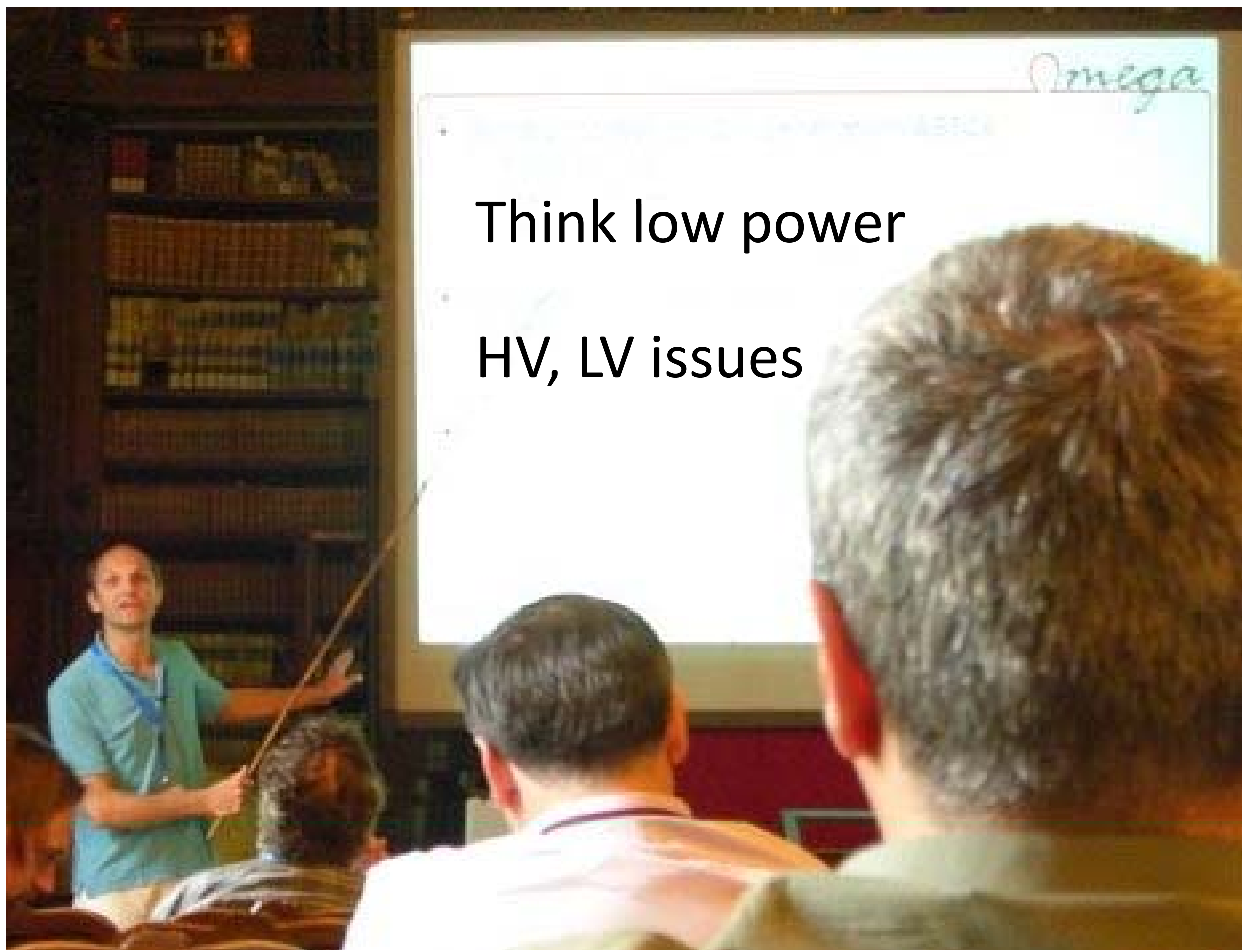
Play with freq, #partition, RO cables (pairs), # of CC

- Intermediate Concentrator Card (CC)
  - For EUDET DHCAL
  - Could be kept for other detectors
    - Simplest interface
    - Stand alone debug tool
    - Adaptable architecture
    - Low power (located inside, LDA could remains outside)

DIF/DAQ (2)

- Think low power
- Think low space
- Think easy debug

Simple protocol, well dimensioned according to the local data rate

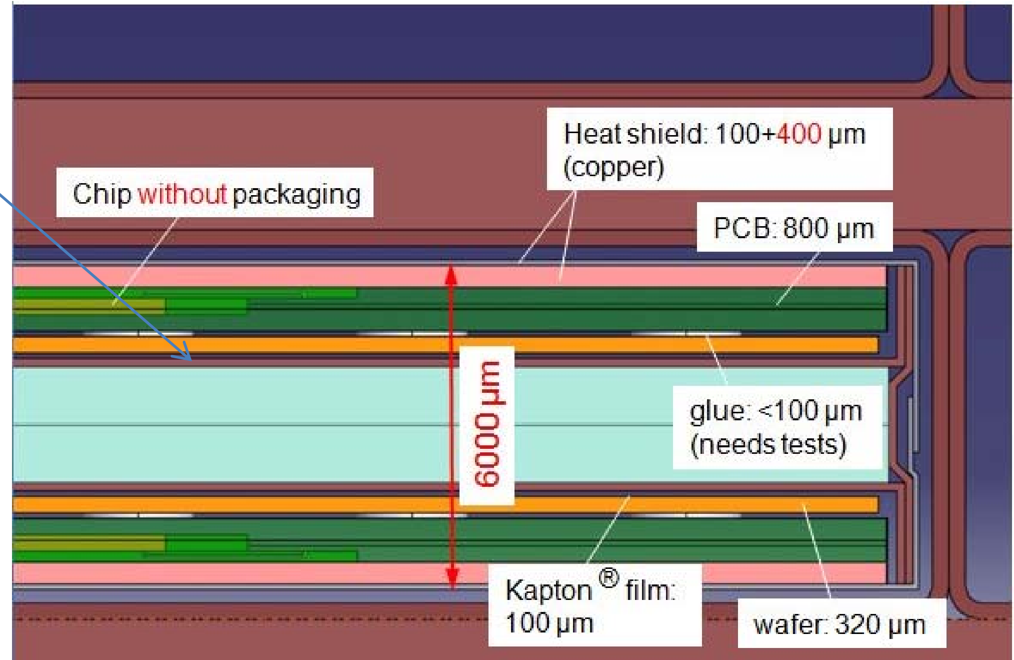


CALICE
Calorimeter for ILC

HV (mechanics)

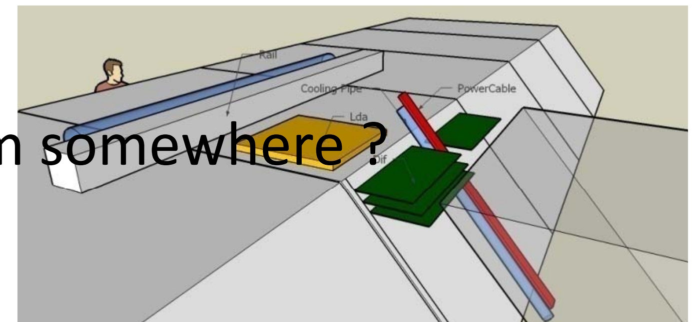
HV on kapton film

Glue ?
Foam ?
Thickness !



Can not be un mounted !
- Find a solution
- Or discard other features for un mounting ASUs

Location and connectors (bus topology) from somewhere ?



No matters for EUDET but…

CALICE Calorimeter for ILC

LV

- Power pulsing will be tested
  - Power supplies as if it were ILD
  - Distant 8-10 V main PSU, low current capability
  - DIF (of LDA or …) has to provide constant 3 V
    - Regulator
    - Capacitances to locally store power for chips
- Low drop-out regulator (thermal dissipation)

Direct powering : U=q/C, dU= didt/C
dU = 100 mV, di=128*1 mA, dt=9 ms : C = 12 mF

With regulator 8 V – 3 V : U=q/C, dU= didt/C
dU = 4 V, di=128*1 mA, dt=9 ms : C = 300 uF

Place for capacitances on ILD DIF !

eDIF at LPC

- DIF for lab. Tests of ASU (cosmics)
- Also a prototype for a debuging tool on beam
- Common developments with standard DIF or CALICE
  - SLAB/ASU interface, with a larger scope
    - Manage 2-4 SLABs in //
    - Access to debugging features of ROCs
  - USB
- Board received since 2 months

Compatible with SkiROC 2
FW could dev. By LPC ??

From DHCAL ? = CALICE common ?

Conclusion

- Options to configure HW/FW/SW in order to perform ILD like tests (data rates, power pulsing, thermal tests)
- System level specs with coloration (EUDET, CALICE, ILD)
- To be finalized for the next CALICE week

- Electronics WEB site for CALICE
- CALICE electronics mailing list
- CALICE technical notes
- EVO meeting about electronics
  - Weekly ?
- EUDET specific inputs tomorrow

High tech cooling solution