IN2P3

Omega

CAC UR IPN Orsay

HARDROC STATUS

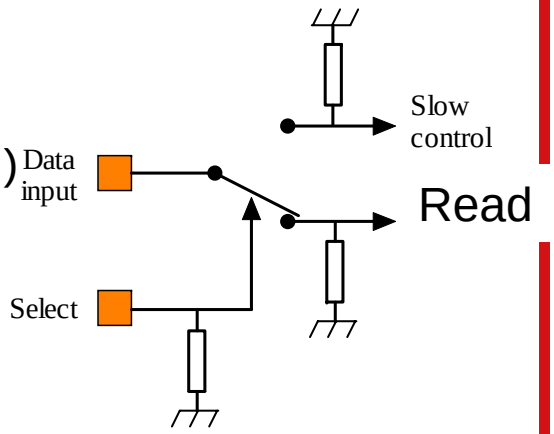
June 2nd, 2008

Orsay MicroElectronic Group Associated

DESIGN of HARDROC2

- Hardroc2 submission: mid june 08

- Correction of the minor bugs of HR1:
  - mask, memory pointer: dummy frame
- Shift registers improvements (multiplex, default, extra FF)
- Bypass on critical signals



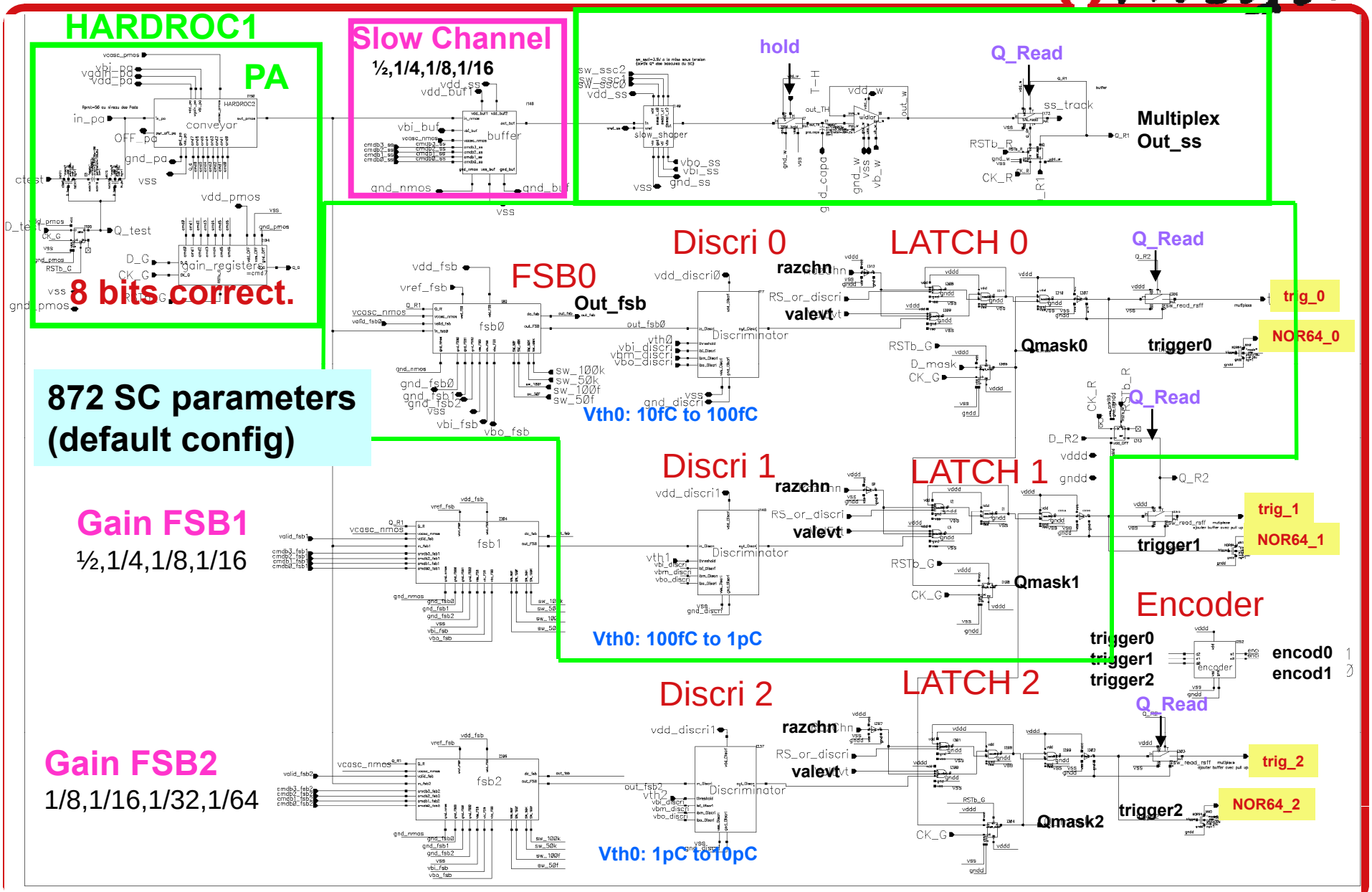
- **Power pulsing:**
  - Bandgap + ref Voltages + master I: power pulsed
  - POD module (power budget): see Fred Dulucq's talk

- **Dynamic range extension**
  - Gain correction: 8 bits instead of 6
  - 3 shapers and 3 thresholds (=> 3 DACs):
    - 10 fC, 100fC, 1pC (megas)
    - 100fC, 1pC, 10pC (GRPC)

- **Bandgap redesigned**

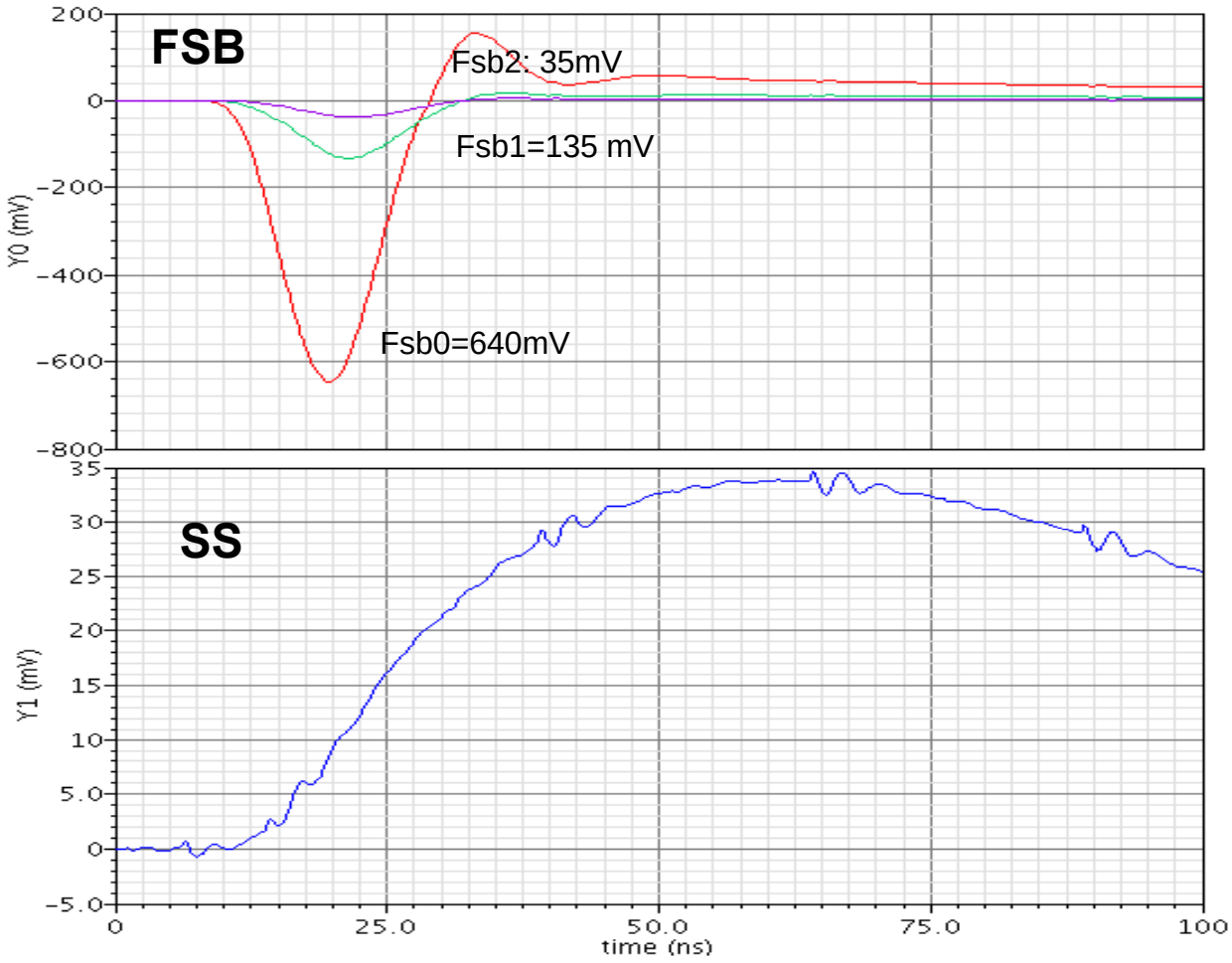
- **HARDROC2 = HARDROC1 + modifs**
  ⇒ **HARDROC1 = BACKUP**

HARDROC2: analog part



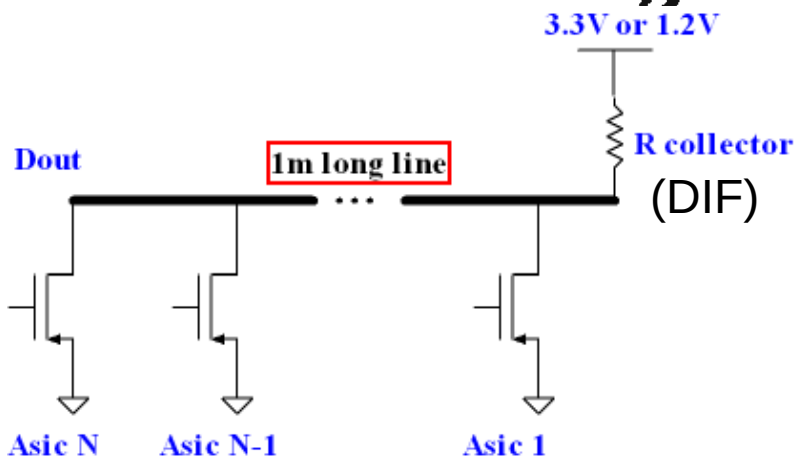
SIMULATIONS

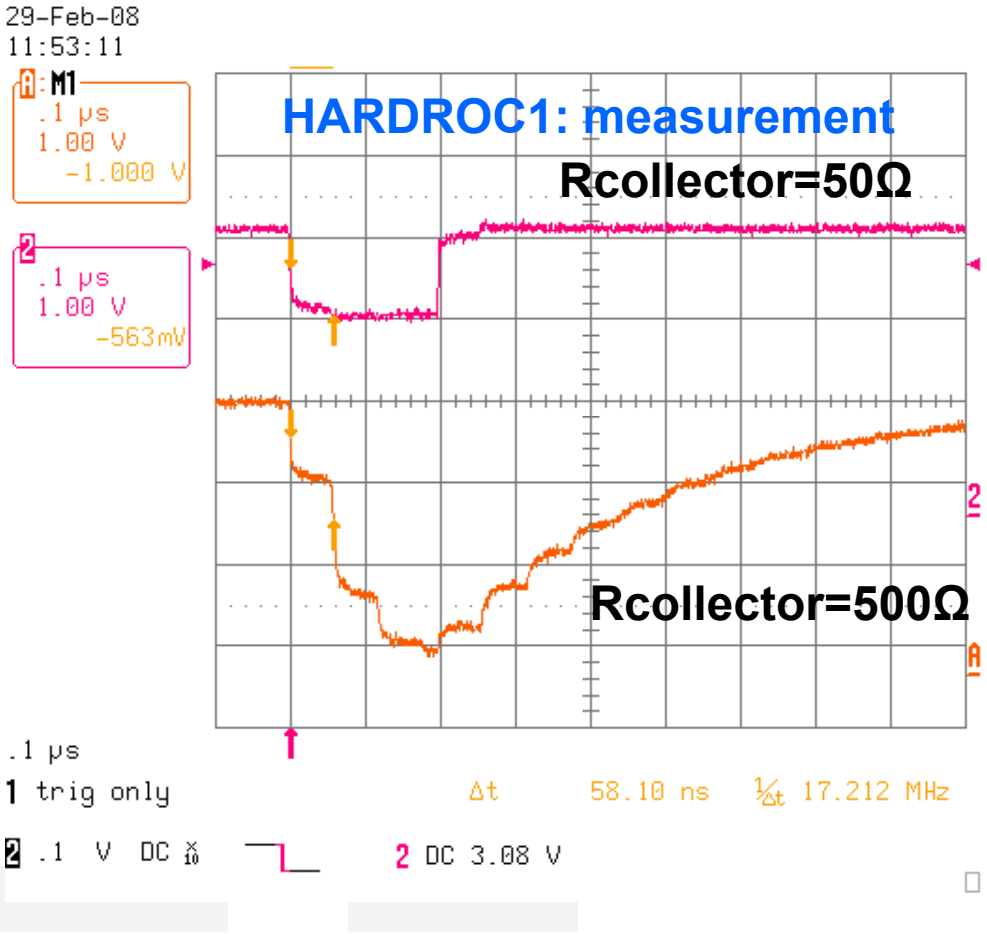
Default SC configuration and Qinj=100 fC



Open collector signals after 1m long line

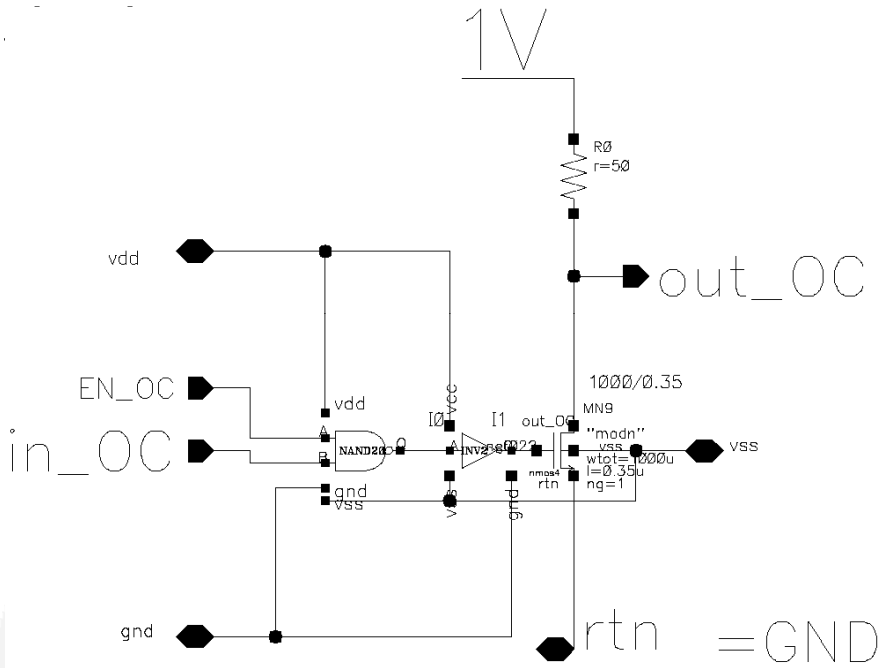
- 5 m data line / slab -> 500 pF

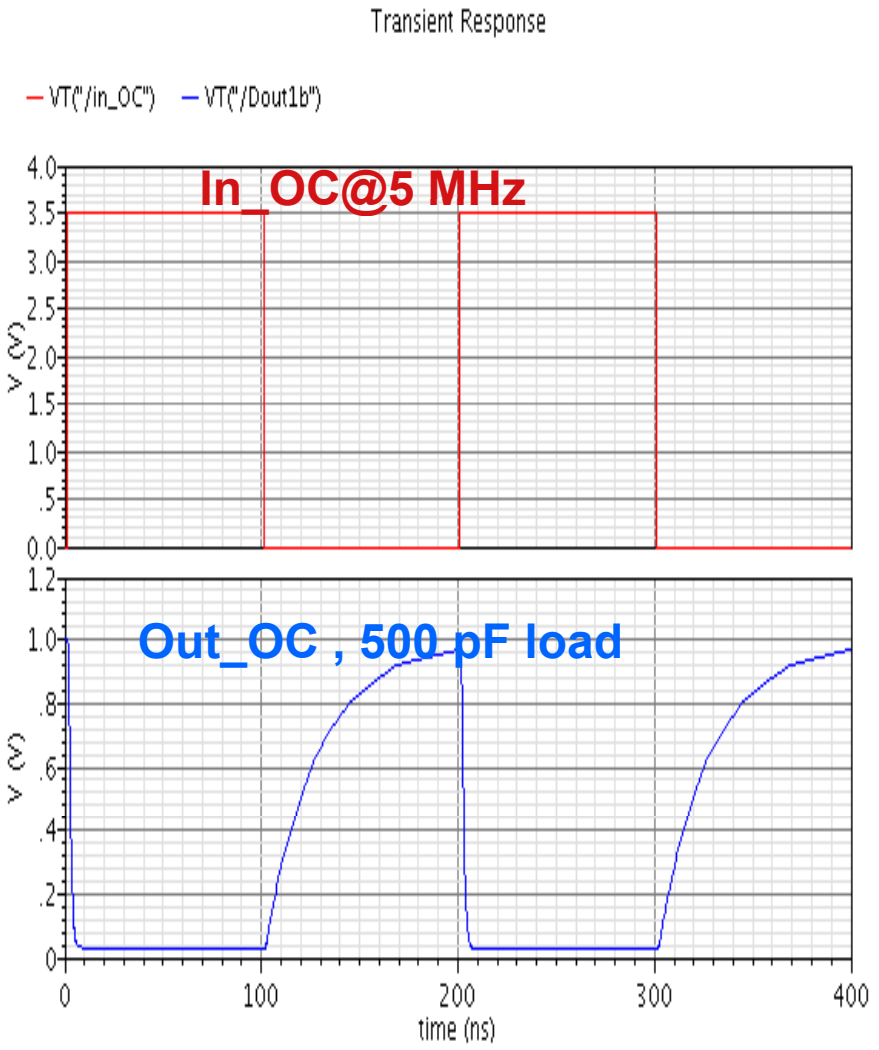




SIMULATION of HR2 OC signals

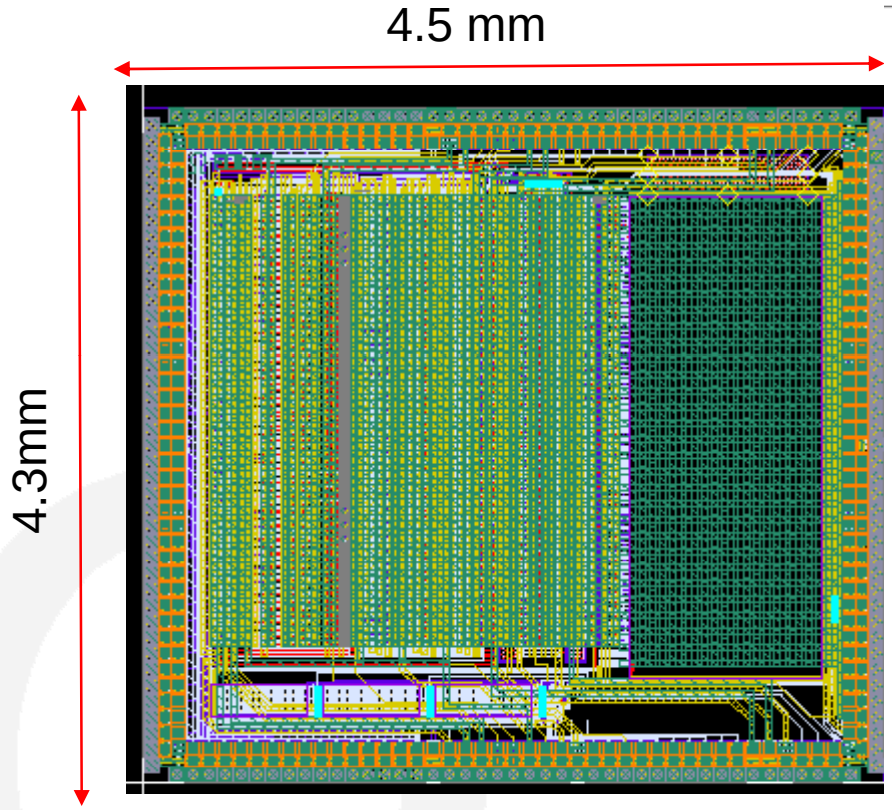
- Hardroc2: change driver transistor

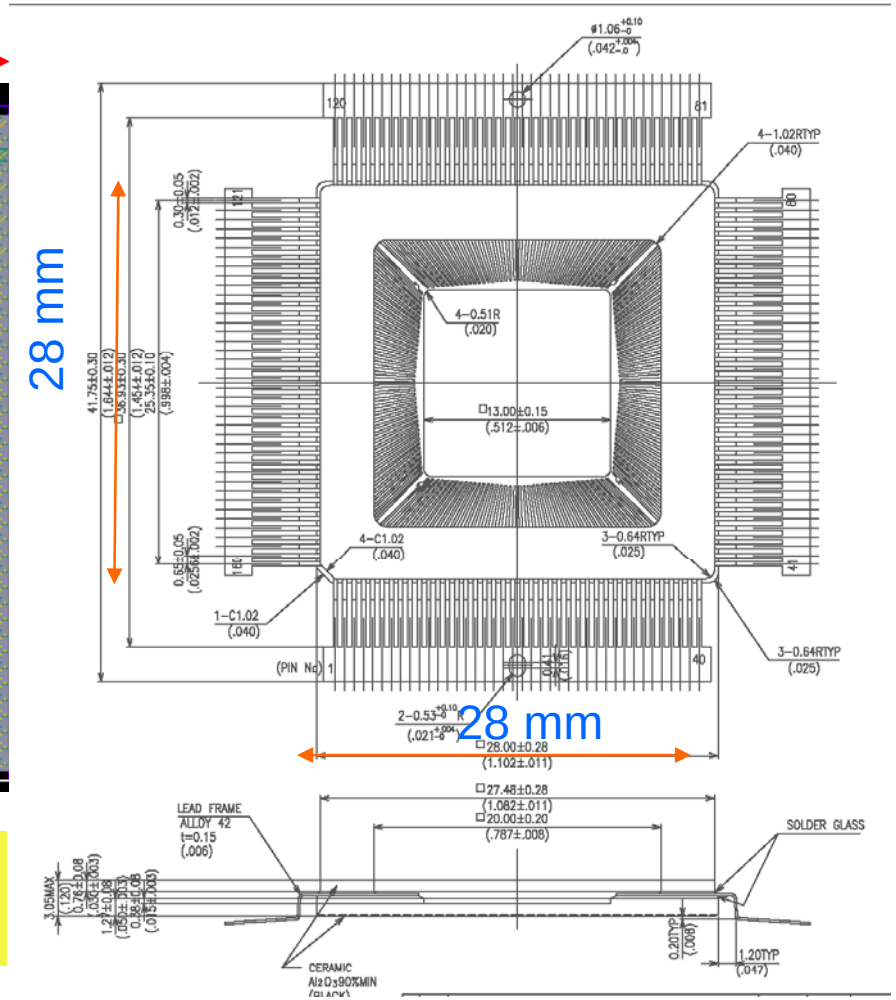




Package: QFP160 (Ceramic QFP176 doesnt seem to exist in Europe)

- 1single row of pads





Ceramic: 4.3 mm
Plastic: 1.4 mm

CONCLUSION

- HaRDROC2 prototyped in june 08
  - Keep HARDROC1 basic architecture and backward compatibility
  - Have 3 very different thresholds
  - Move bonding pads to single row (QFP160 package)
  - + many small changes

  (gain accuracy, power pulsing…)
  - Area : 16 mm2
- HaRDROC2 dies expected mid september