*Si*D Tracker Readout: Context for Cable Design
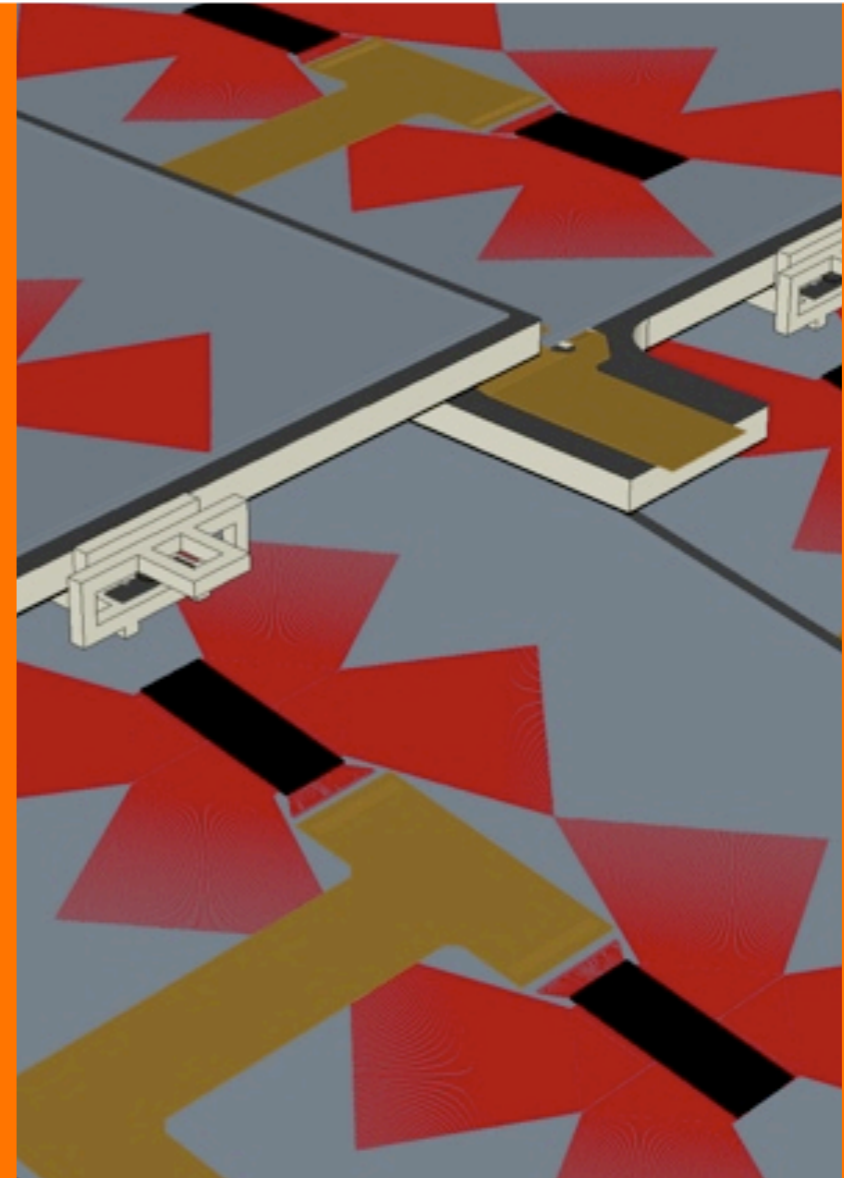
Tim Nelson - SLAC

*Si*D Tracker Pigtail Cable Review

May 29, 2008

Outline

- *Si*D tracker hardware R&D

- The *KPiX* readout concept

- *Si*D barrel tracker sensor prototypes

- Design requirements for readout cable

Key Hardware R&D Driver

Large silicon trackers (ATLAS, CMS) have been too massive for the physics mission of the ILC
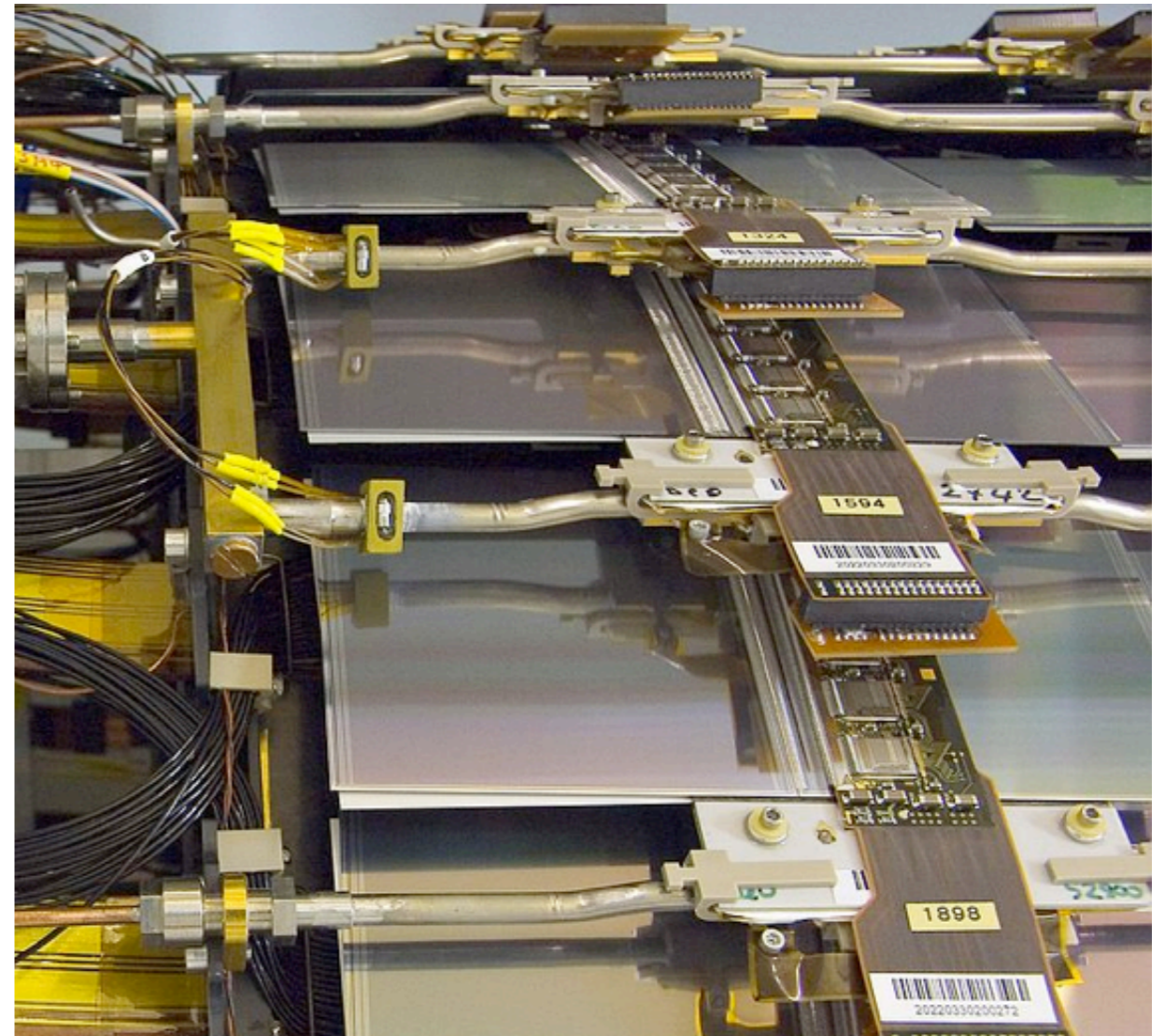
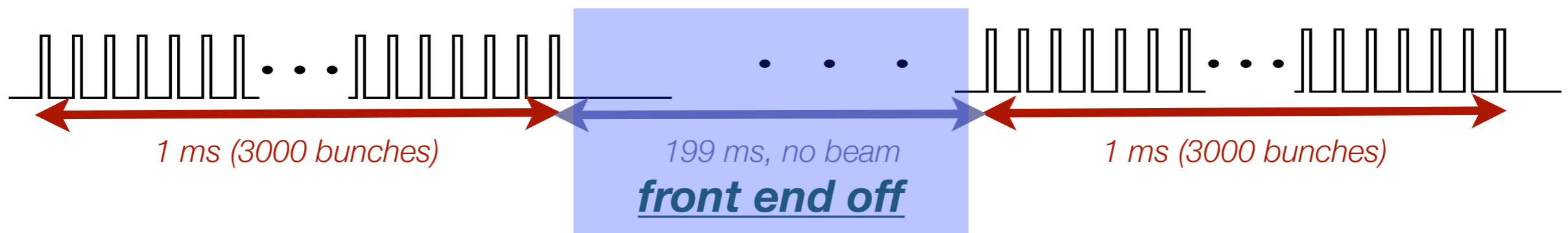**This issue drives nearly all hardware R&D for solid state tracking at the ILC**
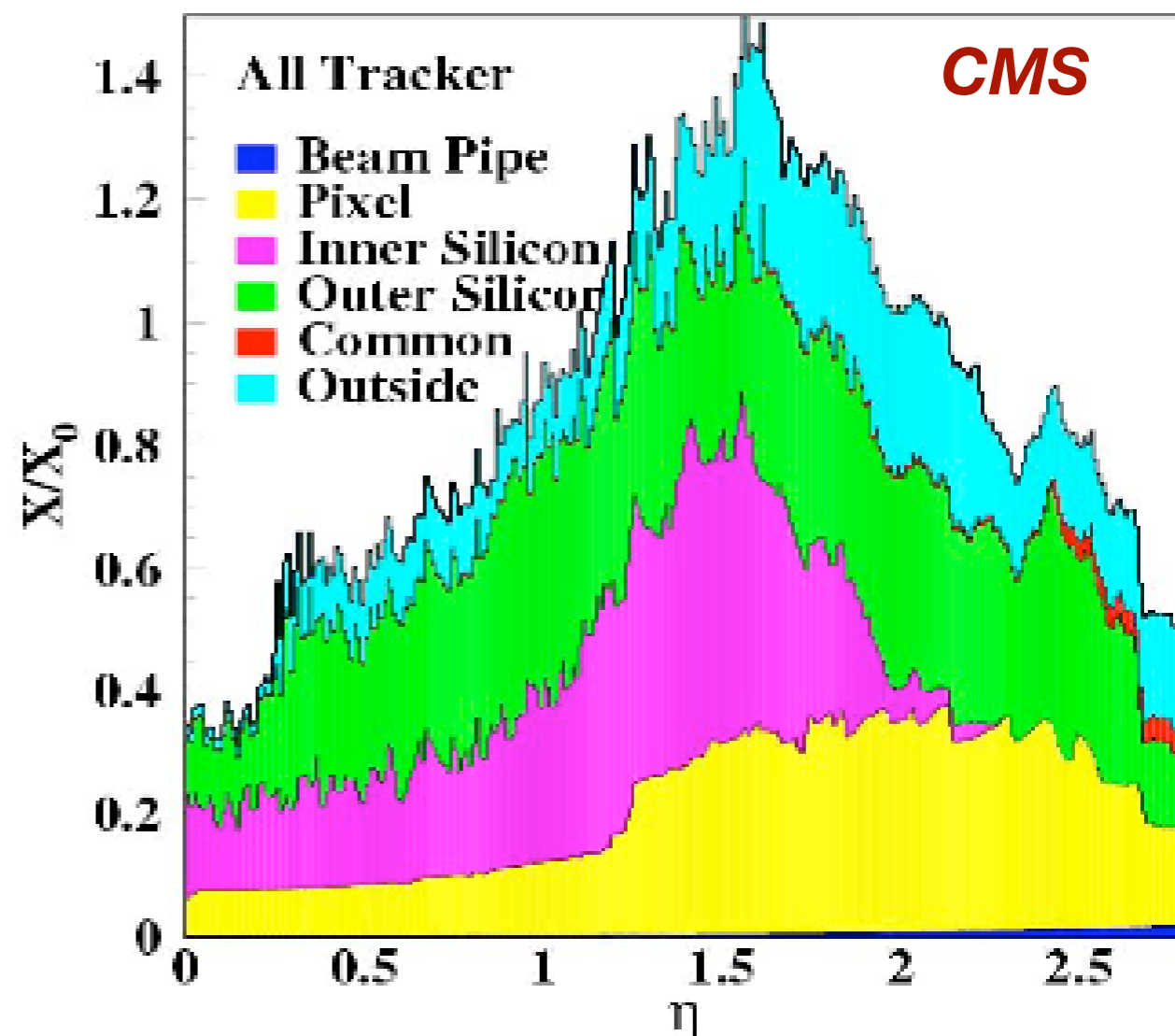
Reducing Material

ATLAS SCT

- Cooling: eliminate

- Readout / Power: reduce

  - Chips

  - Hybrids

  - Cables

- Support: minimize

- Avoid unnecessary redundancy

# The Hows and Whys of ILC Readout Electronics

1 ms (3000 bunches)   *199 ms, no beam*
                            front end off   *1 ms (3000 bunches)*

- Pulsed operation of front end results in ~100X reduction in dissipated power
  - Minimizes services: ***cooling***, cable plant
  - *Many* ILC detector ideas don't work without pulsed power
    - dense Si-W calorimetry
    - low-mass tracking
  - Pulsed power is a common element of many ILC readout efforts
  - The *SiD* realization of this an ASIC called ***KPiX***: achieves 20μW/channel avg.
  - ➡ ***~600W total for 30 million channels: tracker can be gas cooled***

What is Special About K*PiX*?

1 ms (3000 bunches)

199 ms, no beam

1 ms (3000 bunches)

digital section inactive
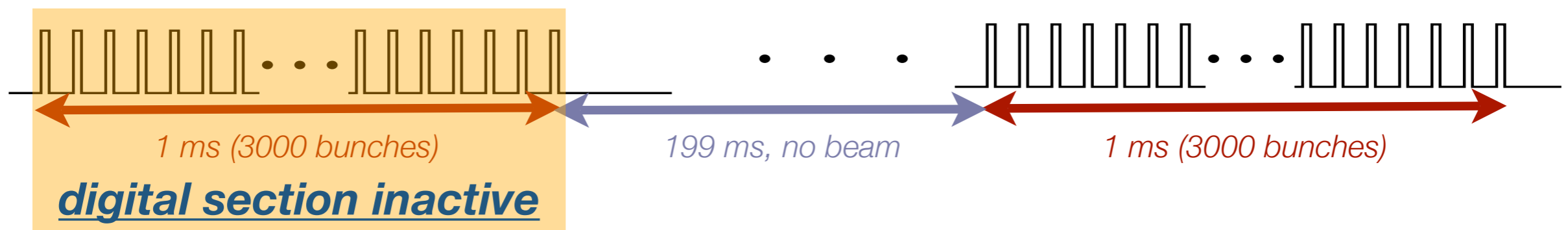
- K*PiX* stores signals acquired during a bunch train in 4 analog buffers

  - hits are time-stamped to individual bunch crossings, reducing background susceptibility

  - digitization and readout occur between bunch trains, minimizing potential for pickup of digital activity on analog front end (only synchronous LVDS clock): allows chip to be more closely coupled to detector electrodes

  - ➡ ***Along with an enormous repertoire of built-in capabilities and flexibility of configuration, KPiX may be bump-bonded directly to sensors***

*Si*D Tracker Module Design

An aggressive approach to reduction of readout material:

- bump-bonded ASIC with double-metal readout: *no hybrid circuit board!*
- Short, single-sensor modules ensure low capacitance ⇒ high signal/noise
  - negligible single-hit inefficiency reduces reliance upon redundancy in layout
  - excellent single-hit resolution provides best possible momentum resolution
  - per-sensor occupancy from physics+noise is small, simplifying pattern recognition

Double-metal readout traces

Readout chips

Power and readout must also be routed on double-metal!

Kapton cable
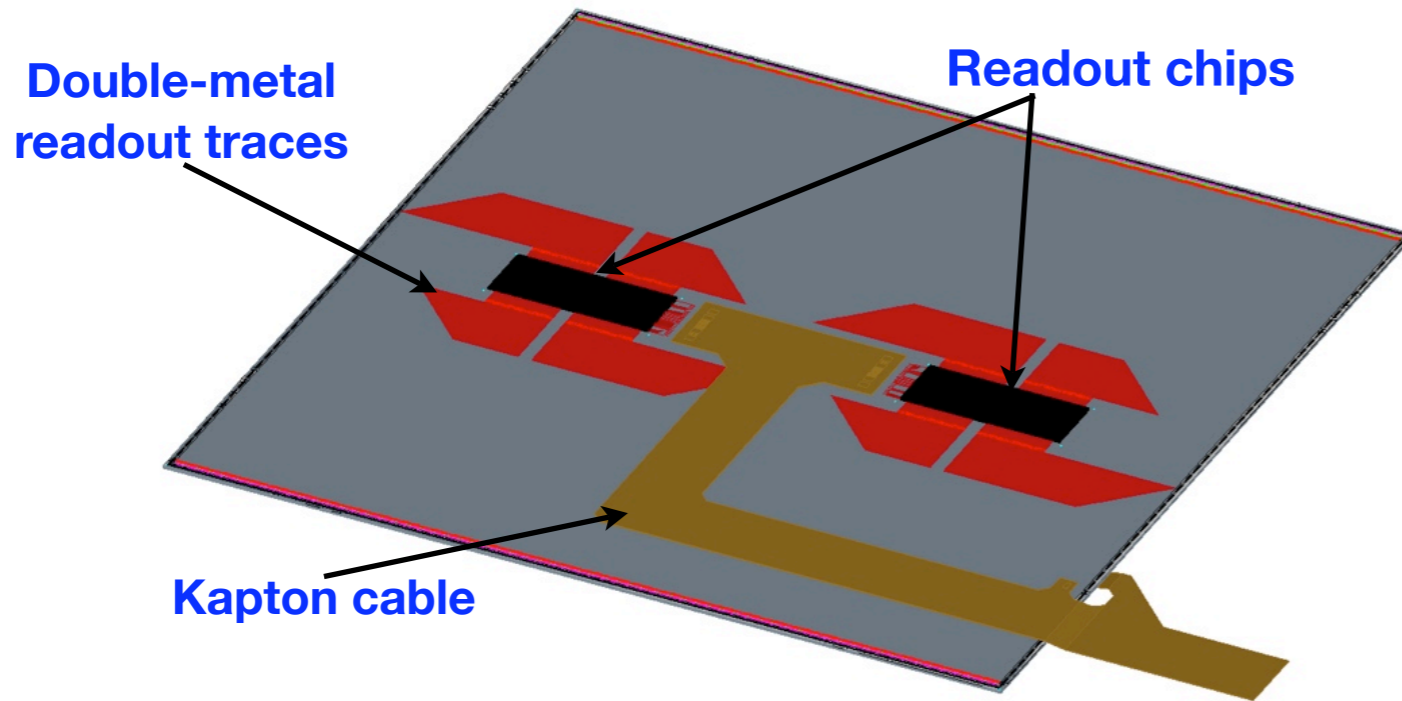
With exception of small surface mount resistors/caps and a mini-connector: this is everything!
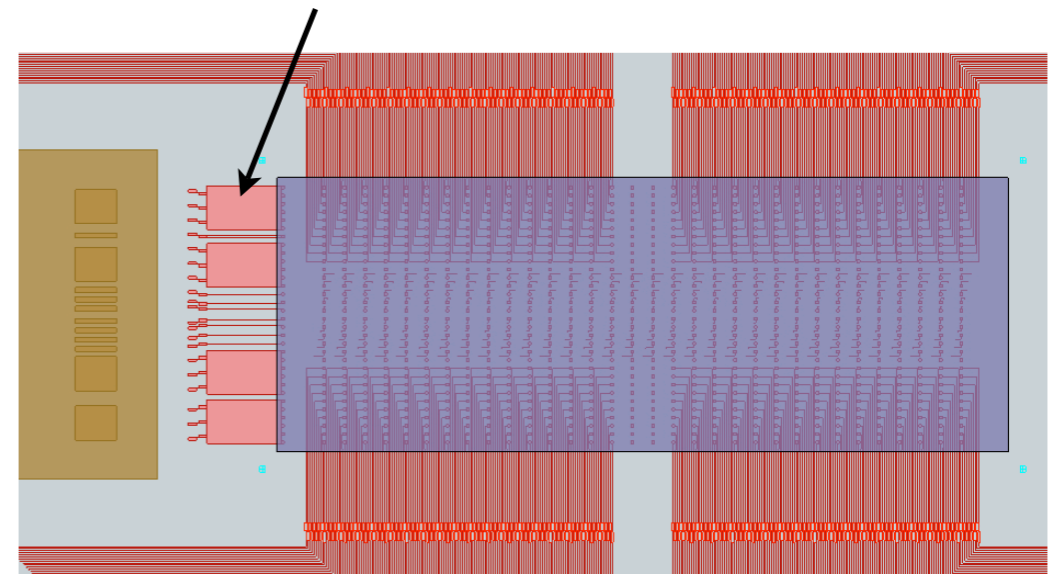
KPiX
SLAC, U. Oregon

- TSMC 0.25μm CMOS
- 32×32 array = 1024 channels
- working with 2×32 prototypes

First versions targeted only at ECal

- dynamic range switching for large charge depositions in ECal (0.05-2000 MIP range)
- bias current servo for DC coupled sensors
- built-in calibration circuitry

Other applications demand additions

- Nearest neighbor logic, high-gain feedback capacitor for tracker
- Polarity selection (GEM readout)
- External trigger for test beam

All features tested and working

KPiX64
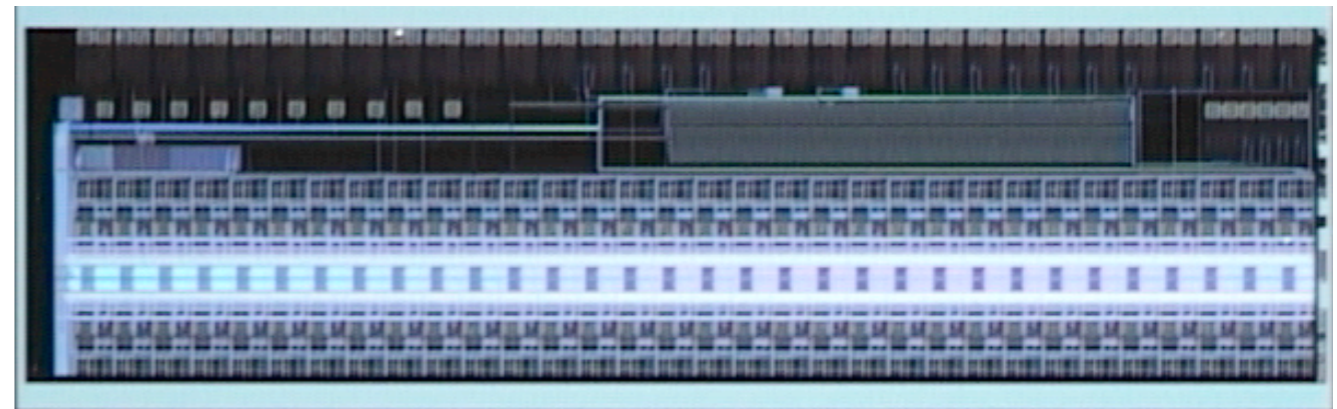
a single cell of KPiX

200 μm

500 μm
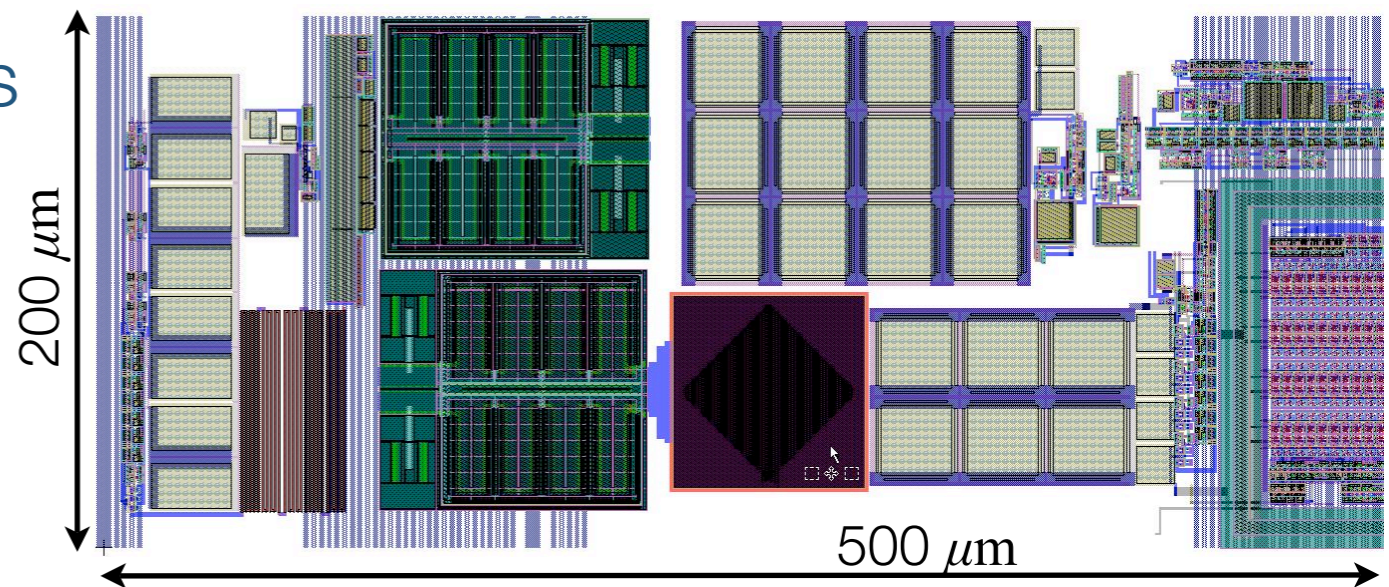
K*iX* Performance

- Each successive generation has added capabilities, improved greatly in performance.

- *KiX*7 is current generation

  - Good gain and threshold uniformity

  - Expected noise achieved in both trigger branch *and* from ADC: ENC = 300+30*C e⁻

  - *No major issues remain!*

Sensors
SLAC, FNAL

- Need ~30,000 sensors: keep it simple, cheap
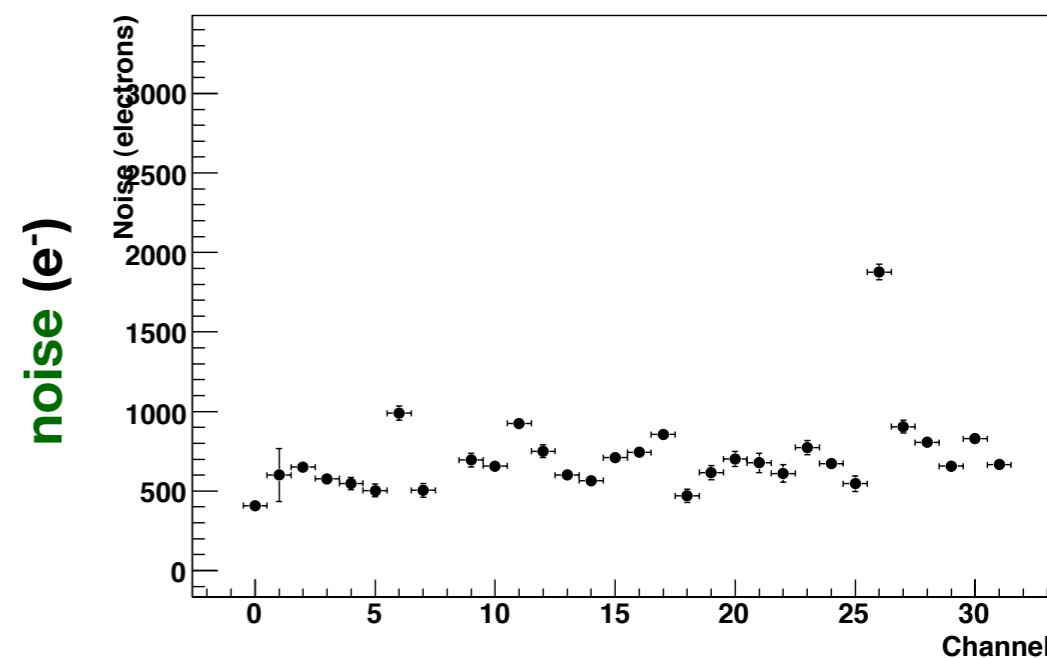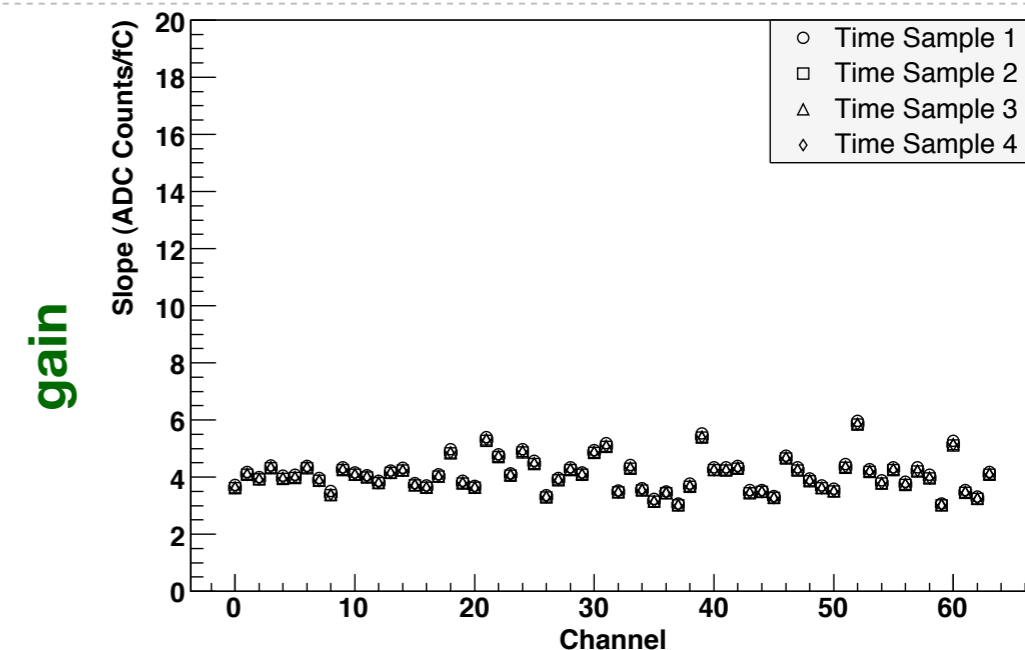 - Single-sided p^+-in-n silicon
  - Largest square sensor from 6" wafer
- Ensure high S/N
  - Short strips with optimized double-metal
- Achieve best resolution for channel count
  - 25 micron sense pitch, 50 micron readout: results in excellent resolution
- Minimize potential problems with double-metal power/readout scheme
  - Lowest possible power/ground impedance
  - Minimize coupling between LVDS clock traces and underlying strips

readout(sense) pitch (μm)

simulation, benchmarked against test beam

50 (50)

50 (25)

25 (25)

Resolution (μm)

Signal/Noise

Double-metal Optimization

Signal traces:

- HPK double-metal traces down to 2μm width

- balance capacitance against series resistance, minimize variations among channels

- Layout began with previously-learned lessons learned from others, proceeded through a great deal of ANSYS modeling

➡ $8(9)\mu$m implant(sense strip) width, 4μm double-metal readout width:

- C=14-18 pF for 95% channels, 20 pF max

- R < 350 Ω for all channels

➡ S/N = 20-25 with K*PiX*

The model for case 2 is plotted in Fig.2. There are 12 conductors. The capacitance matrices are listed on next page.

Fig.2 case (2) model

Conductors 8, 10 and 12 are 1 X 4
Other conductors are 1 X 8.

Thickness of silicon dioxide above conductor 8, 10 and 12 is 0.5, beneath it is x = 0.9 or x = 3.0.

Thickness of silicon nitride is 0.5

Capacitance matrix for case (3)
x= 0.9 micron phi = 26.3 degree
         2/5/07
conductor length is 1000 micron, the unit of capacitance is pF

```
0.023018
7.49E-03   2.02E-02
2.32E-03   7.48E-03   2.30E-02
8.88E-03   8.75E-03   8.68E-03   4.79E-03
8.11E-03   8.01E-03   8.14E-03   4.34E-04   2.66E-03
8.74E-03   8.79E-03   8.87E-03   1.44E-04   4.33E-04   4.74E-03
8.69E-03   8.16E-03   7.84E-03   1.29E+00   1.39E-03   5.57E-04   2.57E-02
1.17E-02   1.15E-02   1.14E-02   9.36E-03   8.57E-03   8.67E-04   4.39E-02   1.91E-02
5.18E-03   5.11E-03   5.19E-03   1.44E-03   1.29E+00   1.43E-03   8.64E-03   4.02E-02   1.54E-02
1.15E-02   1.15E-02   1.17E-02   8.70E-04   8.57E-03   9.33E-03   4.73E-03   9.64E-03   4.02E-02   1.91E-02
7.82E-03   8.14E-03   8.68E-03   5.60E-04   1.39E-03   1.30E+00   3.20E-03   4.73E-03   8.64E-03   4.39E-02   2.57E-02
```


5.44E+00

The length of conductors are 1000 μ

Aluminum

Doped silicon

Model-26, case 3, x = 0.9, phi = 26.3

Double-metal Optimization

Power/readout traces:

- Want shortest, widest traces for power, ground: 0.08 Ω/pair (round-trip spec is 1Ω max.)

- Narrow LVDS clock traces ⊥ sense strips

- integration over odd number of clock edges will introduce ~3500 e- pedestal shift on channels underneath bond pads from capacitive coupling

  ➡ one clock per BX?

  ➡ clock rate faster than shaper response?

- somewhat smaller is shift due to voltage fluctuations on power and ground traces if assumed to be completely unbalanced

Simulations cannot be trusted at this level: we need to try it!

LVDS clock pair{
4 micron strips
60 micron pads

DGND

DVDD
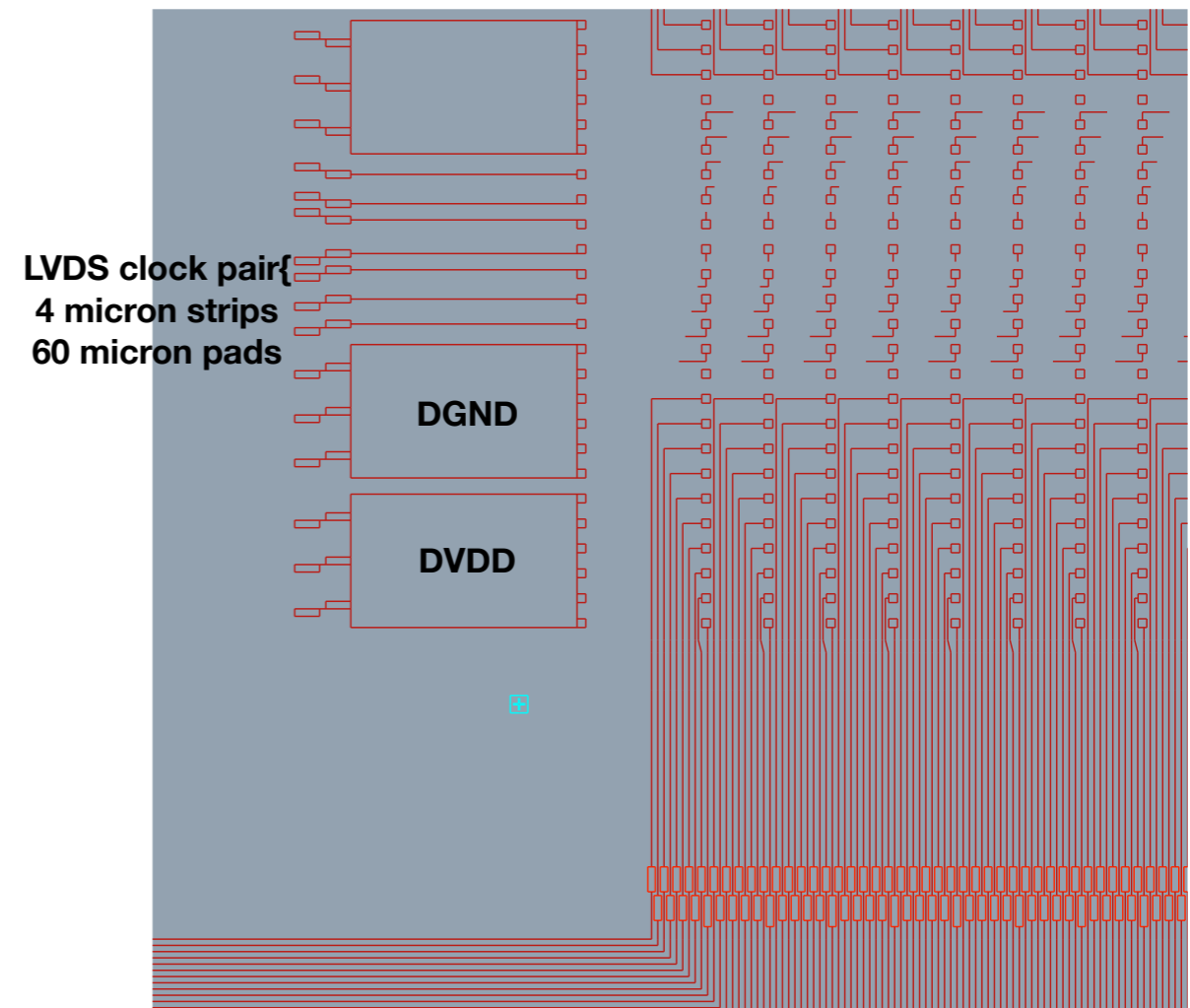
HPK Prototype Sensors

- Received sensors from HPK on March 30.

  - 20 full-sized tracking sensors for module prototypes with full-sized *KPiX*

  - 40 smaller sensors for testing double-metal readout with smaller *KPiX* variants

- Quality excellent: bad channels <1/10000 (!!)

- Appears that there were no yield problems

- Will be tested in the coming weeks
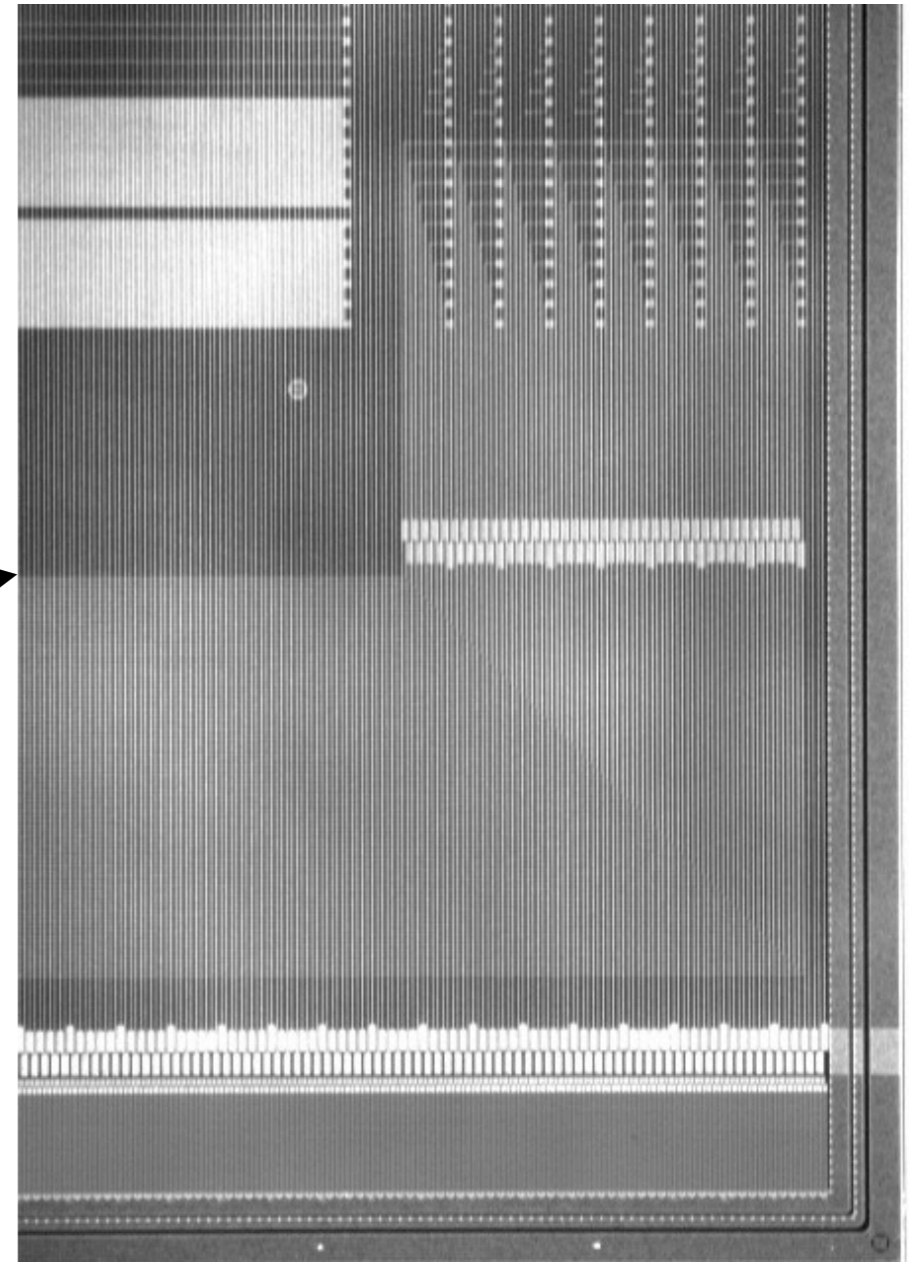
KPiX Bump Bonding
UC Davis
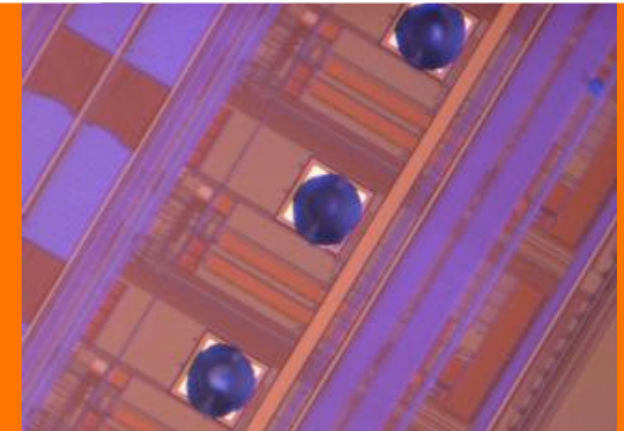
Bump-bonding is a critical process for our designs

- At these pitches, gold-stud bumping becomes feasible, especially attractive for small-run R&D

- First attempts by Palomar Technologies on KPiX-5 and ECal prototype sensors *somewhat* successful

- Only 96% yield on first two test chips

- Corrosion problem between epoxy used for making final bond and Al pads: at worst we will have to add Ti-W as one would for indium bumping
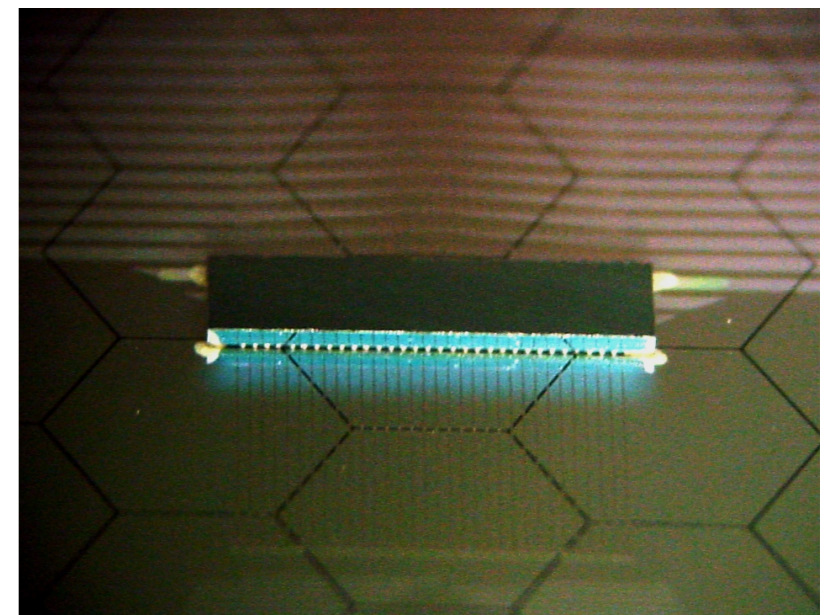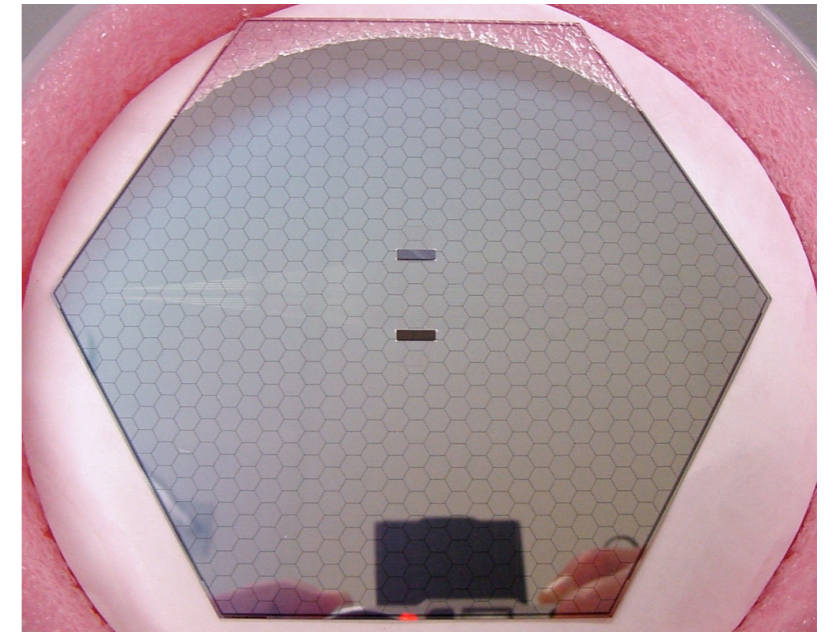
Encouraging progress for an unfamiliar technique: anticipate using this process for prototype modules

Pigtail Cable
UNM

- Pigtail glues to sensor, wirebonds to double-metal, bias tab at edge

- Connects to straight extension cable running to ends of cylinders (up to 1.7m)

- ¼-ounce copper on $50\mu m$ Kapton

  - 2 power+ground pairs

  - 8 narrow control/readout lines

  - HV pair for sensor bias

  - ➡ cable width 8mm
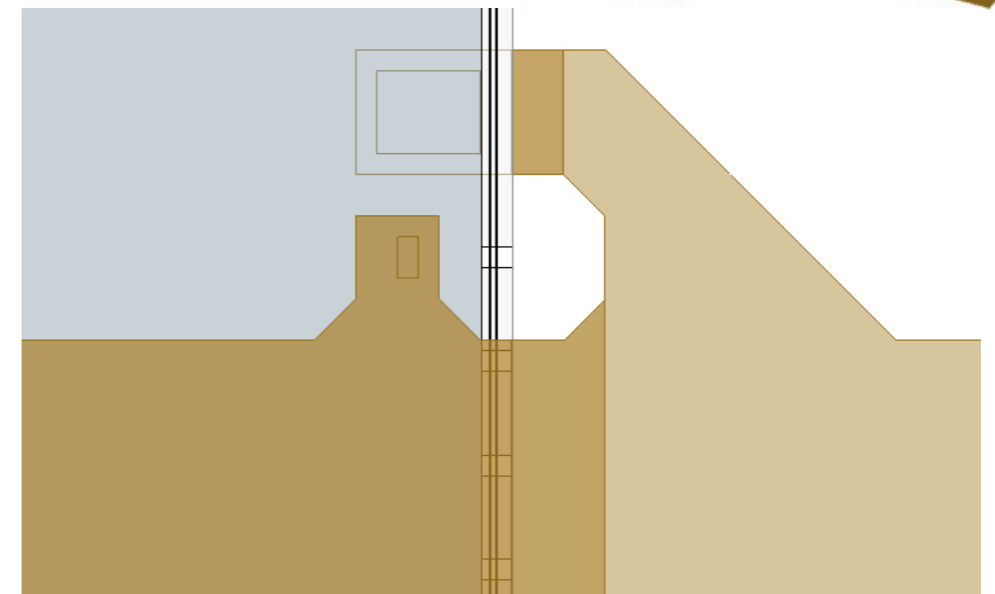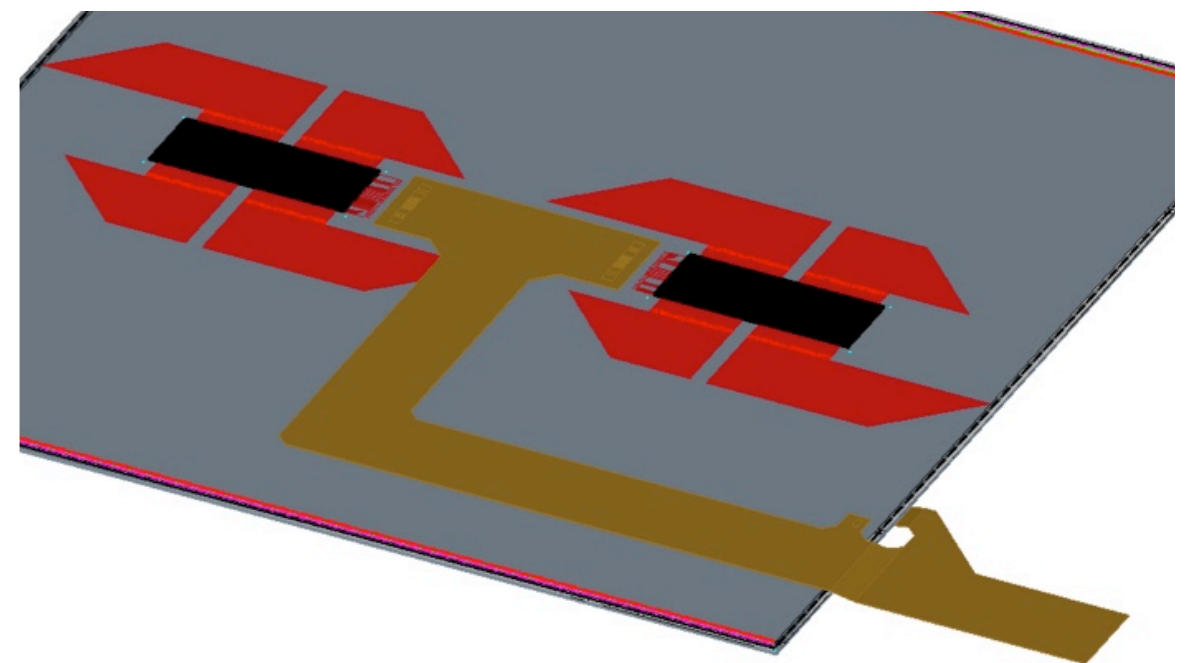
Pigtail Details

- Large pads for wirebonding
- Important to consider details that minimize material
  - Meshed ground plane
  - Thinner Kapton?
- Important to design as robustly as possible
  - Connectors
  - Radiused inside corners?
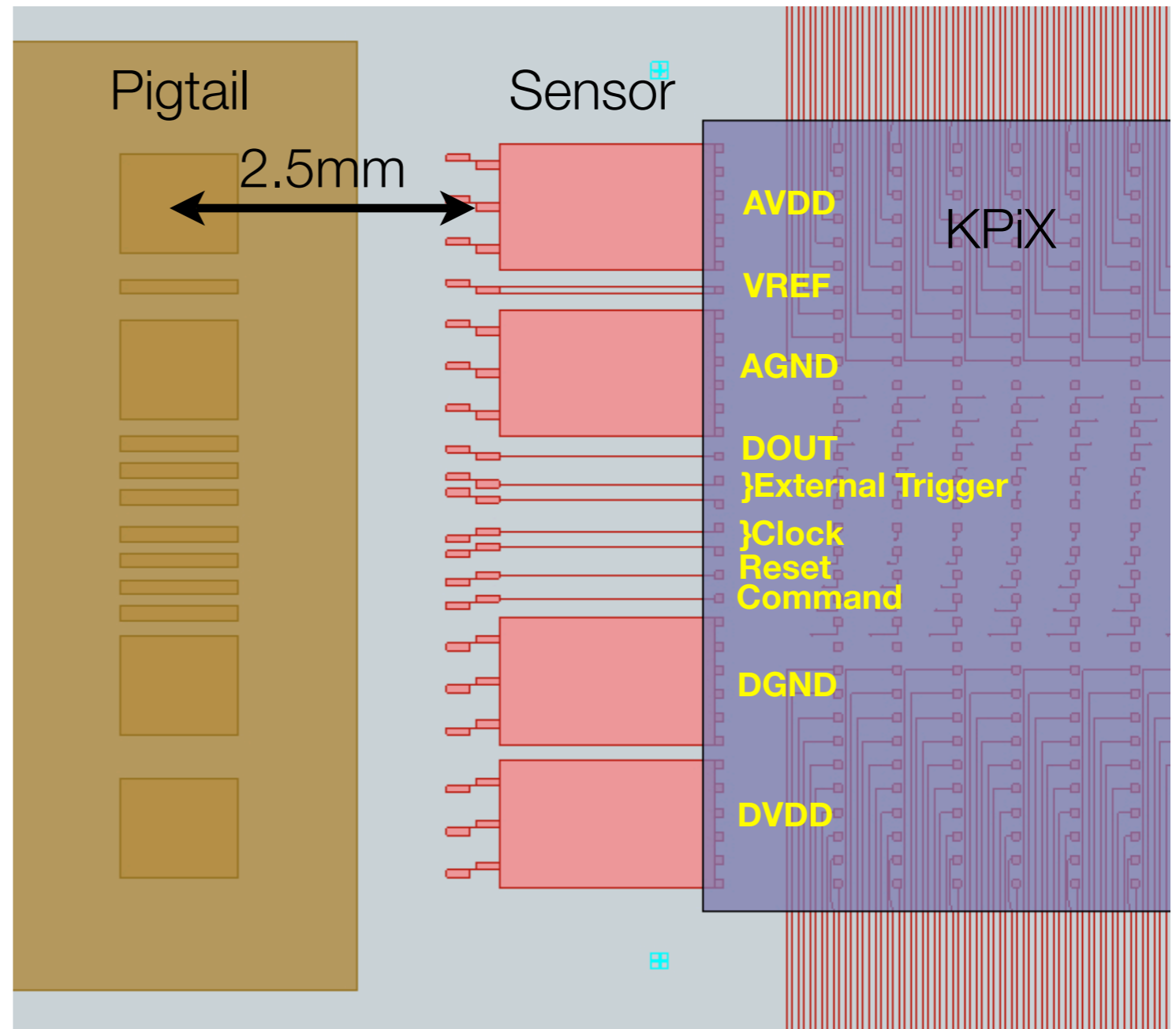
Missing Details

- Critical to define surface mount components required for bypassing, termination

- Dieter Freytag drew up a "maximal" scheme: not clear that all of these components will be required

- At the prototyping stage, we want to have all options available for testing different configurations

- Provisions for these components are a key subject to be reviewed: input from Dieter is necessary
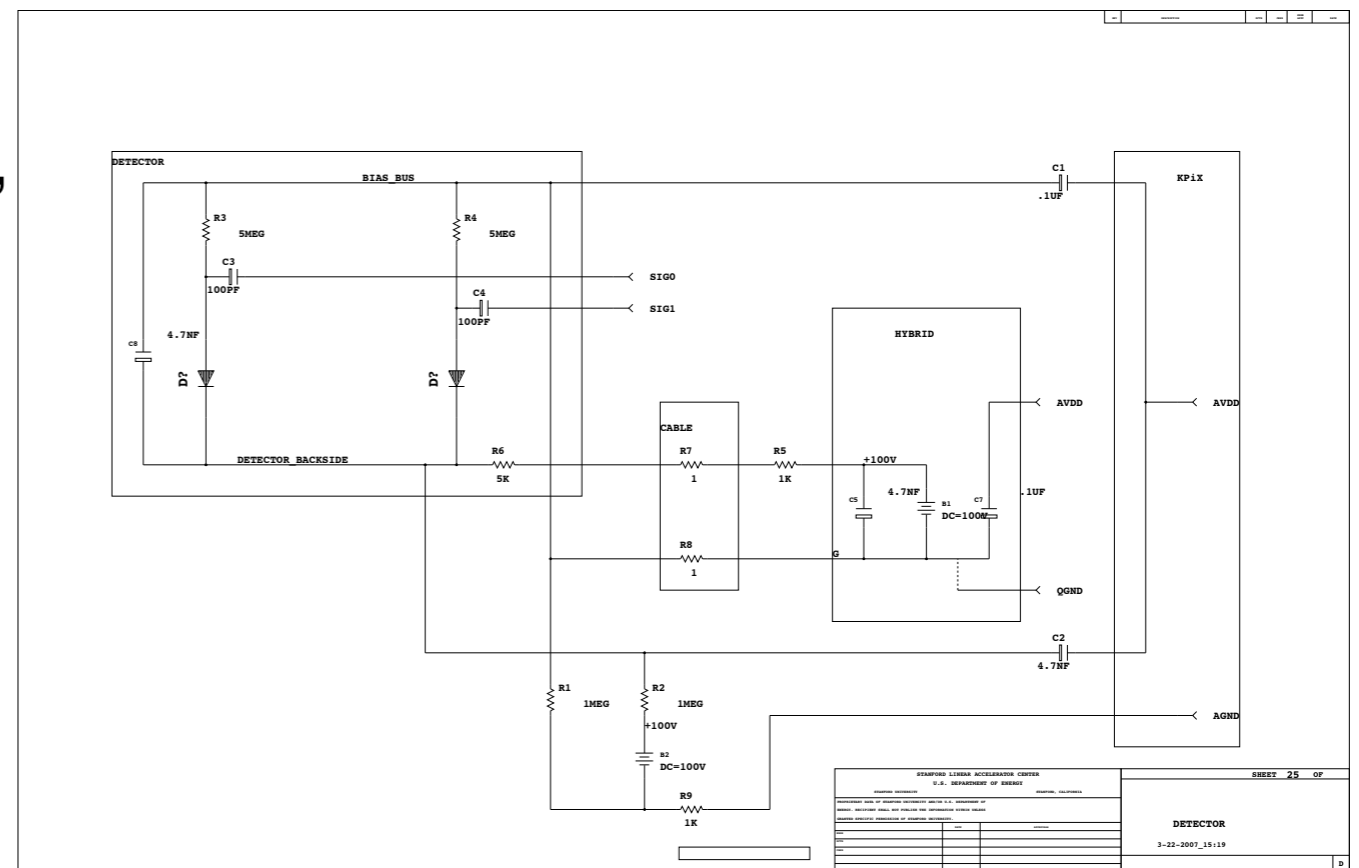
Summary

- The pigtail is a rather simple item mechanically, only a few questions
  - Thickness
  - Nature of ground plane
  - Robustness of connector and sharp inside corners
- The key details are electrical
  - How are HVGND/AGND/DGND connected?
  - How are signals terminated?
  - How does bypassing work?

➡ These are *prototypes* intended for R&D on this readout scheme: we would prefer as much flexibility in configuration as we can have without creating fundamental problems.