IN2P3

Omega

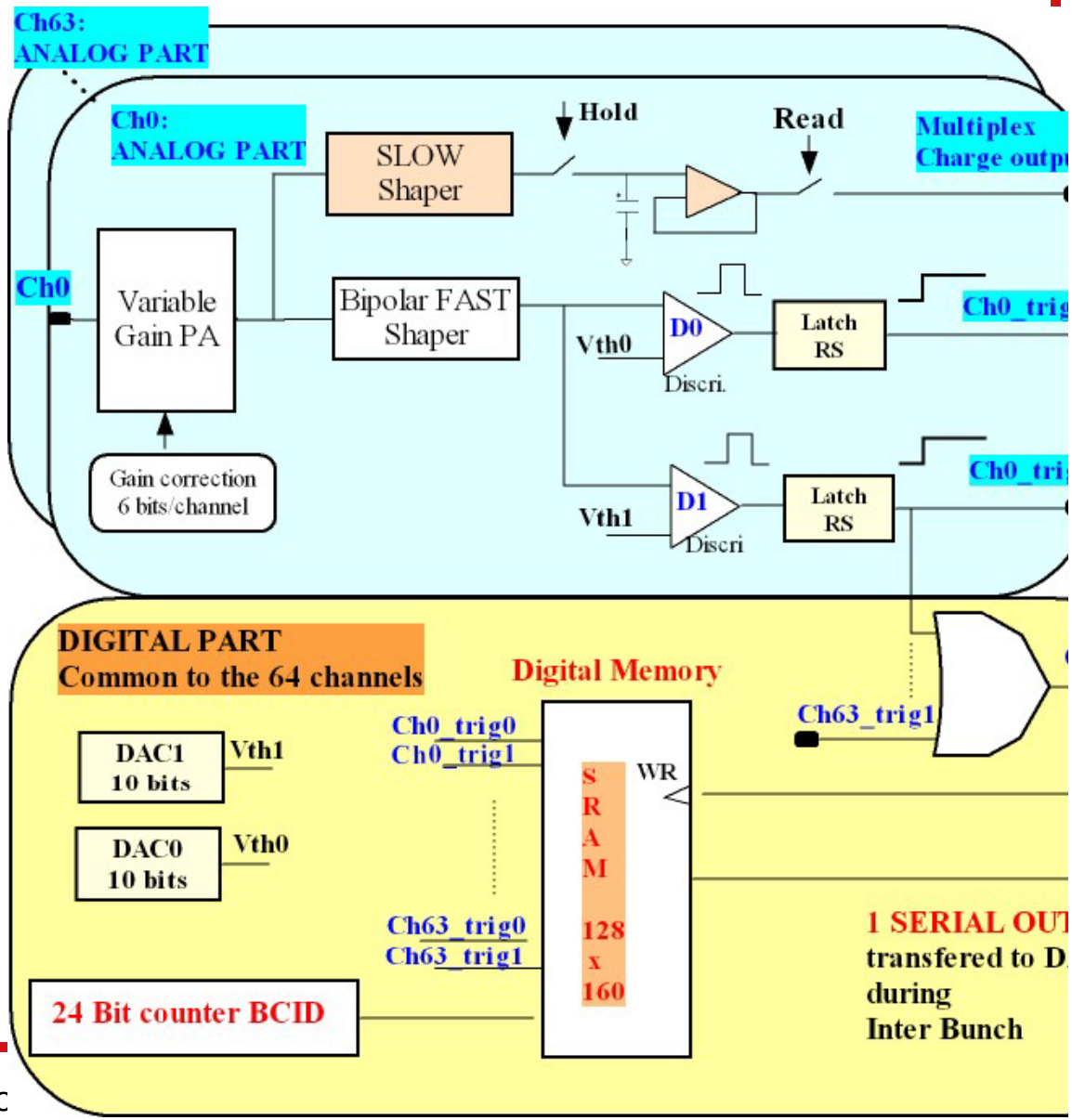
HARDROC2

June 13rd, 2008

Orsay MicroElectronic Group Associated

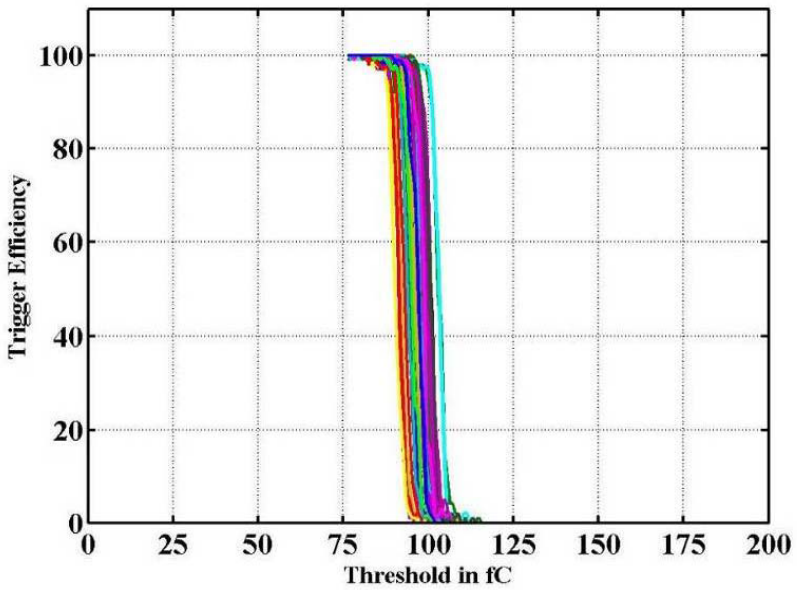
HaRDROC1 architecture

- Variable gain (6bits) current preamps (50ohm input)
- One multiplexed analog output (12bit)
- Auto-trigger on ½ MIP
- Store all channels and BCID for every hit. Depth = 128 bits
- Data format : 128(depth)*[2bit*64ch +24bit(BCID)+8bit(Header)] = 20kbits
- Power dissipation : 1.5 mW/ch (unpulsed)-> 15µW with 1% cycle
- Large flexibility via >500 slow control settings

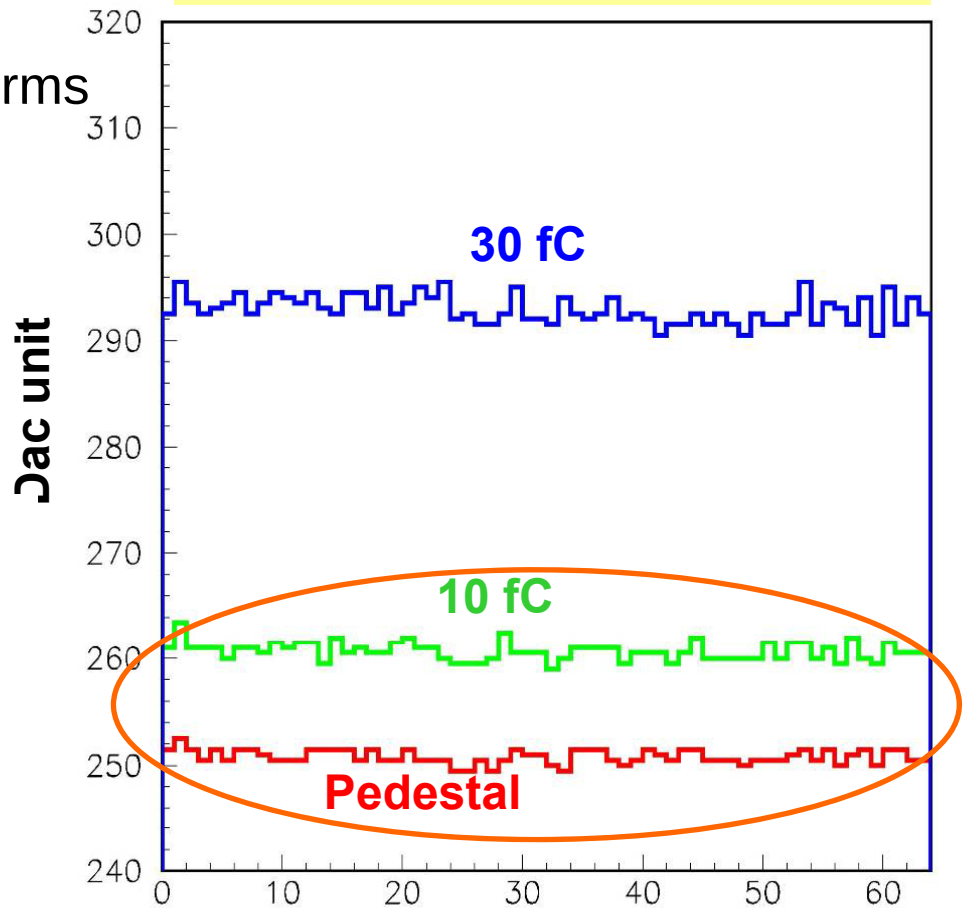


HARDROC1: S-curves of 64 channels measurement

- 10 bit DAC for threshold,
- Noise ~ 1 UDAC (2mV)
- Pedestal dispersion : 0.4 UDAC rms
- Gain dispersion 3% rms
- Crosstalk : < 2%

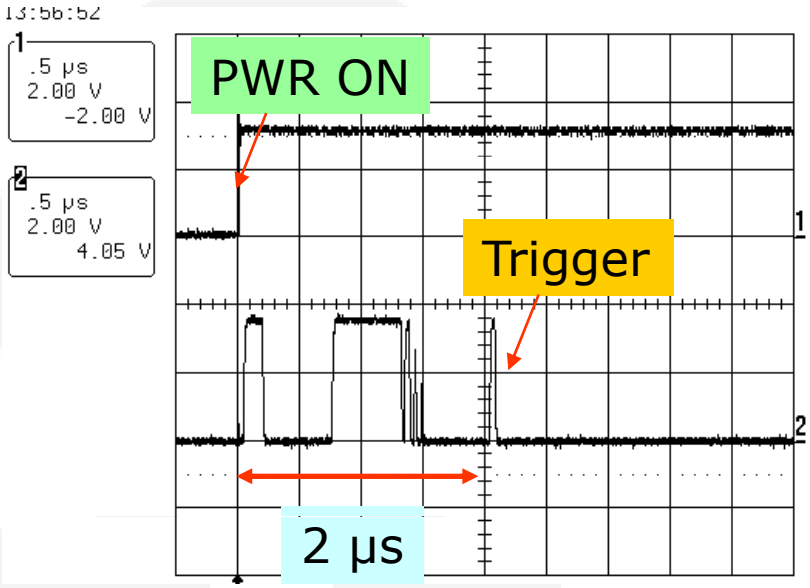


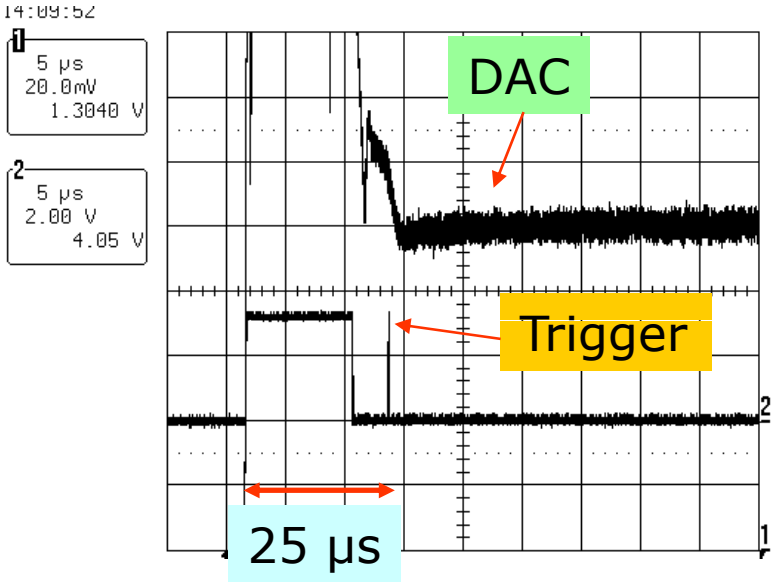
50% trigger versus channel number



HARDROC1: Power pulsing measurement

- PWR ON: ILC like (1ms,199ms)
- All decoupling capacitors removed : difficult compromise between noise filtering and fast awake time
- Awake time :
  - Analog part = 2 us
  - DAC part = 25 us
- 0.5 % duty cycle achieved, now to be tested at system level



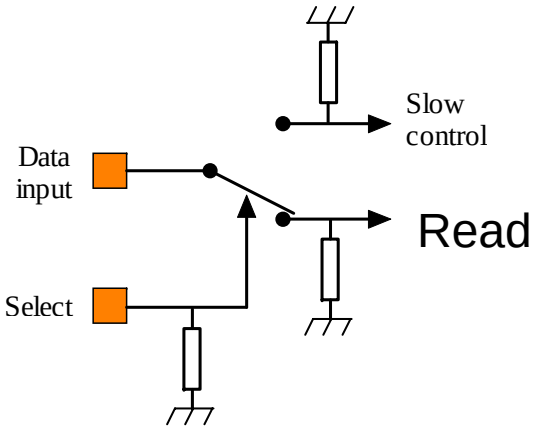


DESIGN of HARDROC2

- Hardroc2 submitted: mid june 08

- **ANALOG PART:**
  - **Dynamic range extension**
    - Gain correction: 8 bits instead of 6
    - 3 shapers and 3 thresholds (=> 3 DACs):
      - 10 fC, 100fC, 1pC (megas)
      - 100fC, 1pC, 10pC (GRPC)
    - Encoder: trig0<i>, trig1<i>, trig2<i> outputs encoded to encod0<i> and encod1<i>
    - **Bandgap redesigned**

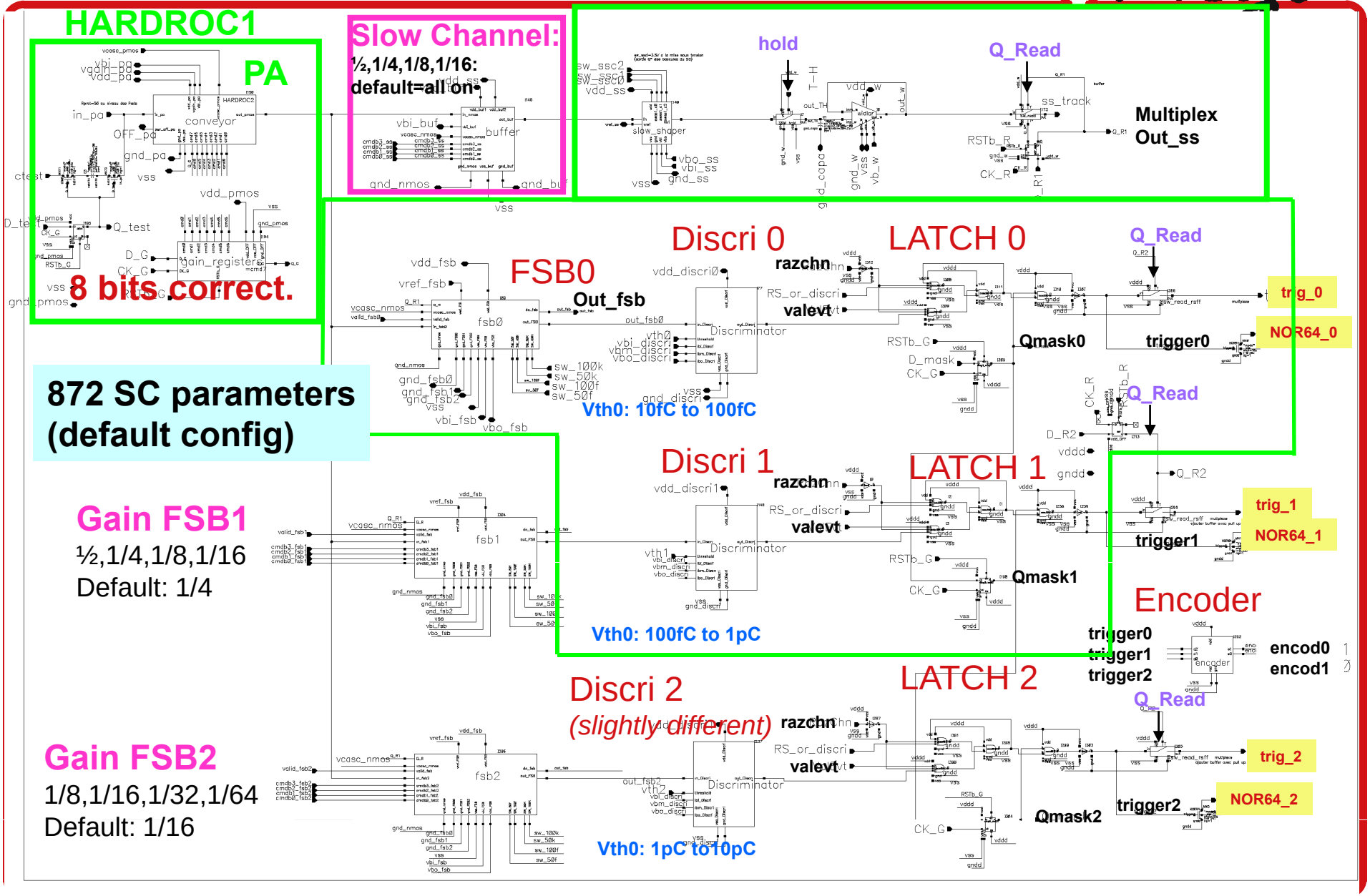
- **DIGITAL PART:**
  - Correction of the minor bugs of HR1:
  - mask, memory pointer: dummy frame
  - Shift registers improvements (multiplex, default, extra FF)
  - Bypass on critical signals



- **Power consumption:**
  - Bandgap + ref Voltages + master I: power pulsed
  - POD module (power budget)

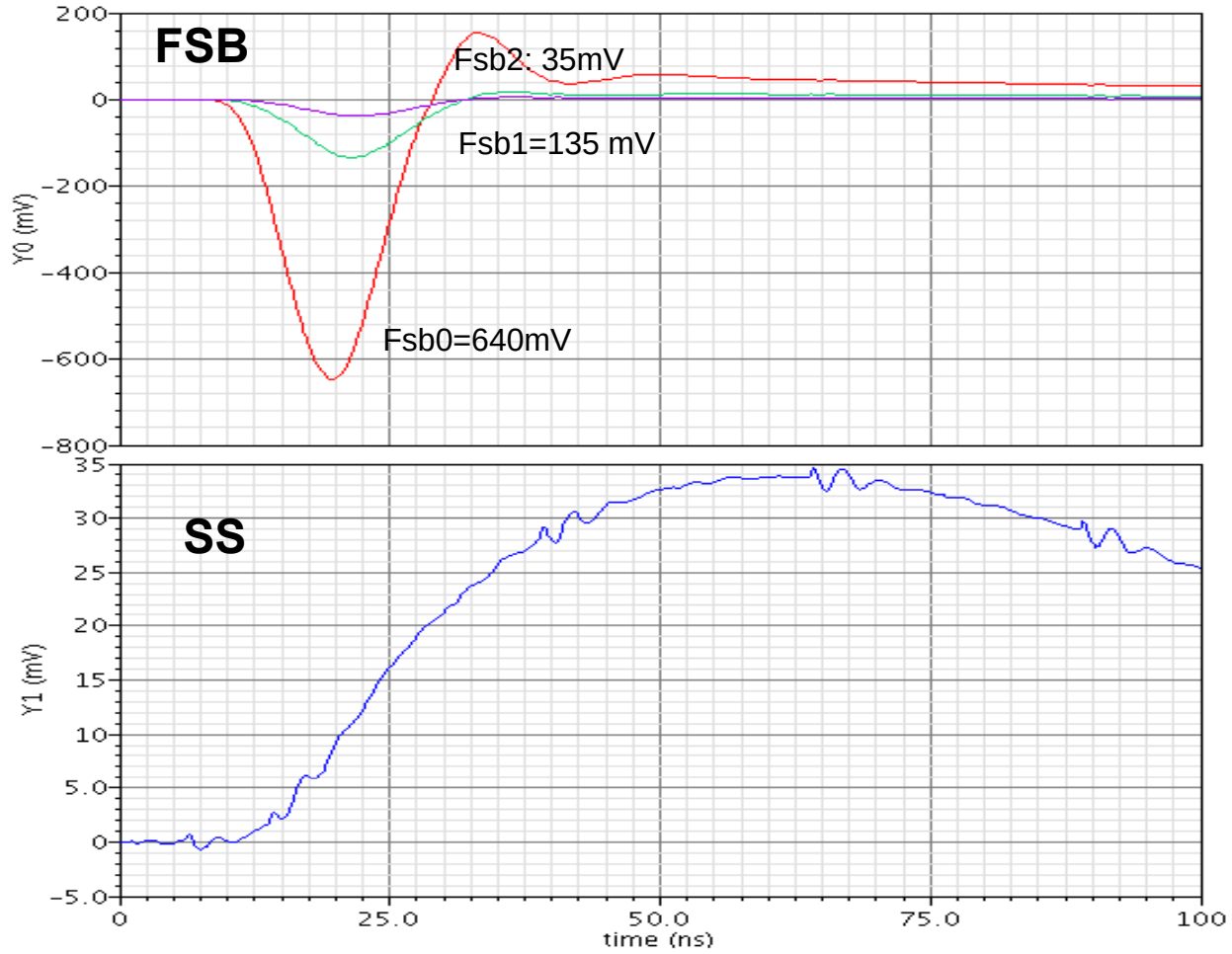
- **HARDROC2= HARDROC1 + modifs**
  - ⇒ **HARDROC1= BACKUP**

HARDROC2: analog part



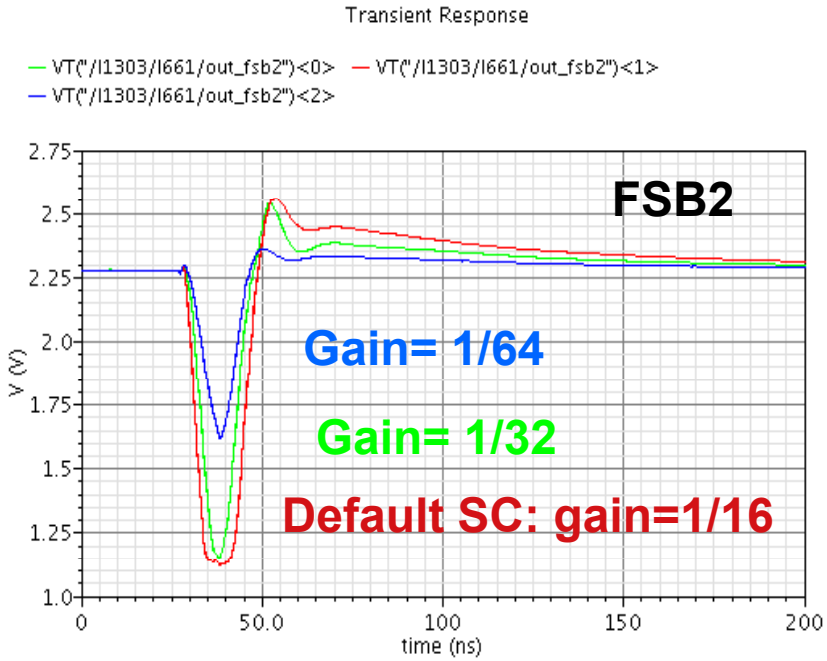
SIMULATIONS: FSB and SS

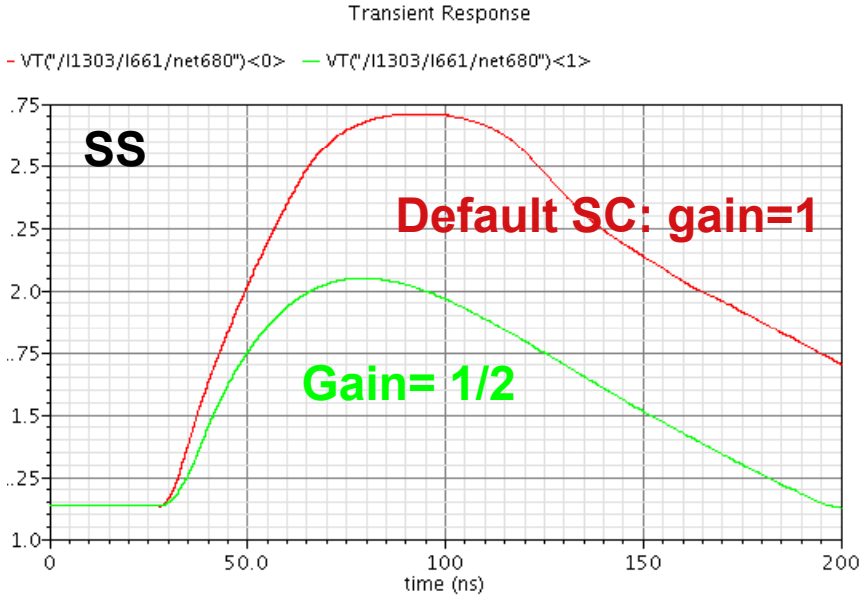
Default SC configuration and Qinj=100 fC



SIMULATIONS: FSB and SS

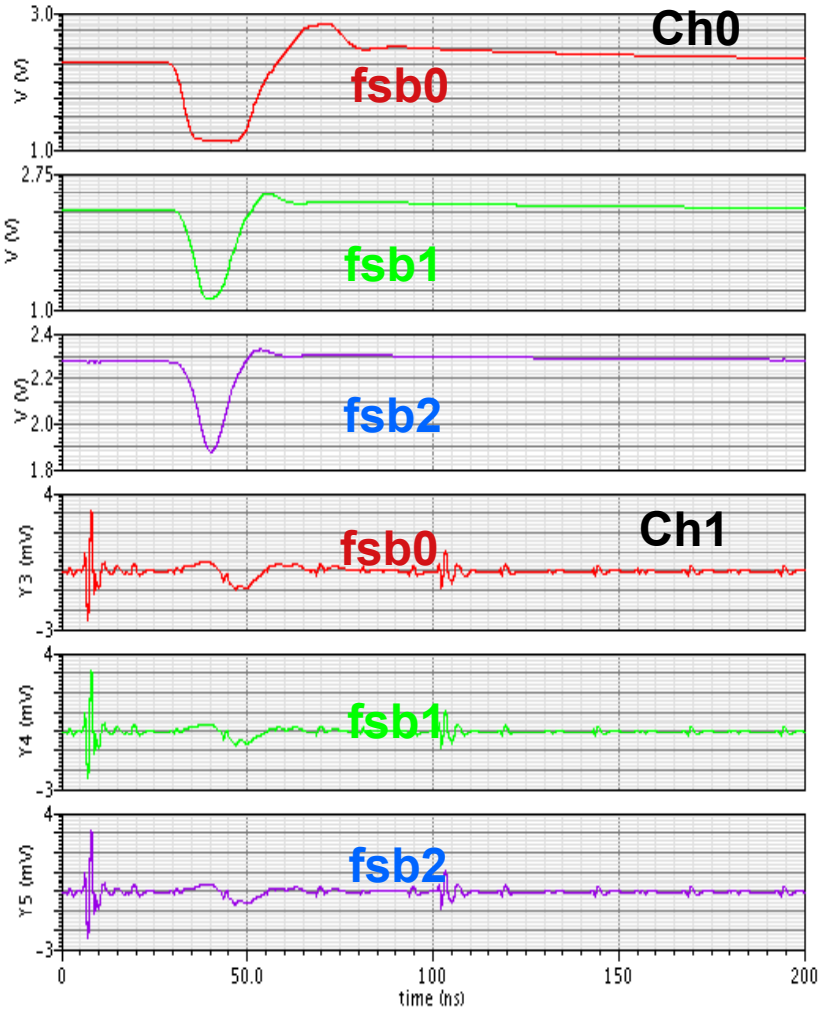
Different SC configurations (gain)
FSB2 and SS
Qinj=10 pC



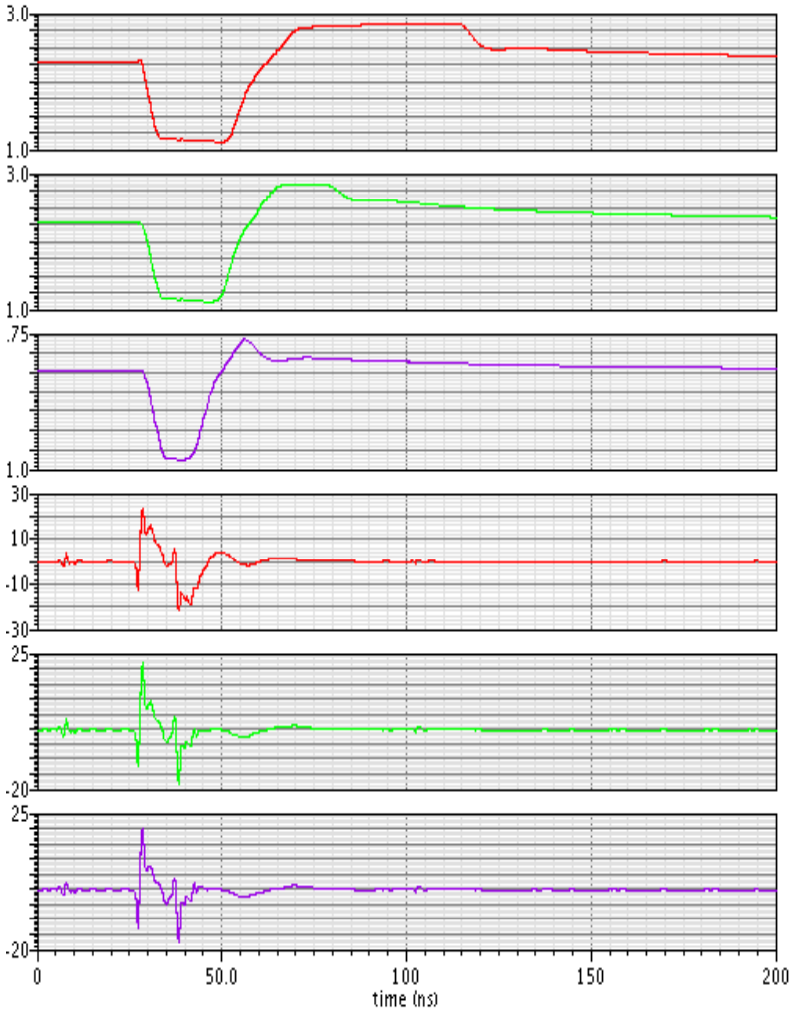


SIMULATIONS: Xtk (1pC and 10 pC)

Qinj in Ch0= 1pC

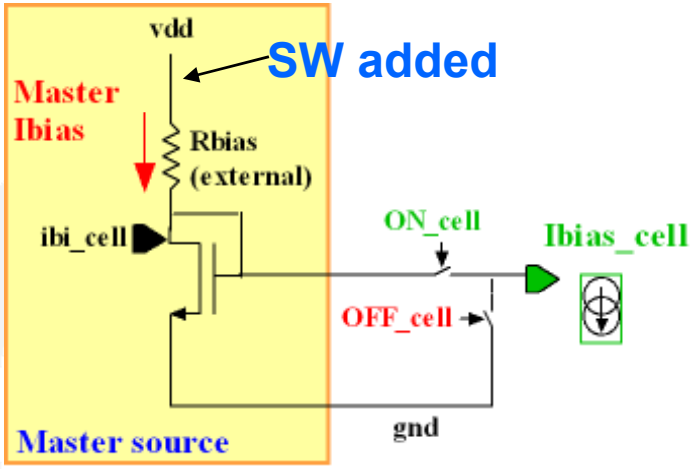


Qinj in Ch0= 10pC



POWER PULSING: simulation of HR2

- Maximum power available:
  - 10 µW/ channel with 0.5% duty cycle ie 640µW/3.5V=180 µA for the entire chip
  - HR2: 95 µA (HR1: 125 µA)
  - OFF= Ibias _cell switched off during interbunch:

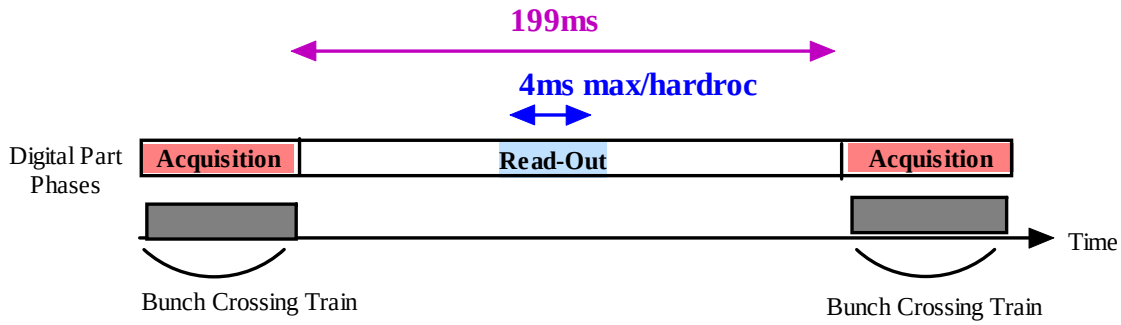


64 channels	ON	OFF
Vdd_pa	2.2mA	0
Vdd_fsb	5 mA	0
Vdd_d0,d1,d2	9mA	1.2 µA
Vdd_bandgap	1.3 mA	0
Vdd_dac	1mA	0
vddd	400µA	1.6µA
Vddd2	2.6mA	0 (with POD)
Total (noPP)	19 mA	3µA
Total with 0.5% PP	95 µA	3 µA

Hardroc2: SW added to switch off all the master Ibias, Vref, V_BG…

Power On digital (POD): Timing aspect 1/2

- ILC based on a 200 ms bunch crossing period



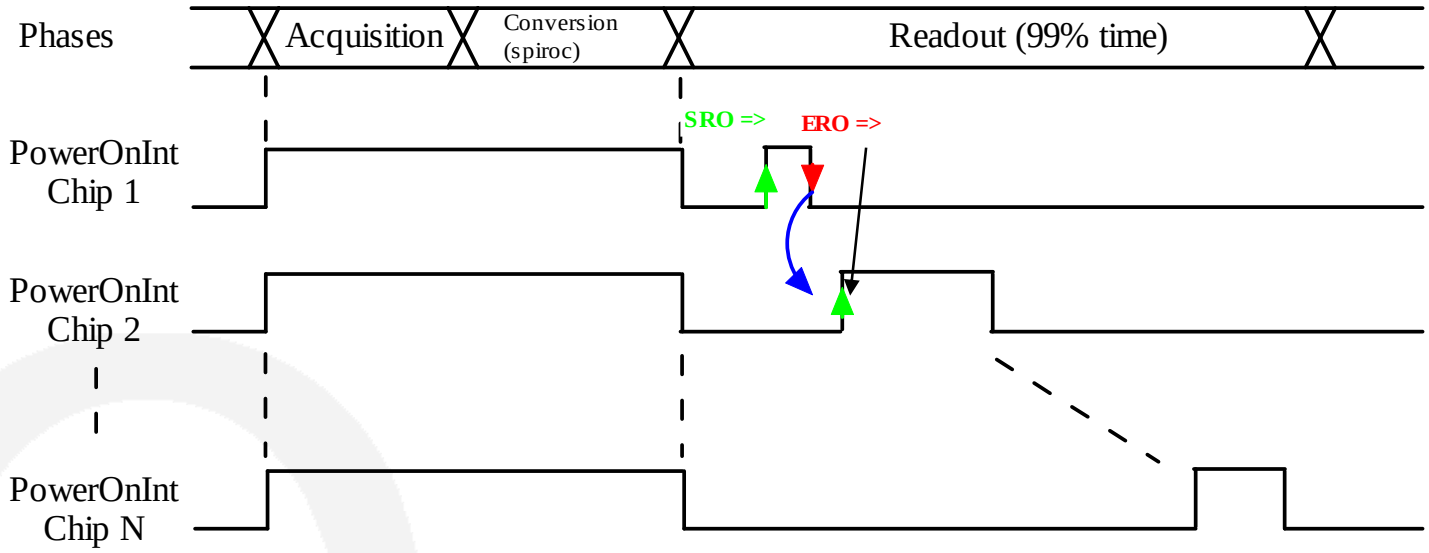
@Frederic Dulucq

- Timing aspect of each phases:
  - Acquisition: 1 ms (common)
  - Readout (daisy chained) @ 5 MHz:
    - max 4 ms for 1 HARDROC
- Max running time for 1 chip < 5 ms (195 ms idle)
- LVDS receiver (Clk40MHz and 5MHz): 2x300µW=> 10µW/ch

=> **LVDS rec can not be powered all the time=> integration of a POD module**

Power On digital: Timing aspect 2/2

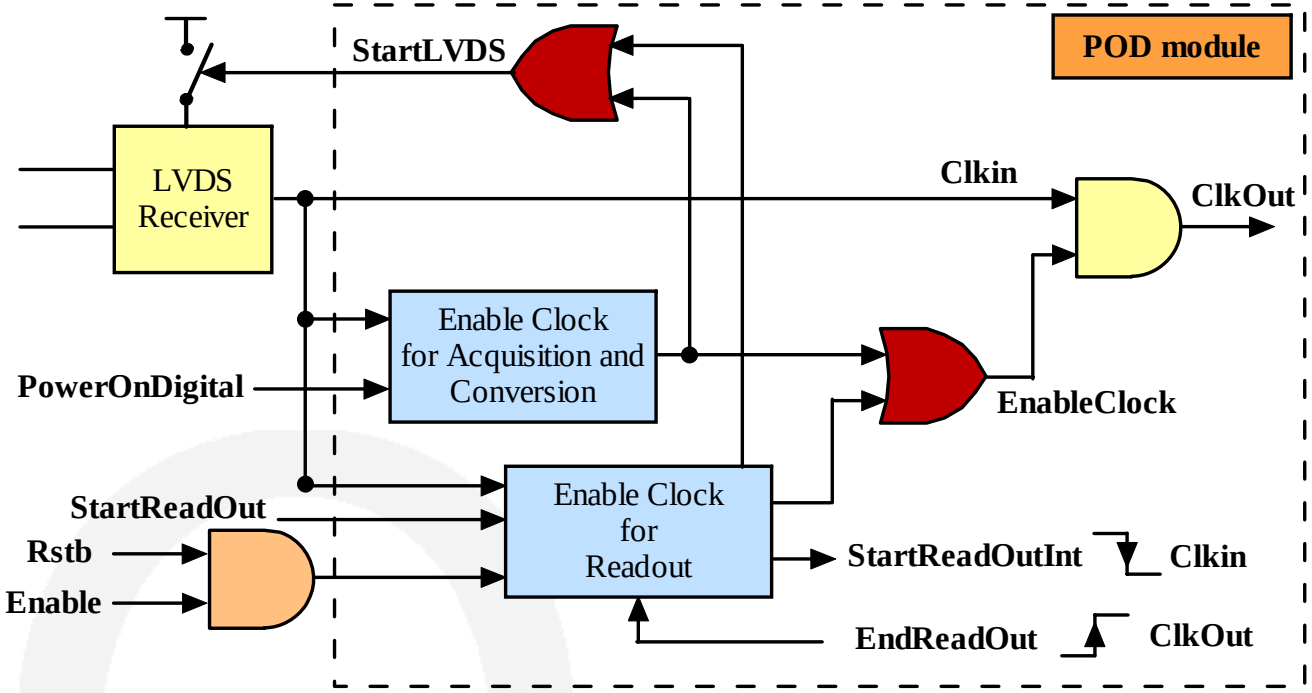
- clocks and LVDS receiver must be power pulsed to meet power budget.

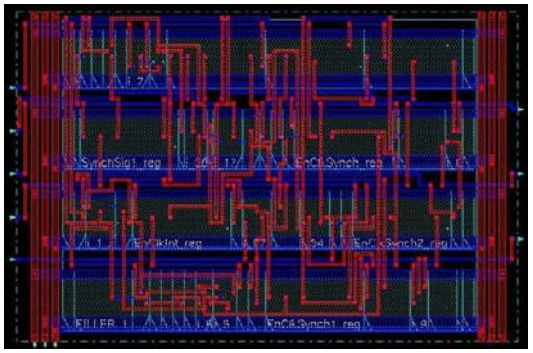


- 2 operation modes :
  - Acquisition, (Conversion) ➔ common to all chips and managed by DAQ
  - Readout ➔ daisy chained managed by **StartReadOut** (sro) and **EndReadOut** (ero)

Power On Digital: POD block diagram

- POD module integrated to power pulse the LVDS receivers of the 5MHz and 40 MHz clocks)

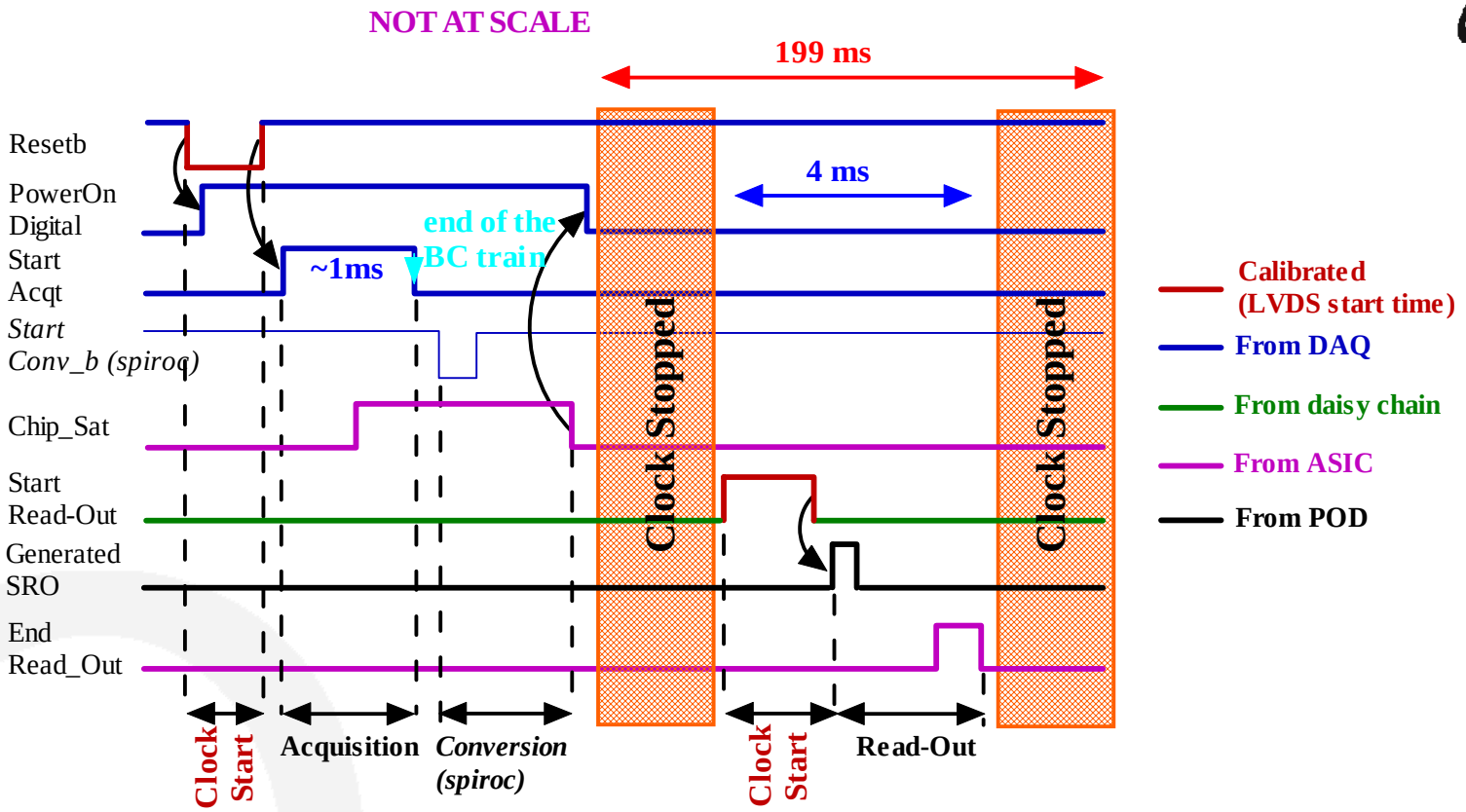




- Clock is started asynchronously, enabled and stopped synchronously (at '0')

- 2 others LVDS receivers (RazChn/NoTrig and ValEvt) active during PowerOnAnalog (during bunch crossing)

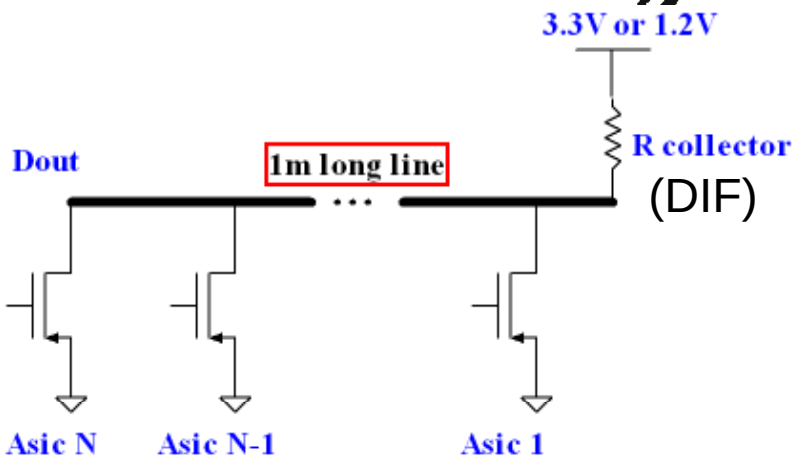
Power On digital: timing sequence of one asic

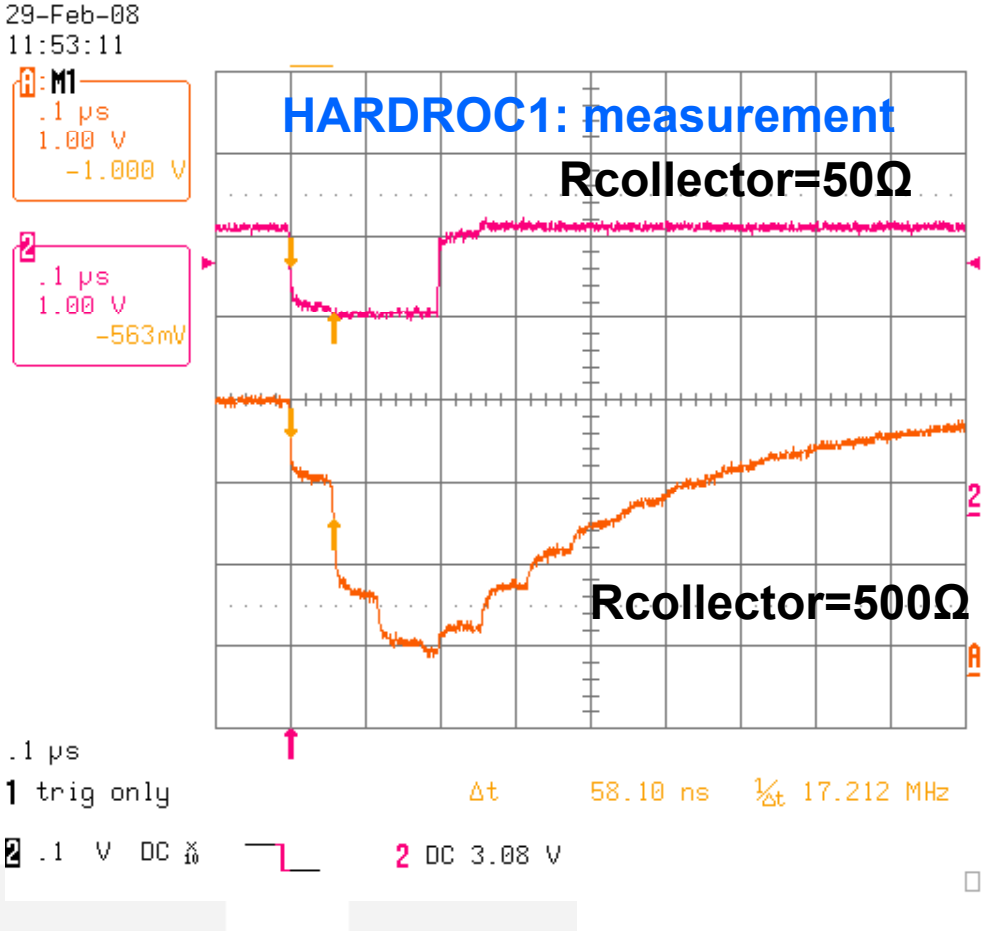


- Some security added:
  - StartReadOut managed asynchronously ➔ low pass filter added
  - Possibility to use StartReadOut instead of the one generated by POD = **POD can be bypassed by SC**
  - PowerOnDigital can be set to '1' by SC => can force the clock

Open collector signals after 1m long line

- 5 m data line / slab -> 500 pF

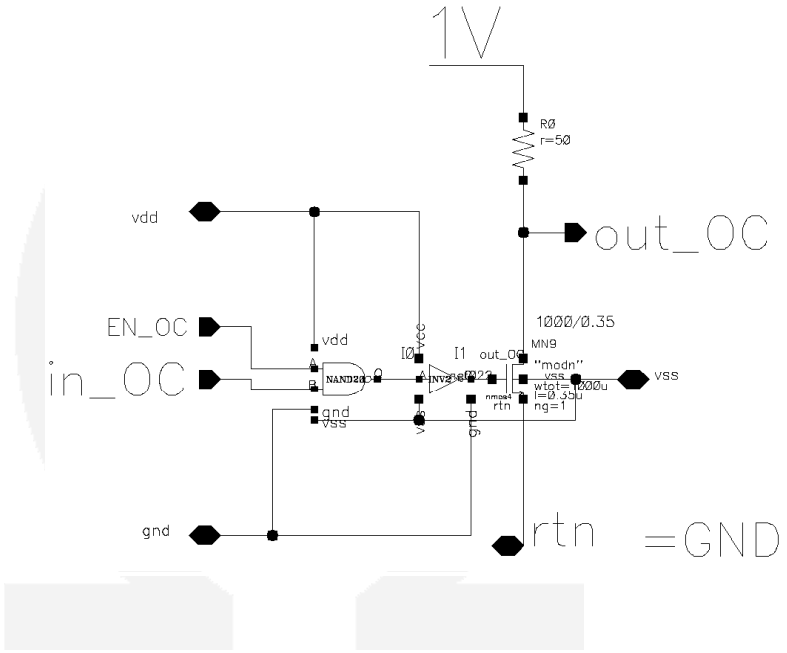


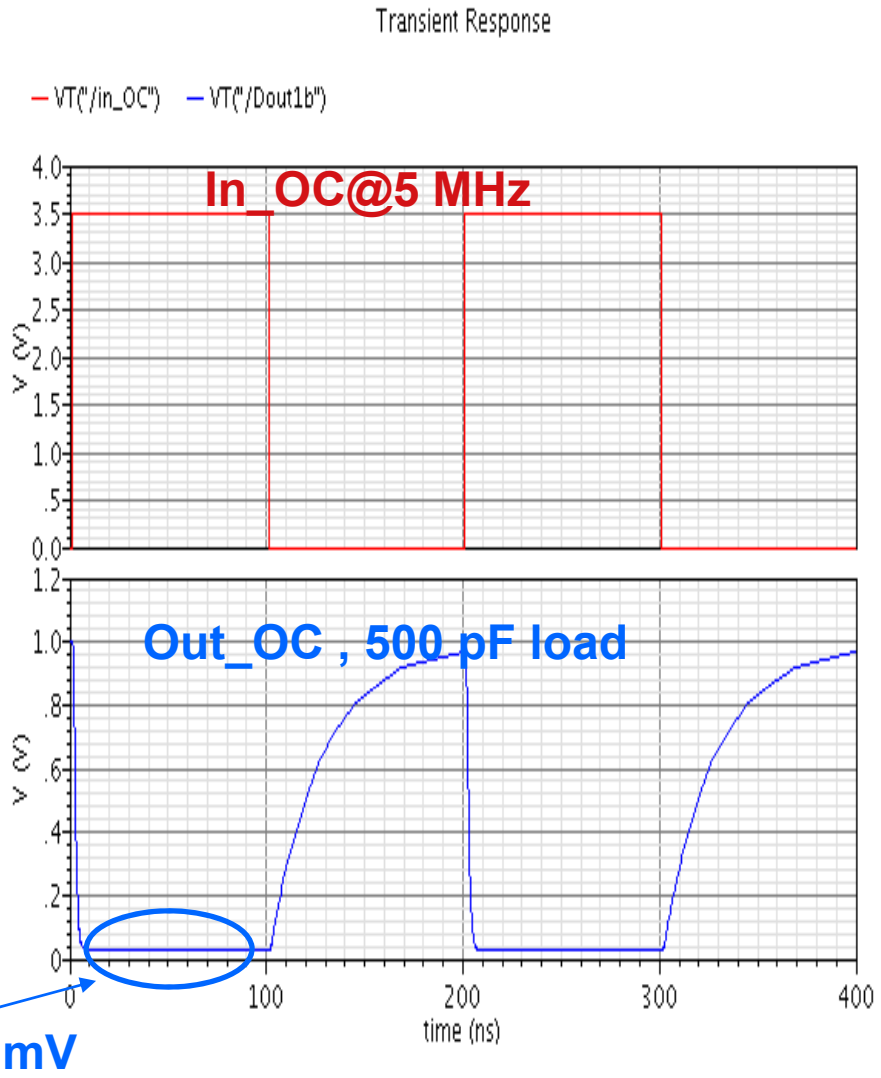


SIMULATION of HR2 OC signals

- Hardroc2: change driver transistor size in ASICs

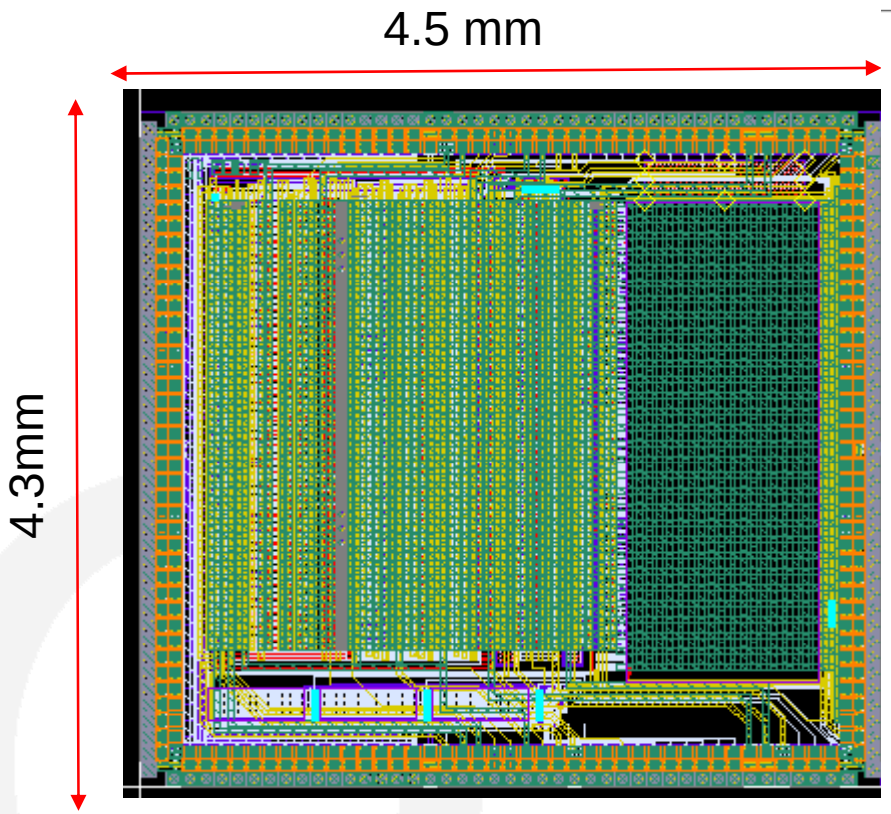
- POWER:
  - 40mVx1V/50Ω=800µW
  - 800µWX4ms/200ms=16µW
  - 16µW/64= 0.25µW/ch

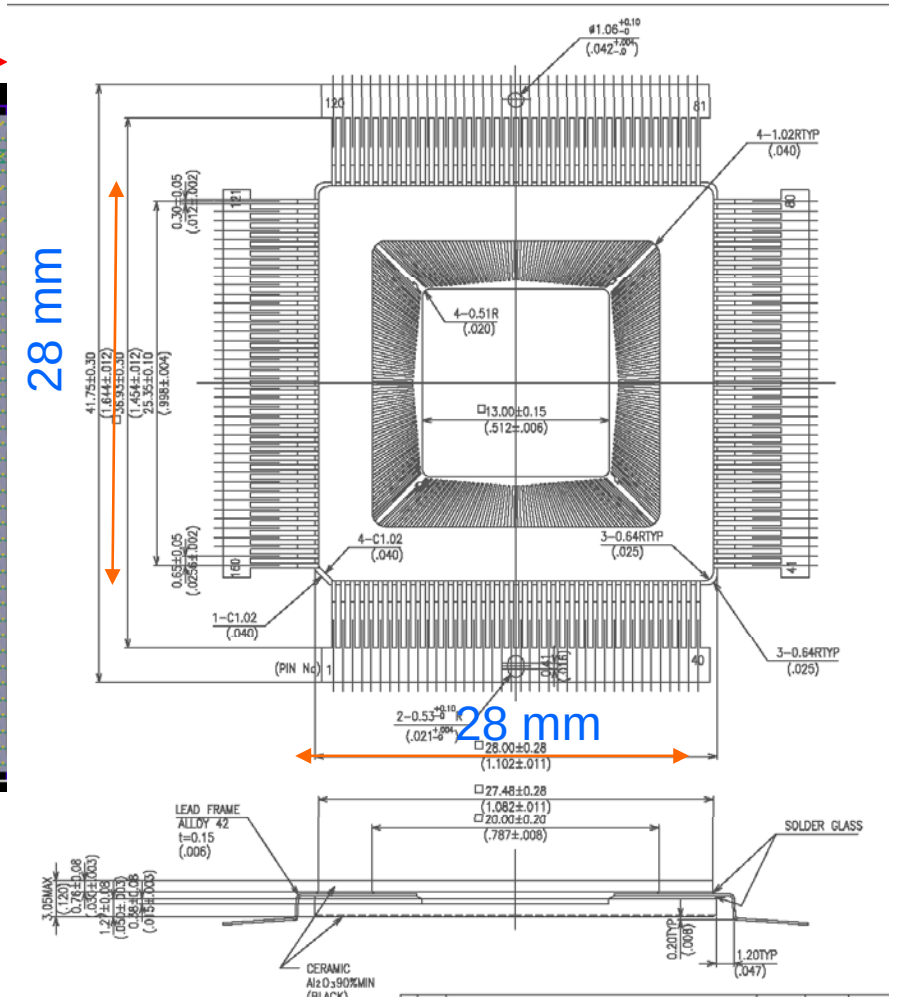




Package: QFP160

- 1single row of pads





Ceramic: 3 mm
Plastic: 1.4 mm

CONCLUSION

- HaRDROC2 prototyped in june 08
  - Keep HARDROC1 basic architecture and backward compatibility
  - Have 3 very different thresholds
  - Move bonding pads to single row (QFP160 package)
  - + many small changes

  (gain accuracy, power pulsing…)
  - Integration of the « POD » module: possible bypass
  - Area : 20 mm2
- HaRDROC2 dies expected mid september