Silicium strips detector readout in 0,13µ m technology

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Silicon strips detector readout

- Front-end's specifications
- First 130nm circuit mesurement
- New readout circuit in 0.13 um
- Conclusion and Future development

Front-End's Specifications

CHARGE MESUREMENT

Preamp + Shaper

Gain: 30mV/MIP with 1-20 MIP input

S/N = 30 750 e- ENC at 1 - 2μ s shaping

Sampling and analog memory

Sparsifier

Threshold adjacent channels sums outputs and activate sampling

ADC

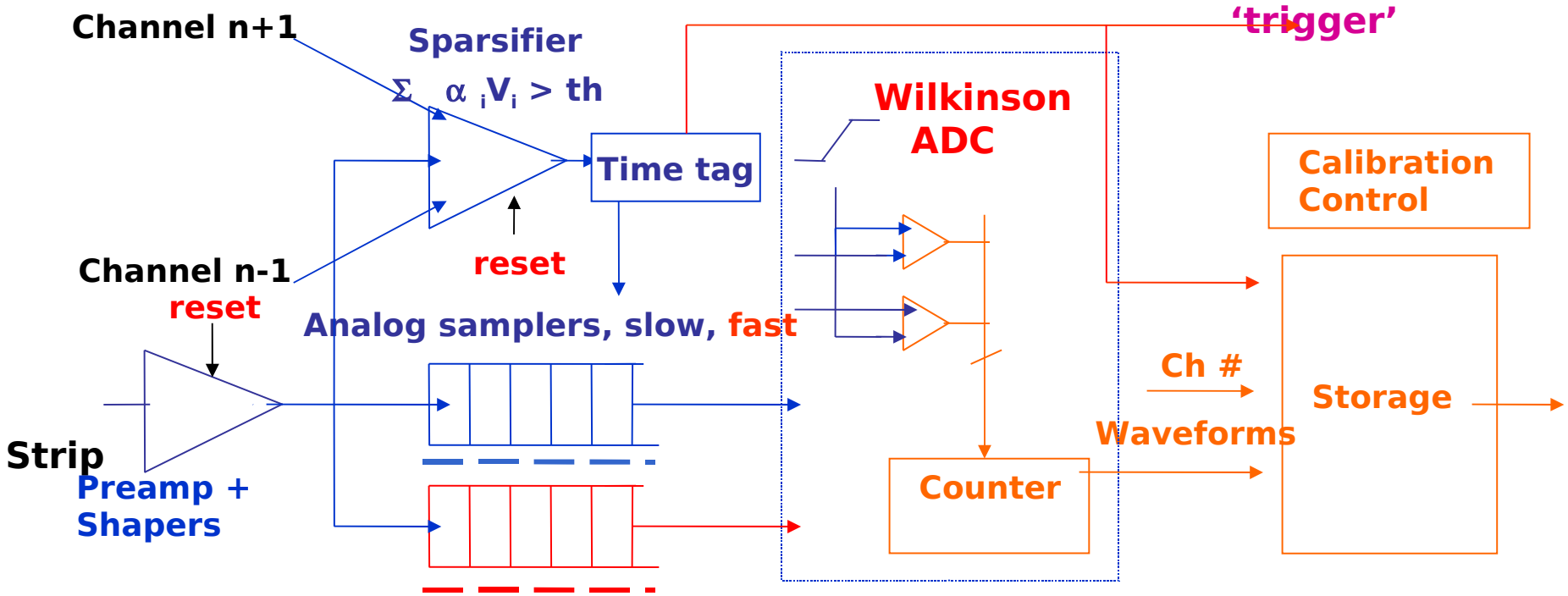
8-10 bits

6 MHz , time interpolated if needed

Front-End's specifications

- Pulse sampling : 8 samples with two shaping times
- Analog Pipeline : 8 events
  2D memory structure: 8x8 caps/channel
- Integrated sparsification/calibration
- ADC : 12 bits Wilkinson
- Power : 1/100 ILC duty cycle: FE Power cycling

FE's foreseen specifications



Charge 1-30 MIP, S/N~ 30, Time resolution: BC tagging 50ns, fine: ~ 2ns

Technologies: Deep Sub-Micron CMOS 130nm

0.18 vs 0.13µ m technology

180nm Mixed-mode process

- 6 metals layers (Al)
- Transistors 3V3
- 1.8V logic supply
- MIM capacitor = 1fF/µ m²
- Three Vt options

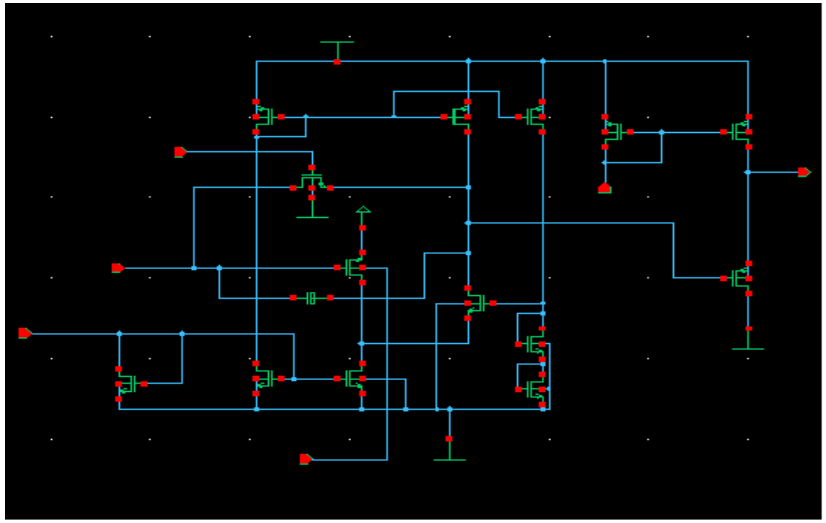
130nm Mixed-mode process

- 8 metals layers(Copper)
- Transistors 3V3
- 1.2V de logic supply
- MIM capacitor =1fF/µ m² or 1.5fF/µ m²
- Same Vt options
- Transistor “low leakage”

First circuit in 0.13 µ m

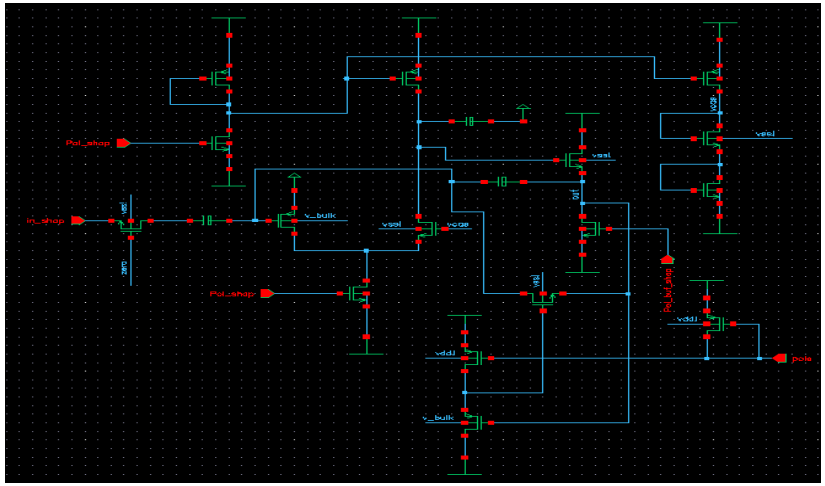
PREAMP

Gain: 28.5mV/MIP
3.3V input transistor 1.5mm/0.5µ m
gm = 1.5 mS/ ~70 µ A
Feedback capacitor = 133 fF
Output dynamic : 20 MIPs
(linearity = 1% at 20 MIPs)
Noise@70 µ A = 1000e$^-$ + 25e-/pF



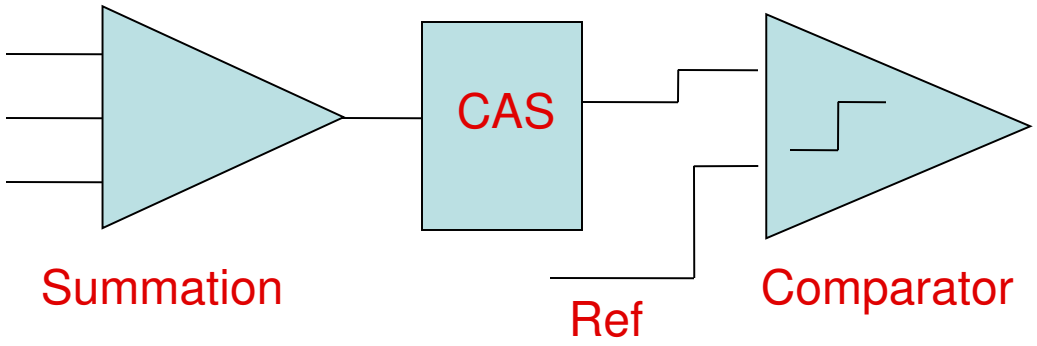
SHAPER

Filter RC-CR
Adjustable time :0.7µ s -> 2µ s
Noise@700ns = 335+22e$^-$/pF
Noise@3µ s = 305+16e-/pF
Output dynamic : 20 MIPS

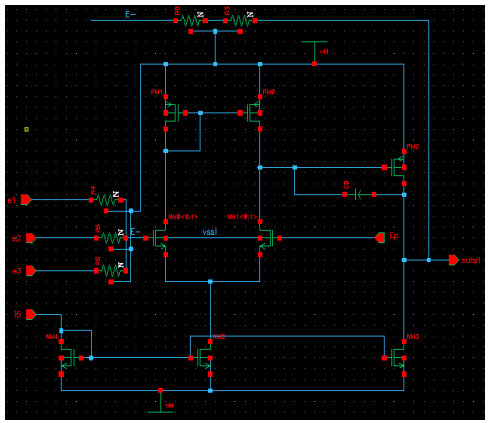


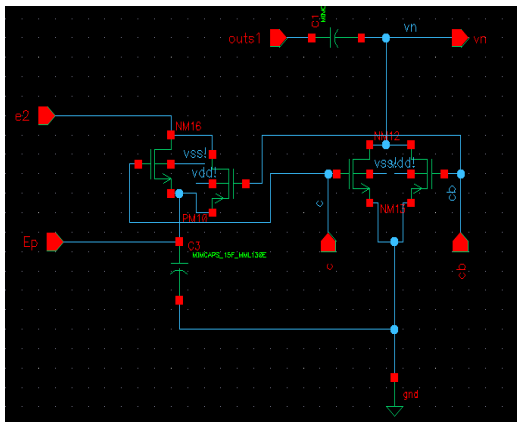
First circuit in 0.13 µ m

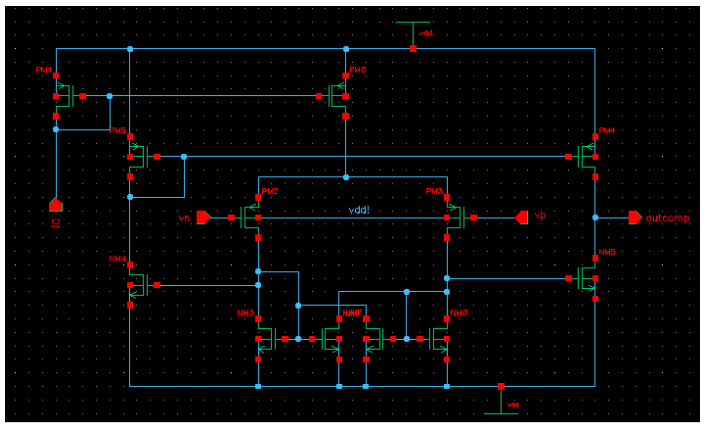
SPARSIFIER



- Threshold analog sums of adjacent channels
- Resolution ~ 0.1mV
- Response time = 186ns

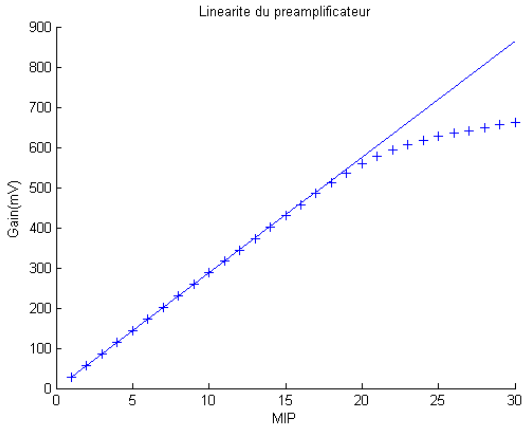




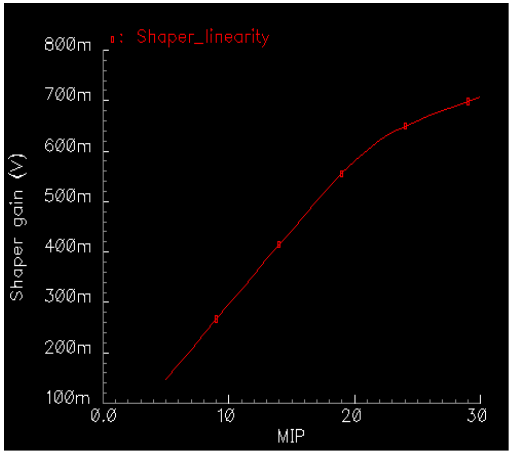


First circuit 0.13 µ m

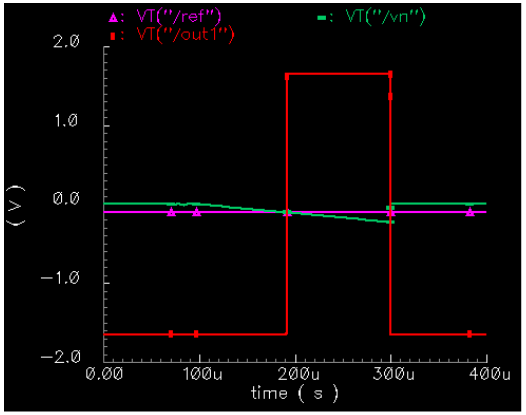
SIMULATIONS :



Preamp's linearity



Shaper's linearity

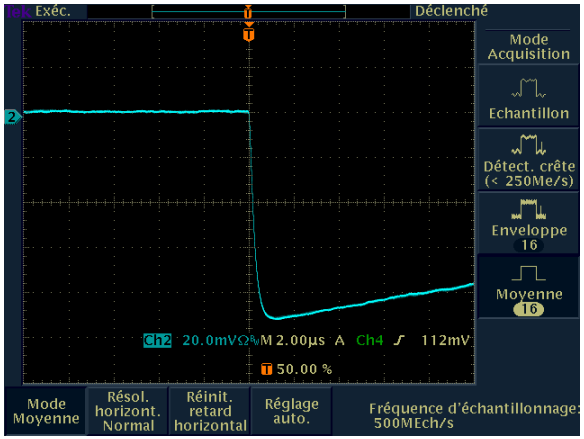


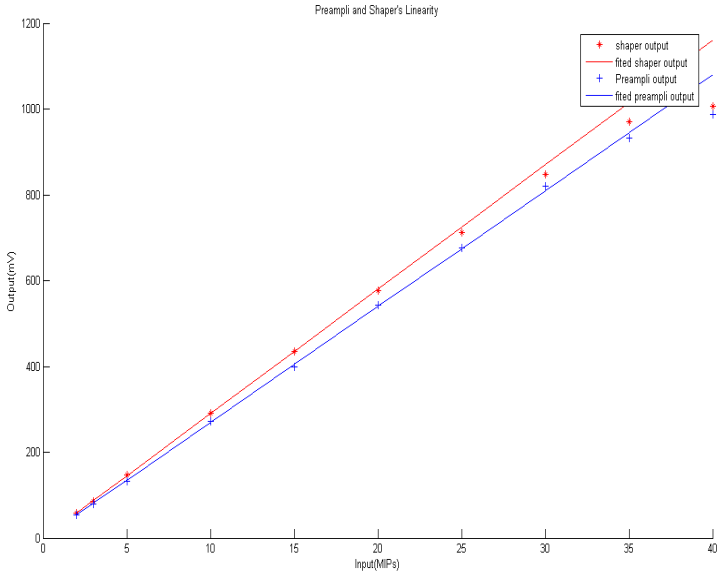
Sparsifier's response

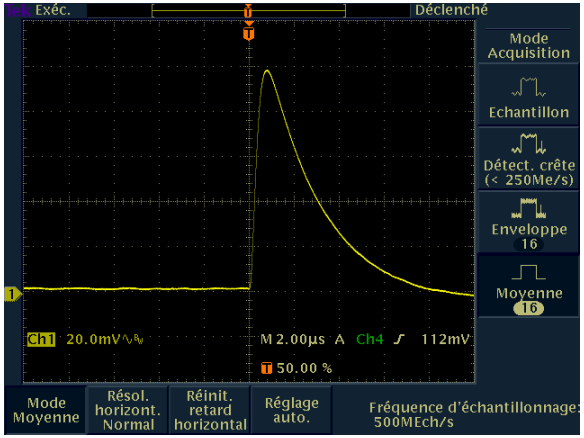
First circuit 0.13 µ m

MEASUREMENT : GAIN - LINEARITY

Preamp Ouput







Shaper output

Preamp :

Gain = 27mV/MIP

Dynamic = 20MIPs (<1%)

Shaper :

Gain = 29mV/MIP

Dynamic = 20MIPs(<1%)

New readout circuit in 0.13 µ m

88 channels (1 test channel)

2D memory structure: 8x8/channels

Fully digital control:

- Bias voltage(10 bits) and current (8 bits)
- Power cycling (in optional)
- Shaping time
- Sampling frequency
- Calibration
- Event tag and time tag generation

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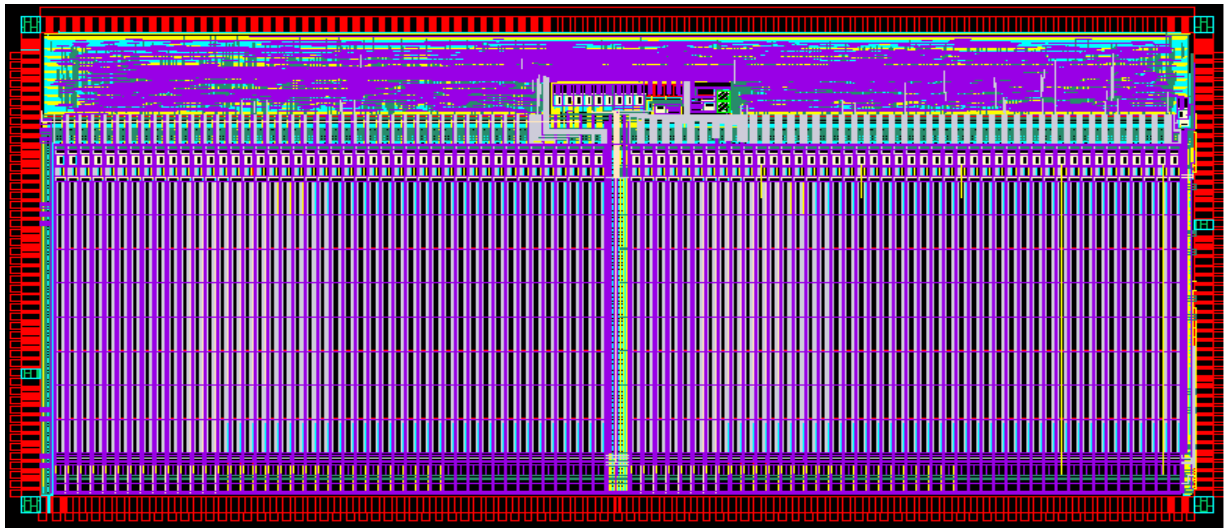
2 Trigger modes: Internal (Sparsification intergrated)
External (LVTTL) for beam test

New readout circuit in 0.13 µ m

LAYOUT :



Size: 5mmx10mm
88 channels (105um pitch)
105umx3.5mm/channel

Analog: 9.5mmx3.5mm
Digital : 9.5mmx700um

Submitted in Juin 24th '08

Conclusion and Future Developement

- **Advantage :**

- Smaller, more compact, programable, flexible

- **Drawback :**

- Problems with noise models

- No access to full library -> difficult to have a full verification

- The disign kit is not well documented

- **Future Work and Development :**

- Testing the chip when receiving

- Develope the 128 channels circuit in technology (UMC/IBM ??)

- Implementation testability for digital part

END