

USB module

<http://ilcagenda.linearcollider.org/conferenceDisplay.py?confId=2798>

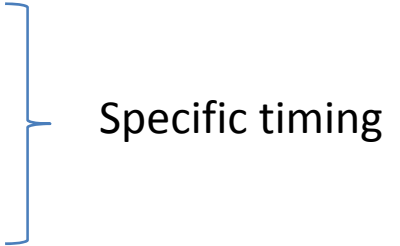
CALICE technical meeting on EVO

Wednesday, June 18

14:00 CEST

Duration : 1h

USB fifo : FTDI245BM chip

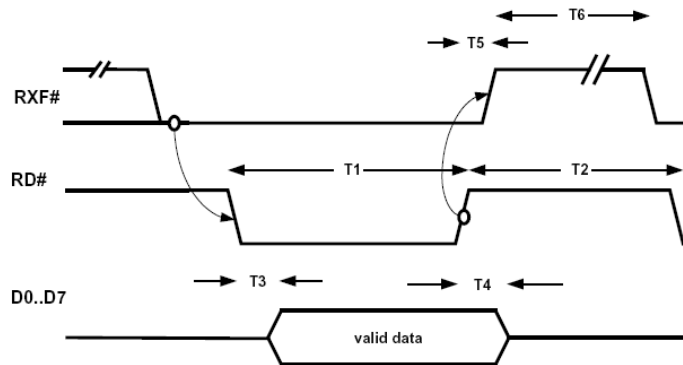
- FIFO
 - 384 byte Tx Buffer (from chip to PC)
 - 128 byte Rx buffer
 - 300 kB/s to 1 MB/s (according to driver)
 - Interfaced to fpga
 - 4 control signal (double handshake)
 - 8 bits data bus (bidirectional)
 - End point ID in external EEPROM
 - Need oscillator (6MHz)
 - Drivers for free : www.ftdichip.com
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- Specific timing

FTDI-FPGA interface

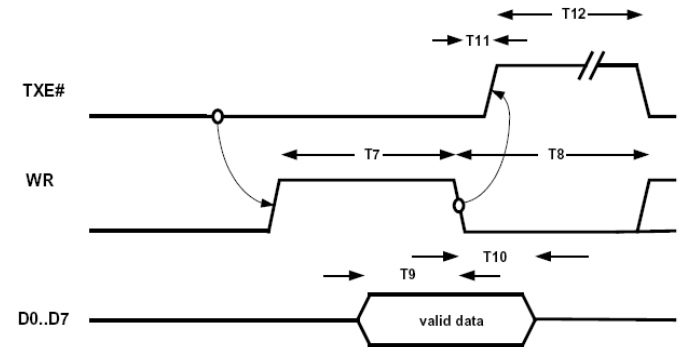
```

siwu      :      out      std_logic;
pwren     :      in       std_logic;
rx        :      in       std_logic;
txe       :      in       std_logic;
rd        :      out      std_logic;
wr        :      out      std_logic;
usb_data  :      inout    std_logic_vector (7 downto 0);
    
```

FT245BM TIMING DIAGRAM – FIFO READ CYCLE



FT245BM TIMING DIAGRAM – FIFO WRITE CYCLE

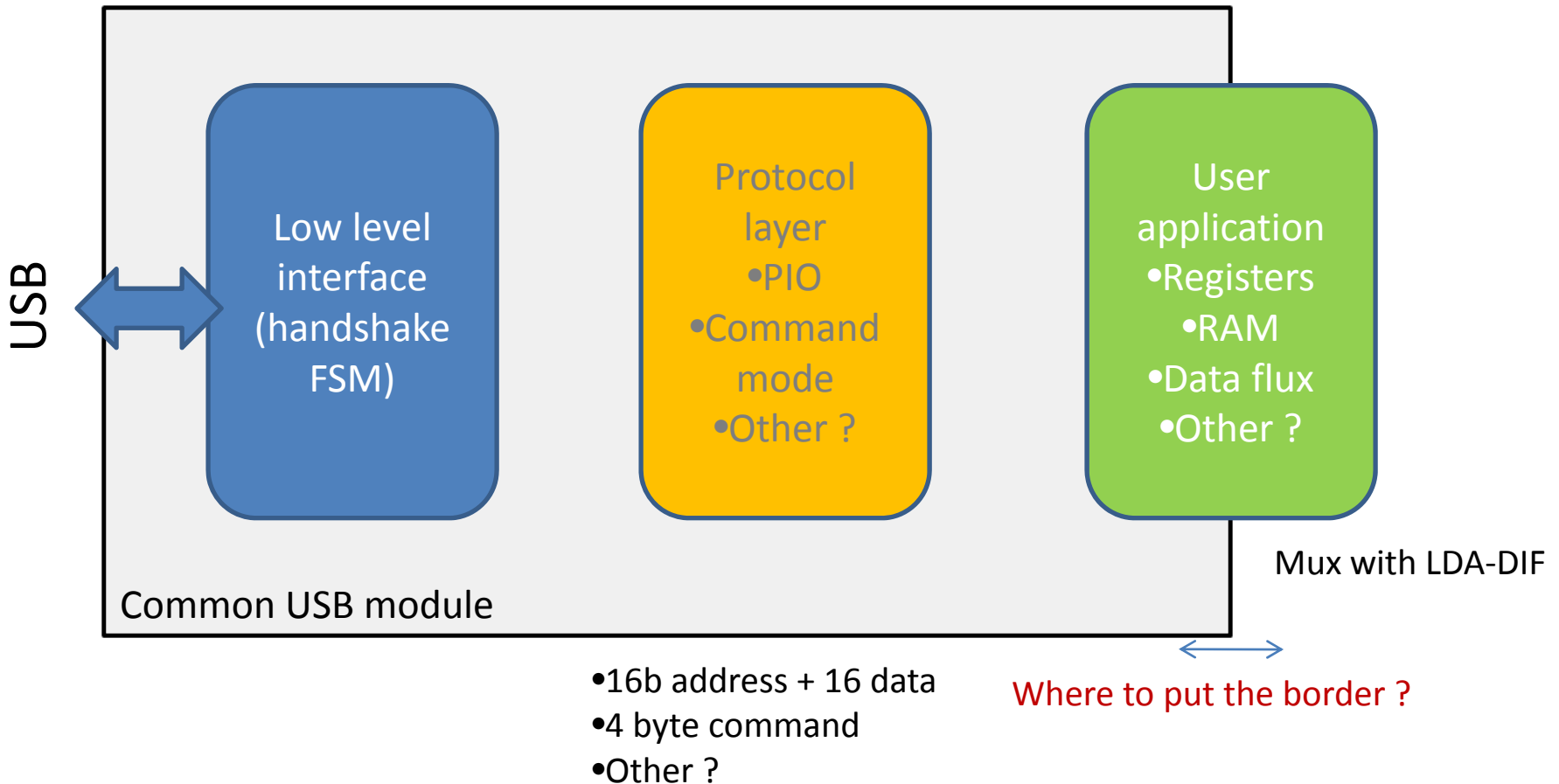


Submodule for low level FSM

Our needs

- DIF registers
- DIF RAM
 - As buffer for SC
 - As buffer for ROC Data
- DIF commands
 - Resets
 - Forced trigger
 - ?
- SLAB/HBU
 - On the flow ? (no DIF buffer = ~ DMA to ROCs)

Module fine structure



SW driver

- Simple functions

- Read
- Write

Carefully read the data sheet :
Buffer is flushed automatically

- Full
- Timeout

Data sent without protocol

- SW driven

- Common higher level library to better fit our needs

- WriteSC (...)
- ReadDAQbuffer(...)
- ResetDIF()
- ...

Hidden USB layers include most of required safety features for data transportation