Calorimeter for ILC	CALICE Electronics short meeting : minutes **List of HW/FW/SW components that could be shared among the collaboration**	Release 1

Revision status	**Comments**	**Date**
Draft 0	First version for comments by RC	06/06/08
Draft 0a	Comments from Julie	11/06/08
Release 1	Public version	18/06/08

CALICE Electronics short meeting: minutes

List of HW/FW/SW components that could be shared among the collaboration

Held on Friday June 06

The purpose of this meeting was to list components that could be shared, based on propositions from participants.

The aim was not

- to discuss about blocs in details
- to give any development responsibility to anybody
- to decide to develop a particular bloc as a common component at the level of the CALICE collaboration

The meeting started at 14:00 CEST.

List of the participants: Julie Prast (LAPP), Guillaume Vouters (LAPP), Christophe Combaret (IPNL), Felix Sefkow (DESY), Mathias Reineke (DESY), Bart Hommels , Maurice Goodrick, Mark Kelly, Franck Gastaldi (LLR), Clement Jauffret (LLR), Remi Cornat (LLR), Vincent Boudry (LLR),…

1) A definition of a sharable bloc was proposed (Rémi)

Attempt to define something that can be shared

- Must have a well defined interface and parameterization
- Must have a clearely defined function
  - (Commonly) written specification document
  - Can be short
- Contact person
- Schedule
- "Small" is efficiently sharable
- Level of test and versioning (status)

2) An USB FW interface was proposed by Julie Prast

   It is inspired from initial code from Clement (LLR). The interface is made up of 3 blocs:

   - A low level module to manage R/W operations on the FTDI chip

- A protocol bloc which decodes the mode of the operations (command mode or bus mode)
- A more user defined module generating command signals, etc…

The bus mode allows transfers with a 16b address bus and a 32b data bus.

3) Christophe Combaret has proposed a corresponding SW library. A link on documentation should be made available soon
4) Clement Jauffret outlined the availability of FW and SW code about USB used for the 4 chips prototype of the DHCAL. It has to be checked if the code is generic enough.
   Code can be seen at :
   http://llr.in2p3.fr/~jauffret/DHCAL
   login : guest
   passwd : dhcalpasswd

5) Felix pointed on DIF-LDA interface. Marc Kelly answered highlighting the work already done on LDA and providing a link to code and advanced documentation. A common module could be developed from this work. He also proposed a SW tools allowing basic data exchanges on Ethernet to communicate with an LDA for debugging purpose.
   http://daqlic.hep.man.ac.uk/cgi-bin/cvsweb.cgi/calice_lda/hdl/?sortby=date;f=H

6) Julie suggested a bloc to manage the analogue probe interface (includes an ADC) of the ROC chips. It is being developed but not tested yet.

7) As no more proposals were expressed, Rémi closed the meeting pointing out the consequences of sharing blocs : it creates some dependencies between projects and peoples that should be carefully evaluated before to take any decision about common developments (technical board). Persons having proposed a bloc or component are invited to give a link on existing documentation and/or to write a short document (few sentences, 1 page) to explain what the bloc consist in.

   Finally a short discussion about how to organize meetings dedicated to each blocs occurs. Two options have been expressed: one short meeting about each bloc (Rémi), small number of longer meetings about more than one topic (Maurice ?).

   The meeting ended at 14:47.

Conclusion of the meeting: The following list has been established. It is based on proposal from the designers of the modules. Next meetings will be dedicated to give more details about each modules.
On line written table to list sharable modules (to be completed):

Component name	Contact person	status	schedule	description
USB Analogue RO RO itf DIF-SLAB itf LDA-DIF itf LDA-ethernet USB debug sw	Julie Julie Clement LPC ? or LAPP Marc Marc Clement	V0 tested Not tested Working with old ROCs		