# Towards the Final Telescope Sensor : TC/MIMOSA-26

## Progress Report

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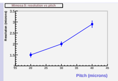
*on behalf of IPHC and IRFU/Saclay*

## OUTLINE

- **Strategy of the chip development (reminder)**
- **Column parallel sensor prototyping :** *Objectives of IDC prototyping – Lab & beam test results*
- **The question of radiation tolerance**
- **SDC-2/SUZE-01 zero suppression $\mu$circuit :** *Established performances*
- **Final chip : status of design and plans**
- **Summary - Outlook**

- **Motivation for a dedicated beam telescope architecture:**
  - *beam intensity : read-out* $\lesssim 10^4$ *frames / second*
  - *DUT surface & resolution requirements : active surface of 1x2 cm*$^2$ *with* $\gtrsim$ *0.5 million pixels*
  - $\Rrightarrow$ *sensor should incorporate zero suppression* $\Rrightarrow$ **+** *integrated signal discrimination*

- **Development strategy:** *two prototyping lines pursued in parallel*
  - *column // architecture adapted to the required speed* ▷ *MIMOSA-16* ▷ **IDC/**MIMOSA-22
  - *integrated* $\emptyset$ *& output memories adapted to the corresponding occupancy* ▷ **SDC-2 /**SUZE-01





# Reminder on Architecture Motivation and R&D Strategy (2/2)

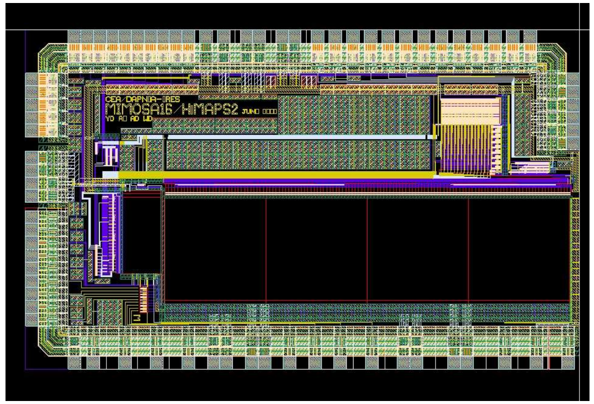
- **Specific goals of IDC :**
  - *validate the fast read-out architecture developed in MIMOSA-16 (next slide ) at* **Real Scale**
  - *extract an optimal pixel design (sensing diode and signal prcoessing $\mu$circuits)*
  - *improve the chip testability (JTAG, analog outputs, pads, ...)*

- **2 versions of IDC designed and fabricated :**
  - *MIMOSA-22 : mainly for overall pixel architecture definition*
  - *MIMOSA-22bis : robustness, fine tuned optimisation, radiation tolerance*

- **Objective beyond IDC :**
  - *once validated, the IDC architecture will be merged with SDC-2*
    - $\Rrightarrow$ *Final Sensor (TC/MIMOSA-26), to be sent for fabrication in Novembre*

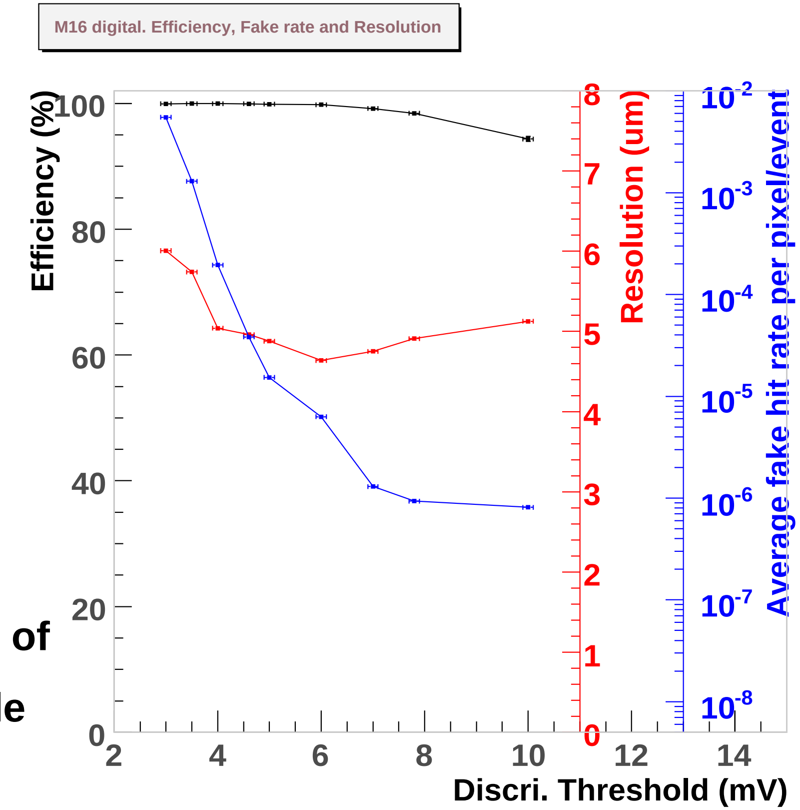
# Performances of a Small Prototype with Digitised Output

- *MIMOSA-16 :* ◇ *fabricated in 2006 (coll. with IRFU/Saclay)*
  - ◇ *32 col. of 128 pixels (25 $\mu m$ pitch, integrated CDS )*
  - ◇ *24 col. ended with an integrated discriminator*
  - ◇ *4 different pixels (i.e. 4 sub-arrays)*




- *Tests at CERN-SPS ($\sim$ 180 GeV $\pi^-$) in Summer 2007*
  - $\rightarrowtail$ *results of one sub-array (S4)*

| *Discri. threshold* | *Detection eff.* | *Fake rate* | *Resolution* |
|---|---|---|---|
| *4 m V* | *99.96 $\pm$ 0.03 (stat) %* | $\sim$ *2·10$^{-4}$* | $\sim$ *4.8 – 5.0 $\mu m$* |
| *6 m V* | *99.88 $\pm$ 0.05 (stat) %* | *<10$^{-5}$* | $\sim$ *4.6 $\mu m$* |




▷▷▷ **Architectures of pixel (integrated CDS ) and of full chain made of "columns ended with integrated discri." validated at small scale**

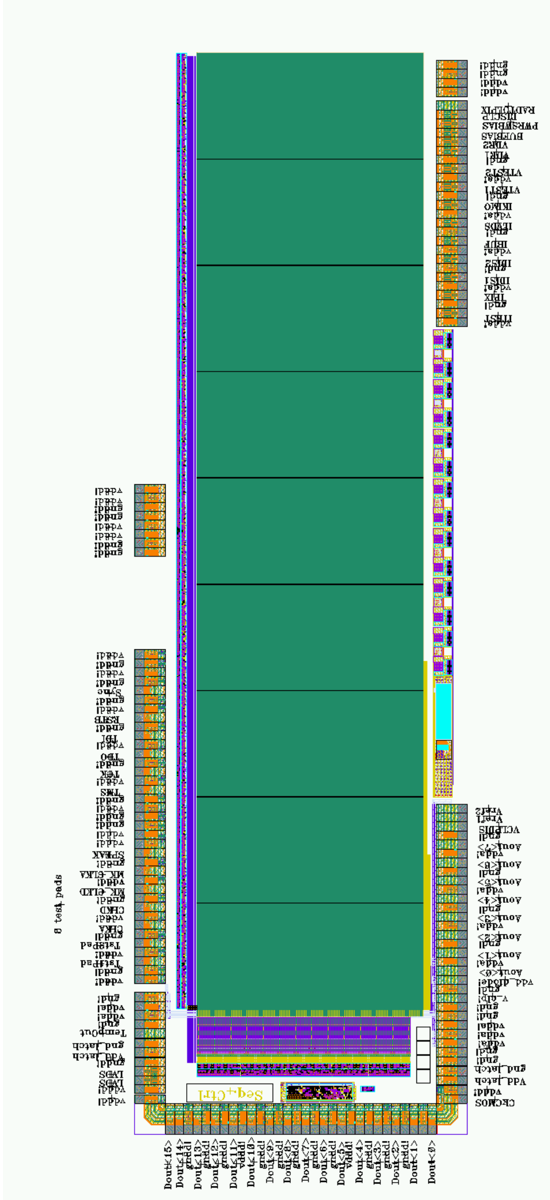
♣ **Extension of MIMOSA-16 $\rightarrowtail$ larger surface, smaller pitch, optimised pixel, JTAG, more testability**

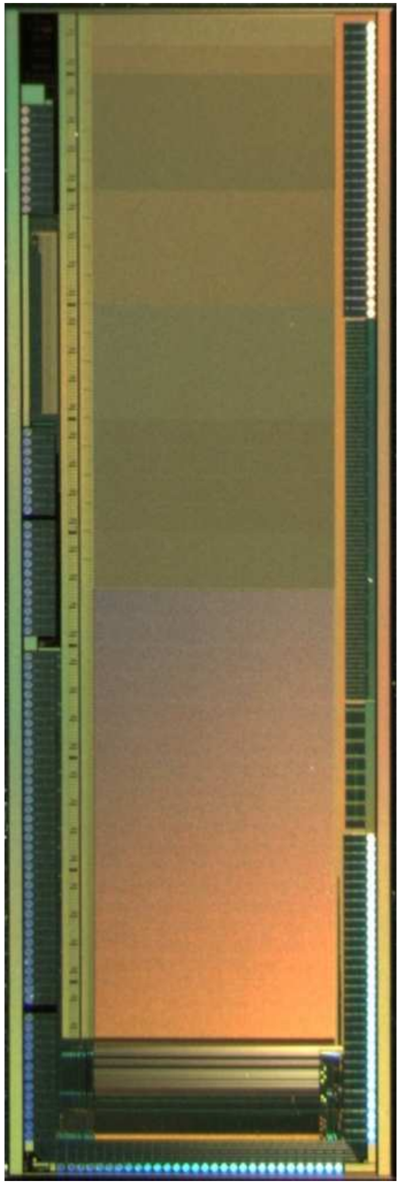
## Pixel characteristics (*optimal charge coll. diode size ?* ) :

- ⋇ **pitch : 18.4 $\mu m$** (compromise resolution/pixel layout)
- ⋇ diode surface : $\sim$ 10 – 20 $\mu m^2$ to optimise charge coll. & gain
- ⋇ **128 columns ended with discriminator**
- ⋇ **576 pixels per column ($\equiv$ final column length )**
- ⋇ 8 columns with analog output for test purposes
- ⋇ 9 sub-matrices of 64 rows :

  17 pixel designs w/o ionising rad. tol. diode

  $\Rrightarrow$ **active digital area $\sim$ 25 mm$^2$** (128 x 576 pixels )
- ⋇ **read-out time $\sim$ 100 $\mu s$ ( $\sim$ 10$^4$ frames/s )**





## Testability :

- ⋇ JTAG + bias DAC $\rightarrowtail$ **programmable chip steering**
- ⋇ 2 additionnal DC voltages to emulate pixel's output

  for independent discriminator performance assessment
- ⋇ output frequency $\leq$ 40 MHz

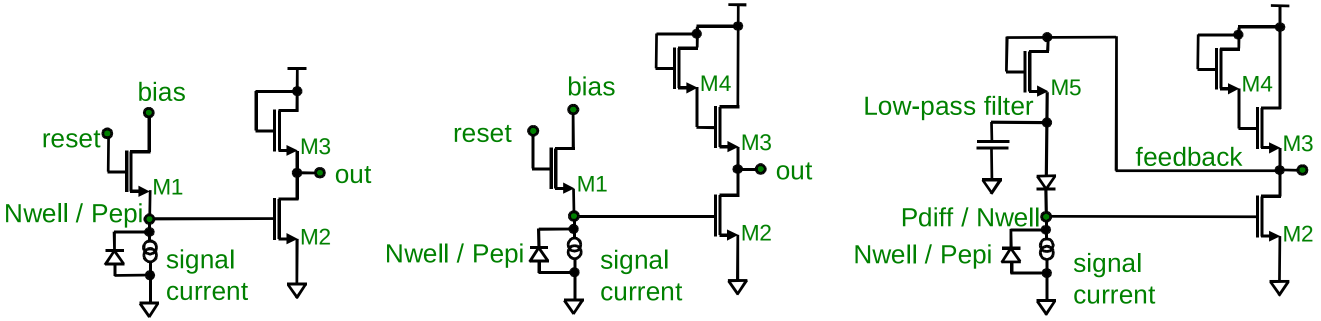
# IDC/MIMOSA-22: Pixel Designs Investigated

- **Topics investigated :**
  - ⋇ *optimum between CCE ($\Rrightarrow$ large diode) and capacitive noise ($\Rrightarrow$ small diode)*
  - ⋇ *effective and robust pre-amplification scheme*
  - ⋇ *low noise (ionising) radiation tolerant design*
  - ⋇ *temperature dependence of performances*
  - ⋇ *performance uniformity over full active surface*
  - ⋇ *comparison with MIMOSA-16 performances (24 columns of 128 pixels)*

- **5 pixel designs implemented, combining 2 reset & 2 ampli. variants (w/o rad. tol. diode, diff. diode sizes):**
  - ⋇ *reset diode with (standard) common source amplifier : w/o improved gain*
  - ⋇ *self-biased feedback diode with common source amplifier with improved gain*
  - ⋇ *feedback reset diode with common source amplifier : w/o improved gain*

- **Status :**
  - ⋇ *back from foundry since Feb.'08*
  - ▷ *lab tests of analog and digital (discri.) outputs with $^{55}$Fe source completed*
  - ▷ *first beam tests (CERN-SPS / August '08) analysed*

- **Various pixel designs (rad. tol. and standard ) :**
  - *reset diode (improved gain)*
  - *self-biased diode with feedback (improved gain)*




(S13) (S10) (S6)

- **Main results obtained with exposure to $^{55}$Fe source (t$_{r.o.}$ = 92.5 $\mu s$) :**
  - *Noise :*
    - *Temporal (pixel) Noise $\sim$ 0.5 – 0.7 mV (10 $<$ N $<$ 14 e$^-$ ENC )*
    - *FPN $\sim$ 0.25 mV*
    - *N (rad. tol. pixels ) $\sim$ N (standard pixels ) + 1 e$^-$ ENC*
  - *Cluster CCE :*
    - *3x3 pixels : 70 – 80 %*
    - *5x5 pixels : 80 – 90 %*
  - *modest T dependence between $\sim$ 10$^\circ$C and 35$^\circ$C : $\lesssim$ 10 % noise variation*
  - *5 different chips characterised : identical performances within $\pm$ 5 %*

# IDC/M22 Lab Tests : Analog Output Results

| | S6 | | S7 | | S8 | | S9 | | S10 | |
|---|---|---|---|---|---|---|---|---|---|---|
| | mV | e- | mV | e- | mV | e- | mV | e- | mV | e- |
| TN | 0.612 | 11.5 | 0.601 | 10.7 | 0.615 | 11.3 | 0.595 | 10.0 | 0.639 | 11.6 |
| FPN | 0.250 | 4.7 | 0.263 | 4.6 | 0.254 | 4.4 | 0.273 | 4.6 | 0.222 | 4.0 |

| | S12 | | S13 | | S15 | | S16 | | S17 | |
|---|---|---|---|---|---|---|---|---|---|---|
| | mV | e- | mV | e- | mV | e- | mV | e- | mV | e- |
| TN | 0.636 | 11.2 | 0.692 | 13.4 | 0.682 | 12.8 | 0.536 | 12.4 | 0.527 | 11.4 |
| FPN | 0.225 | 4.0 | 0.269 | 5.2 | 0.277 | 5.2 | 0.218 | 5.1 | 0.217 | 4.7 |

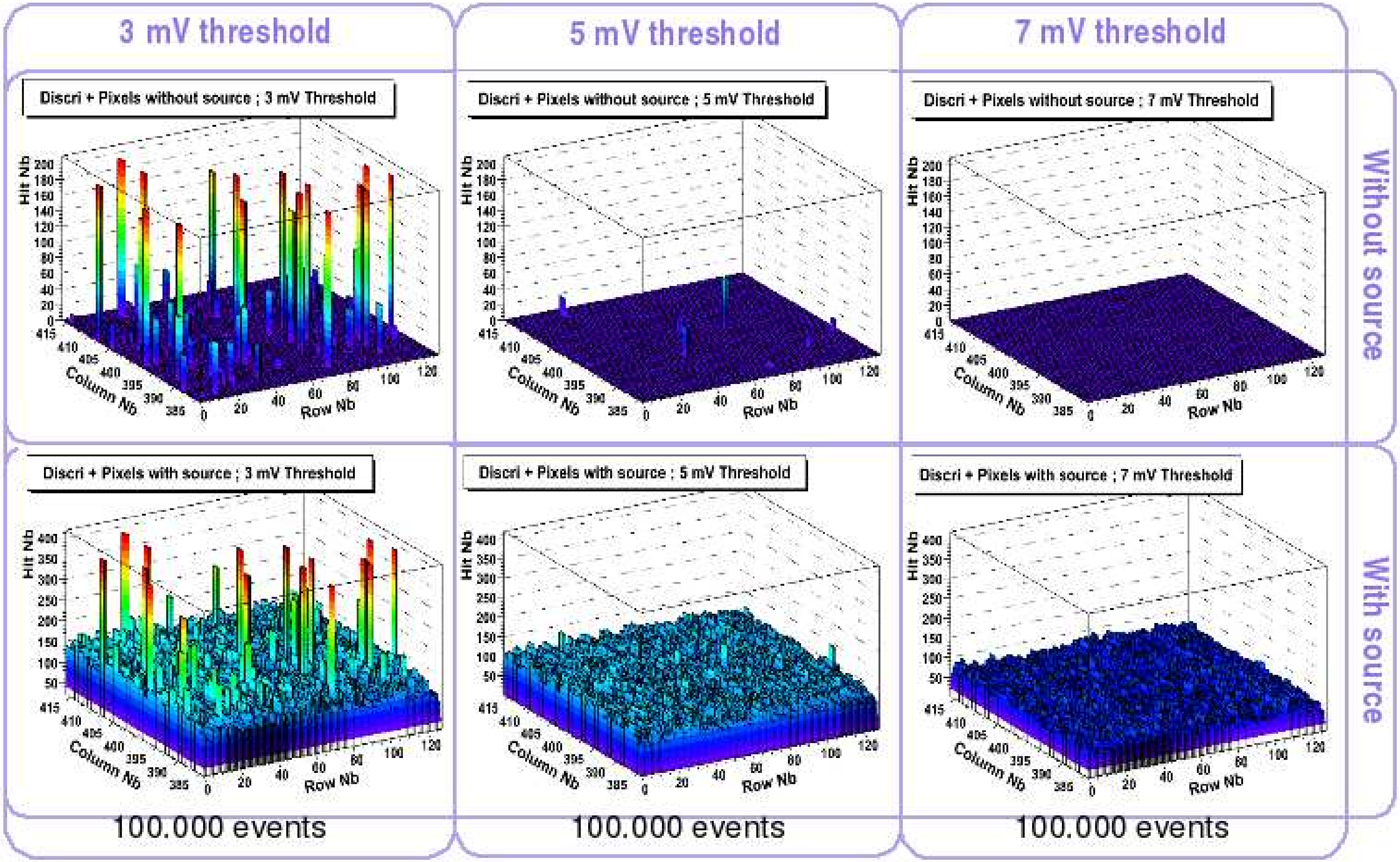
- Pixel Noise ~ 0.6mV
- FPN ~ 0.25 mV

} ⇒ Similar results than smaller prototype MIMOSA16 ones

- RadTol pixels (S6, S10, S13) Noise slightly higher than for standard pixels

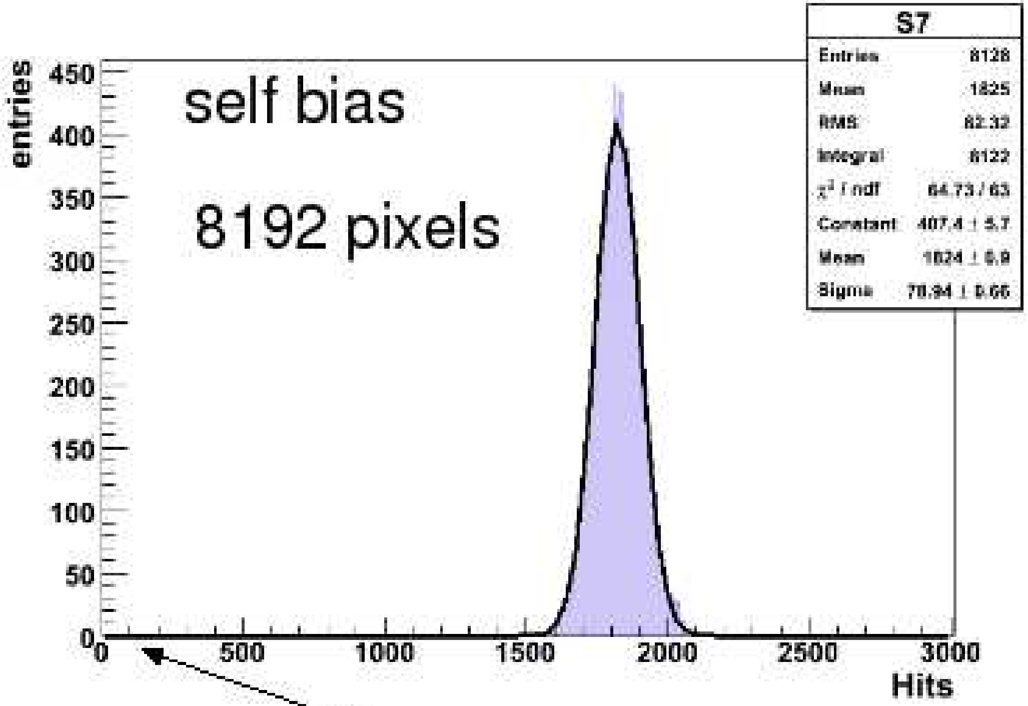
# IDC/M22 Lab Tests : Digital Output Results (1/2)

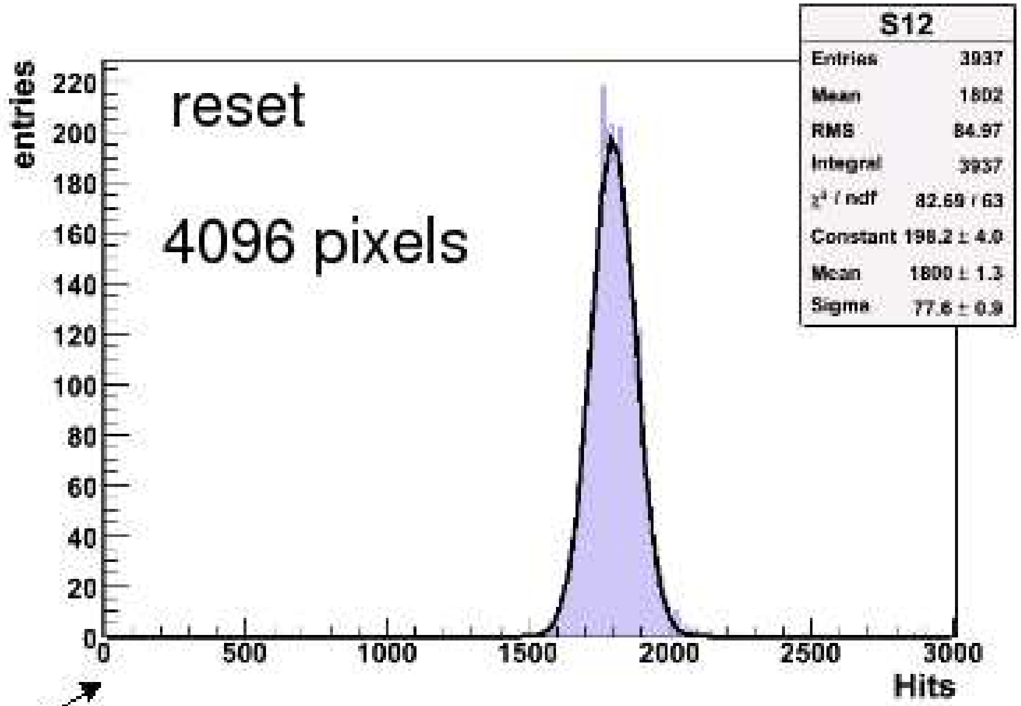
## S12 response for 3, 5 and 7 mV threshold without and with $^{55}Fe$ source



# IDC/M22 Lab Tests : Digital Output Results (2/2)

## 5 mV threshold with $^{55}Fe$ source




No dead pixel number

Good uniformity of discriminator response, within 4%

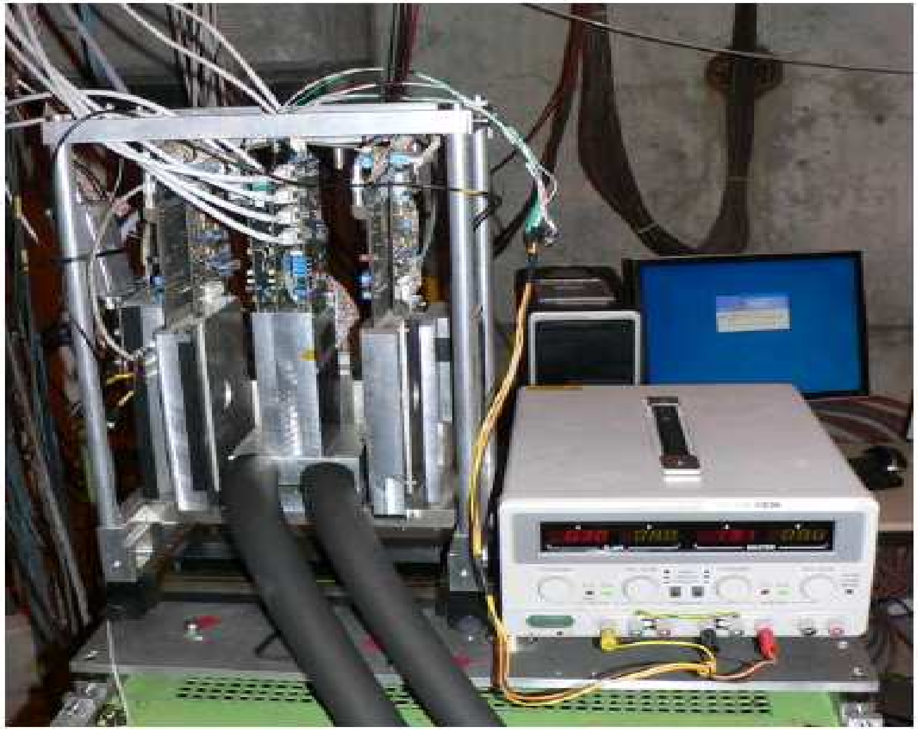
# IDC/M-22 Beam Tests : Data Taking Conditions

- **4 weeks of beam time at CERN-SPS :**
  - ▷ ∼ *2 weeks in August with MIMOSA-22 (EUDET period)*
  - ▷ ∼ *2 weeks in Sept.-Oct. with MIMOSA-22bis (SiLC period)*

- **T4-H6 beam line : ∼ 120 GeV $\pi^-$ beam** ▷▷▷▷

- **Chips mounted at center of Si-strip telescope**

  *(4 pairs of orthogonal strips)* ▷▷▷▷

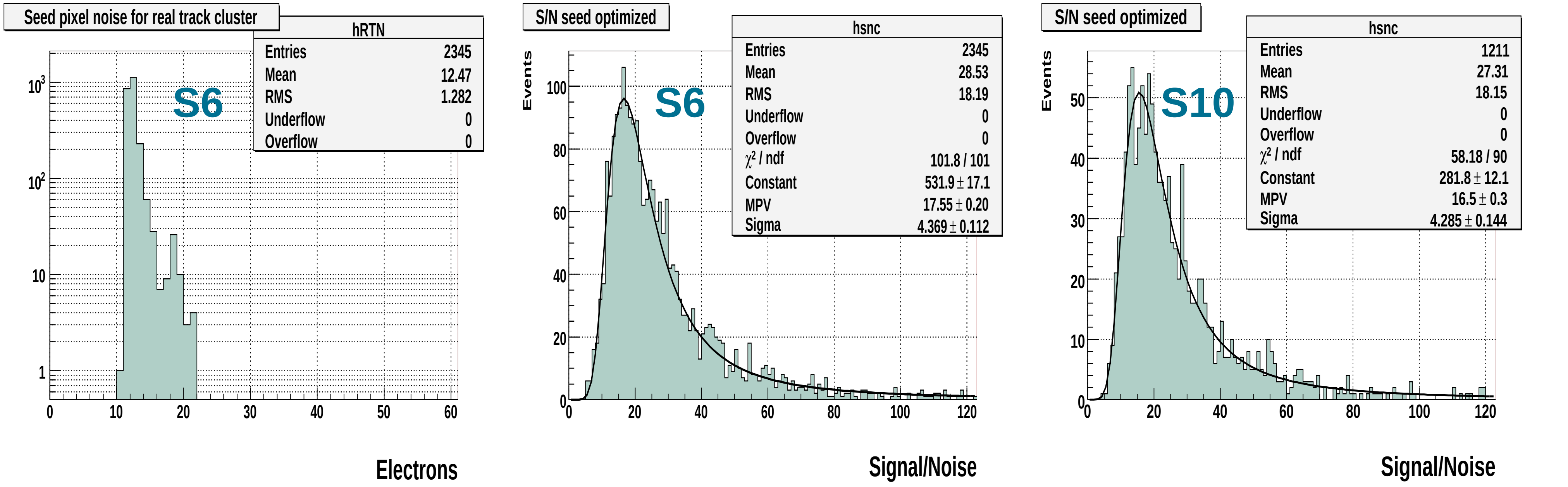


- **2 MIMOSA-22 and 4 MIMOSA-22bis chips tested**

  *at several values of discriminator threshold*

- **$>$ 1 million tracks reconstructed in the sensors**

- Noise and S/N (seed pixel ) distributions delivered by the 8 columns without discriminator



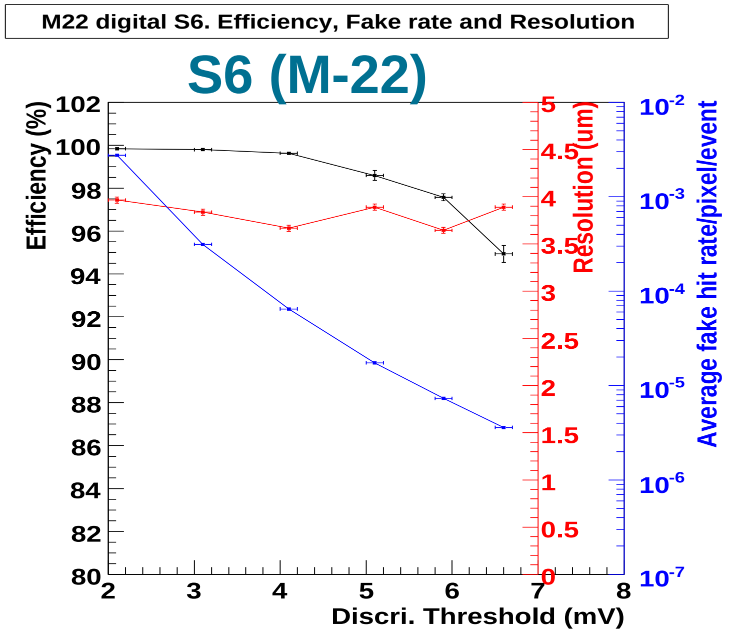

- **Detection performances (det. eff. , N and S/N for hits where the seed pixel exhibits S/N $>$ 4 ) :**

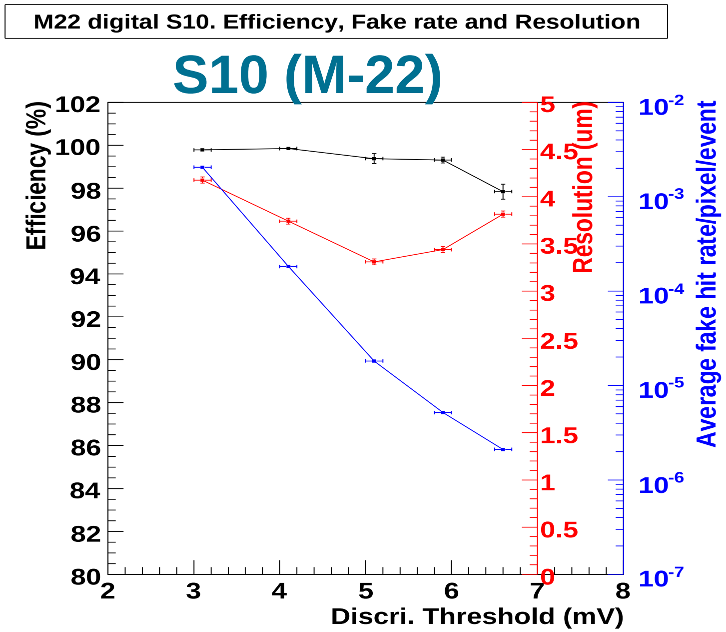
| *Sub-array* | *S6* | *S7* | *S8* | *S9* | *S10* | *S12* | *S13* |
|---|---|---|---|---|---|---|---|
| *Det. eff.* | *99.93 % $\pm$ 0.05 %* | *99.95 % $\pm$ 0.04 %* | *100.00 % +0/-0.30 %* | *100.00 % +0/-0.14 %* | *99.87 % $\pm$ 0.09 %* | *100.00 % +0/-0.08 %* | *100.00 % +0/-0.07 %* |
| *N ($e^-$ ENC)* | *12.5 $\pm$ 0.1* | *11.6 $\pm$ 0.1* | *12.3 $\pm$ 0.1* | *10.6 $\pm$ 0.1* | *13.6 $\pm$ 0.1* | *12.1 $\pm$ 0.1* | *14.0 $\pm$ 0.1* |
| *S/N (seed, MPV)* | *17.6 $\pm$ 0.2* | *18.5 $\pm$ 0.2* | *20.9 $\pm$ 1.1* | *19.5 $\pm$ 0.5* | *16.5 $\pm$ 0.3* | *18.2 $\pm$ 0.3* | *16.0 $\pm$ 0.3* |

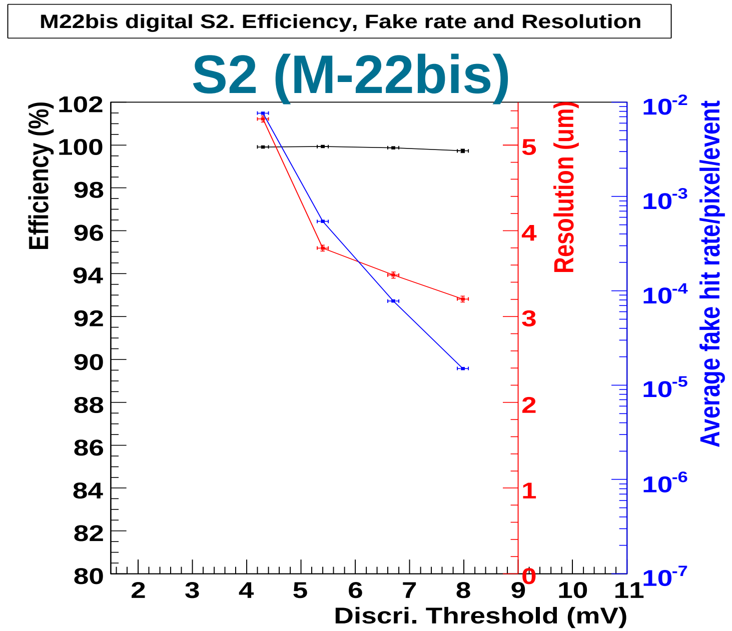
⁕ *very satisfactory performances ( det. eff. $\sim$ 99.9 % and single pt resolution $\lesssim$ 1.5 $\mu m$ )*

$\Rrightarrow$ **pixel architecture (diode size, rad. tol. diode design, amplification scheme ) validated**

- **Det. eff., fake hit rate & spatial resolution for S6 & S10 (M-22) and S2 (M-22bis) vs discri. threshold :**



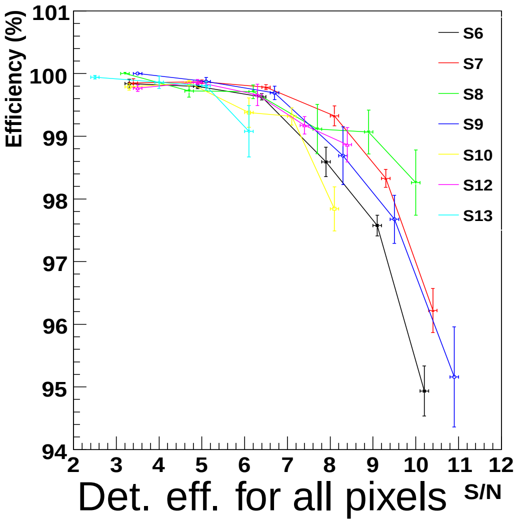

- **Main results:**

  - *rather marginal performance differences between $>$ 10 diff. pixels (e.g. rad. tol. vs standard )*
  - *det. eff. of analog output $\sim$ 99.9 % for all sub-arrays $\Rrightarrow$ pixel architecture validated*
  - *det. eff. of digital output $\gtrsim$ 99.8 % for almost all sub-arrays (agrees with MIMOSA-16 )*
  - *fake hit rate very low (O($10^{-4}$ – $10^{-5}$ )) while det. eff. still near 100 %*
  - *single point resolution $\gtrsim$ 3.5 $\mu m$ (as expected )*
  - *no performance non-uniformity observed over the chip surface $\Rrightarrow$ real scale check validated*

# IDC/M-22(bis) Beam Tests : Pixel Performance Comparison

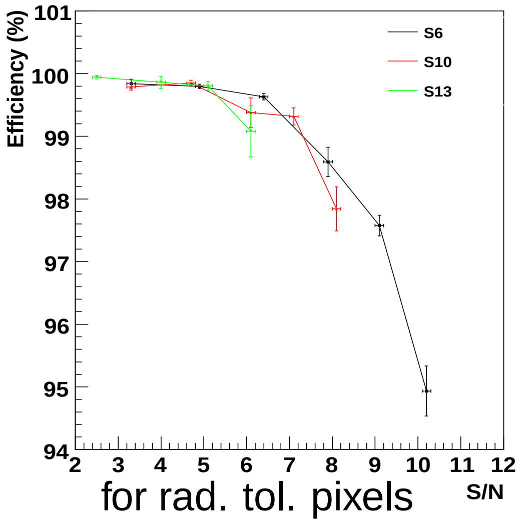
## Comparison of det. efficiency & fake hit rate vs S/N for all sub-arrays :

M22 digital



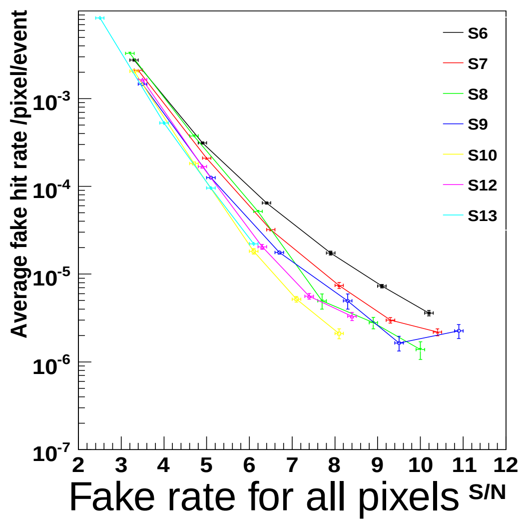

Det. eff. for all pixels

M22 digital



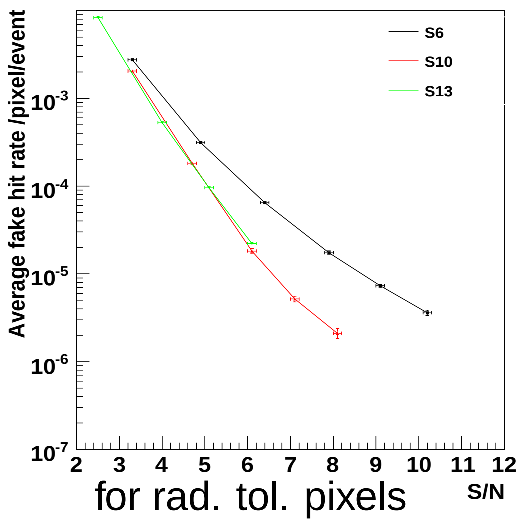

for rad. tol. pixels

M22 digital



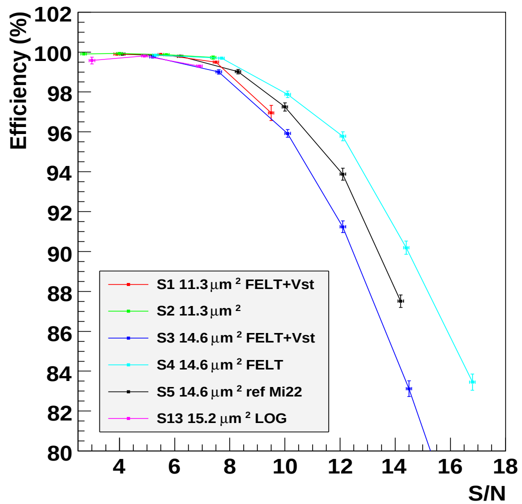

Fake rate for all pixels

M22 digital

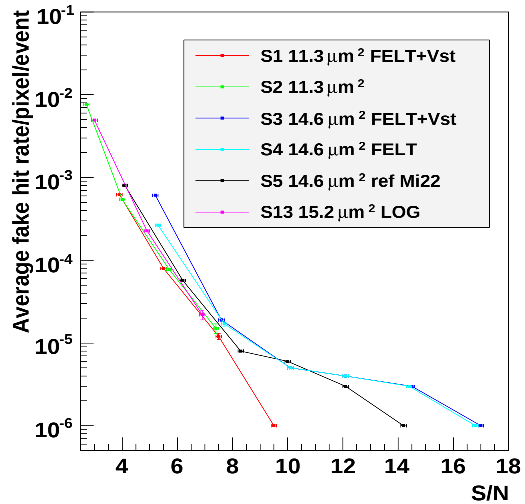



for rad. tol. pixels

M22bis digital Efficiency




M22bis digital fake hit rate




- ▷ **Observed performance differences and analysis maturity don't allow yet to decide for the BT pixel architecure**
- ▷ **Radiation tolerance assessment needed to converge on most adequate pixel design**

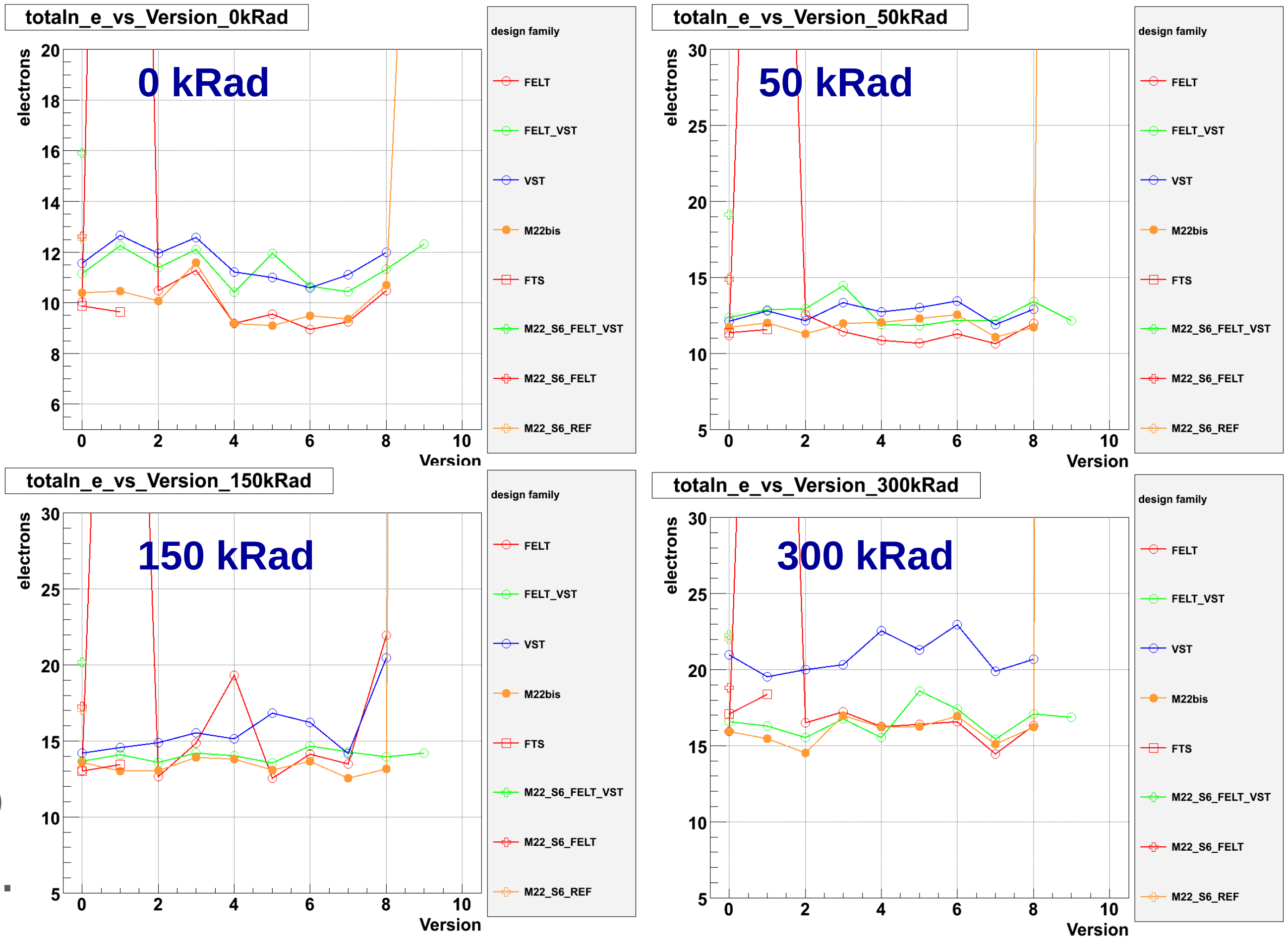
## Why may radiation tolerance be a conCERN ?

- *max. annual doses at DESY* $\lesssim 10^{11}$ *e*$^{-}$ *(few GeV)/yr* $\Rrightarrow$ $\lesssim$ *3.5 kRad &* $10^{10}$ $n_{eq}/cm^2$
- *max. annual doses at CERN* $\lesssim$ *several* $10^{12}$ $\pi^{-}$ *(*$10^2$ *GeV)/yr* $\Rrightarrow$ $\lesssim$ *O(*$10^2$*) kRad & O(*$10^{12}$*)* $n_{eq}/cm^2$

## Assessing rad. tolerance (10 keV X-Rays ) in lab.:

▷ *ex. of S6 (M22) variants at 20°C*

- *before irradiation* $\gtrsim$ *9.5 e*$^{-}$ *ENC*
- *after 50 kRad* $\gtrsim$ *11 e*$^{-}$ *ENC*
- *after 150 kRad* $\gtrsim$ *13 e*$^{-}$ *ENC*
- *after 300 kRad* $\gtrsim$ *15 e*$^{-}$ *ENC*



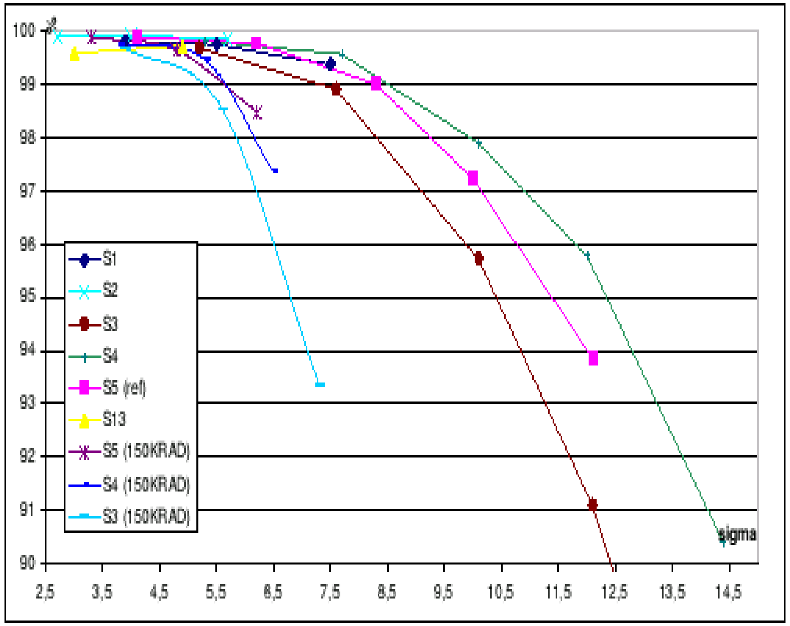

▷▷▷ **Excellent noise performance**

*(but source of noise increase still under study )*

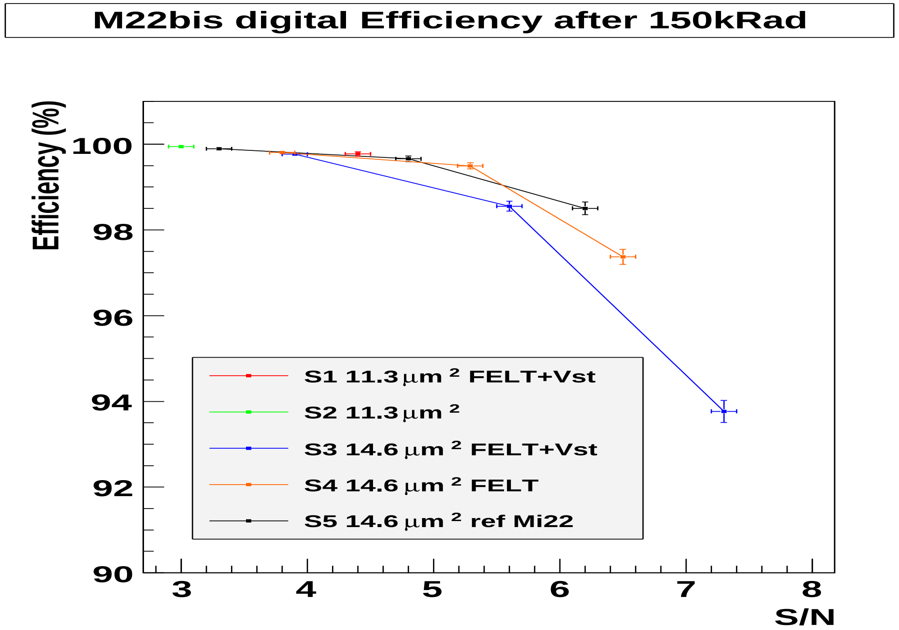
**... watch Charge Collection Efficiency ...**

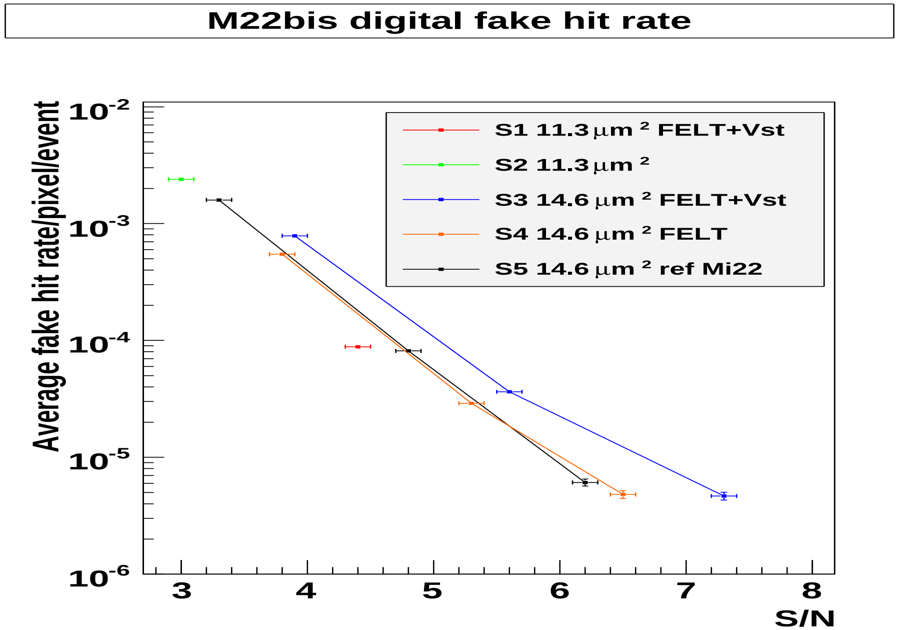
*A. Dorokhov, IPHC, Strasbourg,* 12

## Beam test results with chips irradiated with 150 kRad :




*Det. eff. vs SNR before and after irradiation (150 kRad)*

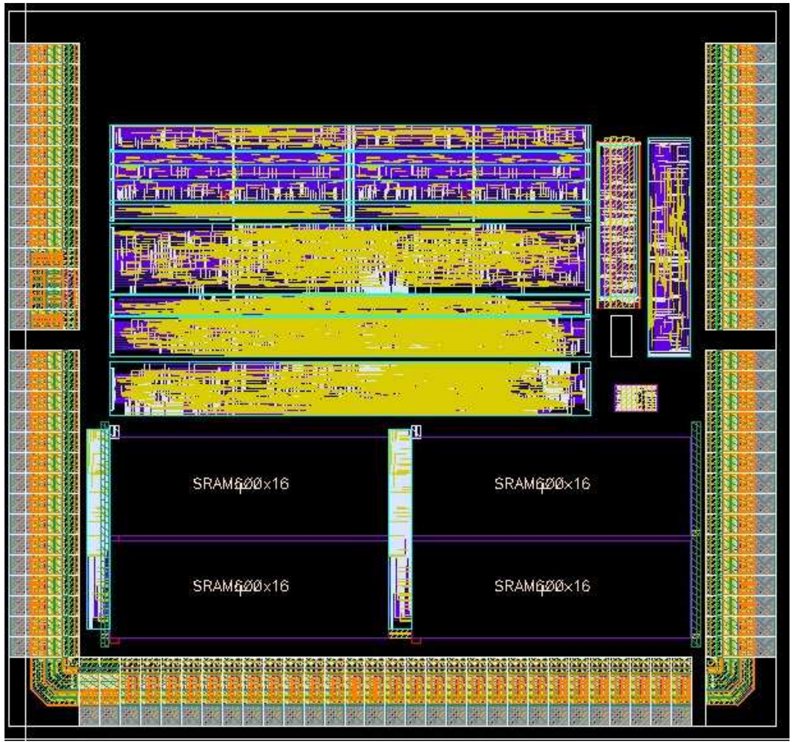



▷▷▷ **Pixel & column parallel architecture with integrated discriminators**

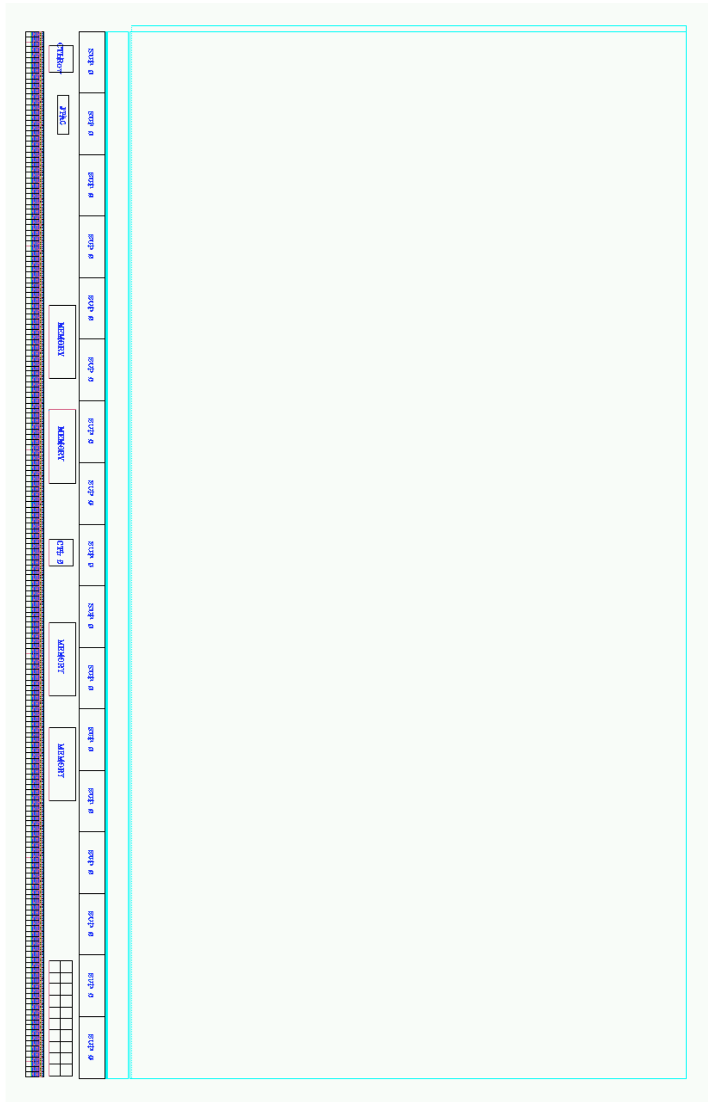
**Fully Validated !!!**

- **1st chip (SDC-2/SUZE-01) with integrated $\emptyset$ and output memories (no pixels) :**
  - *2 step, raw by raw, logic :*
    - *step-1 (inside blocks of 64 columns) :*
      *identify up to 6 series of $\leq$ 4 neighbour pixels per raw*
      *delivering signal $>$ discriminator threshold*
    - *step-2 : read-out outcome of step-1 in all blocks*
      *and keep up to 9 series of $\leq$ 4 neighbour pixels*
  - *4 output memories (512x16 bits) taken from AMS I.P. lib.*
  - *surface $\sim$ 3.9 $\times$ 3.6 mm$^2$*



- **Test results summary :**
  - *back from foundry end of Sept. '07 $\rightarrowtail$ (lab) tests completed*
  - *design performances reproduced up to 1.15 $\times$ design read-out frequency ($T_{room}$) :*
    *noise values as predicted, no pattern encoding error, can handle $>$ 100 hits/frame at rate $>$ $10^4$ frames/s*
- **Still to do :** *evaluate radiation tolerance (latch-up ) of ouput memories*

# Main Parameters of the Final Sensor : TC/MIMOSA-26



- **Autumn 2008 : fabrication of MIMOSA-26 = Final Sensor (TC )**

※ **IDC/M-22 (binary outputs) complemented with $\emptyset$ (SDC-2/SUZE-01)**

※ best performing (rad. tol. ) pixel architecture of IDC/M-22(bis)

$\hookrightarrow$ wait for Octobre beam test final results

※ **Active surface : 1152 columns of 576 pixels (21.2 x 10.6 mm$^2$)**

$\hookrightarrow$ **extension of IDC & SDC-2 from 128 col. to 9 x 128 col.**

※ **Pixel pitch : 18.4 $\mu m \rightarrowtail \sim$ 0.7 million pixels**

$\hookrightarrow$ $\sigma_{sp} \gtrsim$ **3.5 $\mu m$ $\Rrightarrow$ pointing resolution $\sim$ 2 $\mu m$ on DUT surface**

※ **Integration time $\sim$ 110 $\mu s \rightarrowtail \sim$ 10$^4$ frames / second**

※ $\emptyset$ based on 18 groups of 64 columns and assuming $\leq$ 9 "clusters" per row

※ Chip dimensions : $\sim$ 21 x 12 mm$^2$

※ Data throughput: 1 output at $\geq$ 80 Mbits/s or 2 outputs at $\geq$ 40 Mbits/s

※ Engineering run : 2 (+ $\leq$ 4) wafers of $\gtrsim$ 30 chips expected (if yield $\sim$ 50 % )

※ **Design under way $\Rrightarrow$ planned submission date $\geq$ mid-November '08**

- **Col. // architecture with discri. outputs validated for m.i.p. detection on real scale (*128 col. of final length* ) :**
  - *read-out frequency* $\sim 10^4$ *frames/s* ✓
  - *pixel noise* $\sim$ *10–13 e*$^-$ *ENC* $\Rrightarrow$ *S/N* $\sim$ *17–22 (MPV)* ✓
  - $\epsilon_{det} >$ *99.5 % with fake rate* $\sim$ *O(10*$^{-4}$ *- 10*$^{-5}$*), similar to MIMOSA-16* ✓
  - $\sigma_{sp} \gtrsim$ *3.5* $\mu m$ $\Rrightarrow$ *resolution on impact position on DUT surface* $\lesssim$ *2* $\mu m$ ✓
- **$\varnothing$ $\mu$-circuit with output buffers validated for 128 col. at read-out frequency $>$ nominal value** ✓
- **Radiation tolerance :**
  - *achieved ionising radiation tolerance of pixel array sufficient for use of BT at CERN, FermiLab, ...* ✓
    *(source of noise increase still being investigated )*
  - *under way : non-ionising radiation tolerance assessment and latch-up tests of output memories*

$\Rrightarrow$ **TC $\equiv$ final sensor (combining col. // architecture with $\varnothing$ $\mu$-circuit) :**

- *design under way (crucial issues : extension from 128 to 1152 col. of IDC combined with SDC-2 )*
- *in absence of unexpected pb, submission will occur* $\gtrsim$ *mid-Novembre '08*

$\hookrightarrow$ **TC sensor tests expected to start in January 2009**