

TPC Large Prototype cosmic trigger and Micromegas panels

D. Attié, P. Colas, E. Delagnes, M. Dixit, A. Giganon, M. Riallot, F. Senée, S. Turnbull

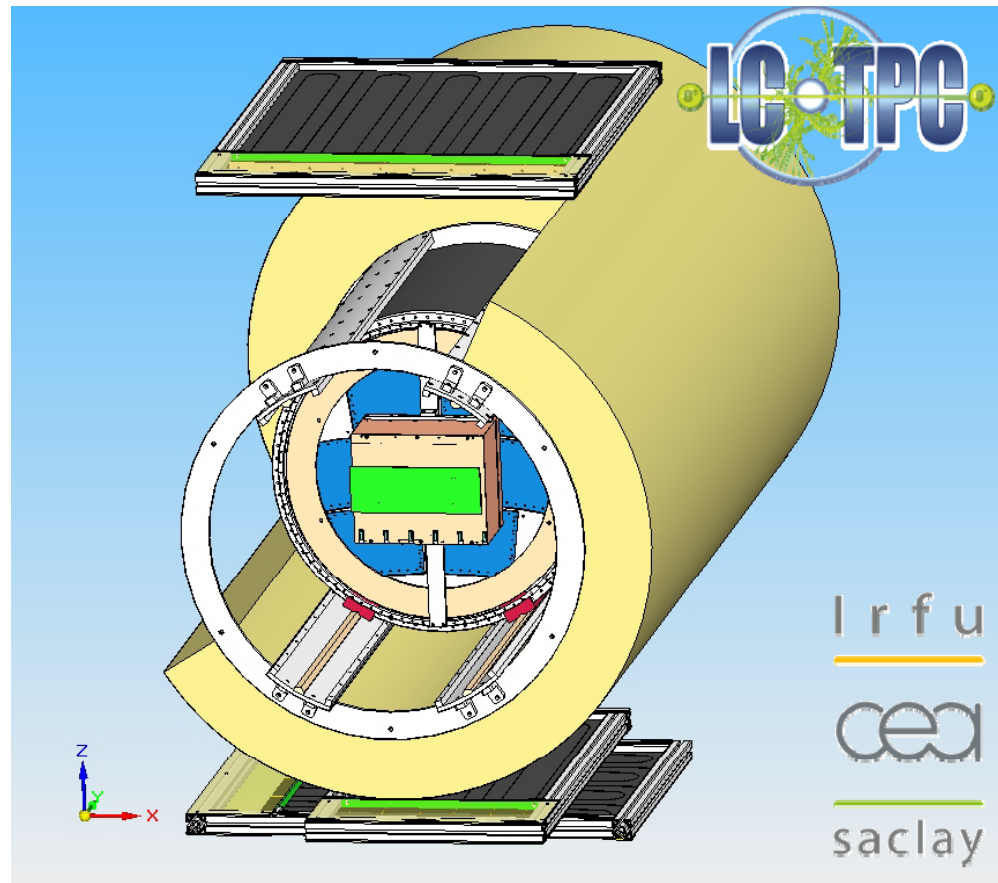


Large Prototype cosmic trigger

Micromegas Large Prototype panels

Studies on resistive coatings

Installation at DESY



l r f u

cea

saclay

Large Prototype cosmic Trigger

Th. Chaminade, P. Colas, M. Karolak, S. Hervé, F. Pierre, J.M. Reymond, (Saclay)

T. Matsuda, K. Dehlmét (KEK, DESY)

Y. Kudenko (INR Moscou)

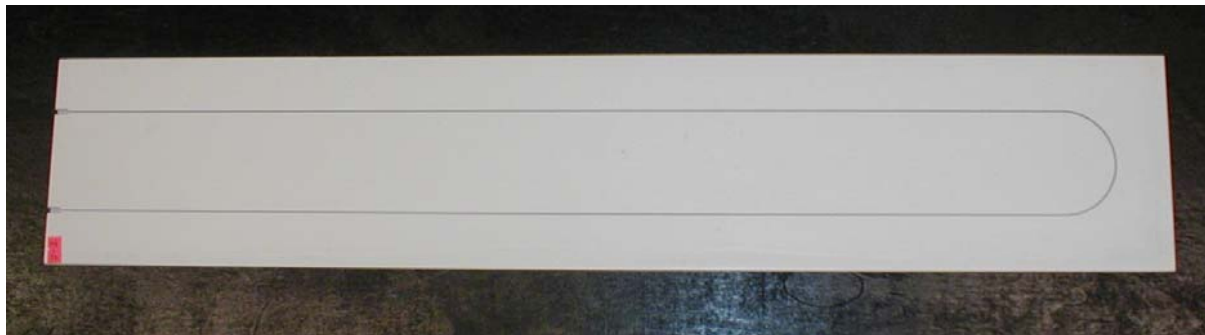
G. De Lentdecker, X. Janssen (Bruxelles)

Magnetic field > 0.3 T around the magnet: standard PMs cannot be used.

T. Matsuda -> use MPPC (=SiPM)

Y. Kudenko -> extrude Scint. and add groove for scintillating fiber. 12 slab design : 5 on top, 3 bottom, 4 transverse

MPPC requires constant temperature: work out a thermoregulation with Peletier devices (JM Reymond)

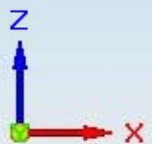
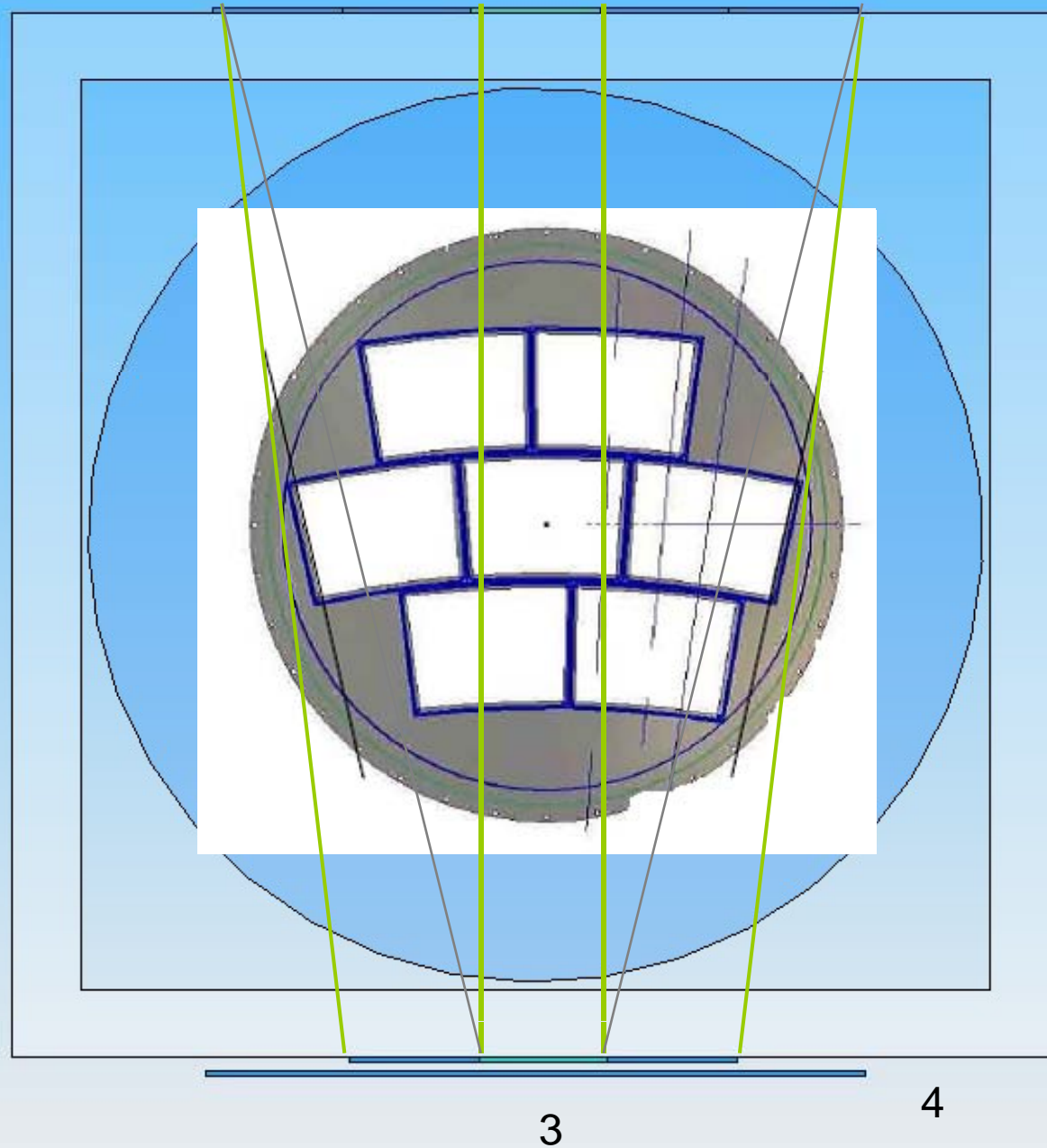


An additional contribution from Saclay to EUDET



5

Many possible combinations, for instance:
1 top + 1 bottom :
central region of central panel
3 top + 1 bottom :
radial tracks on central panels
3 top + 3 bottom :
vertical tracks on most of the central region
Requires a 'bridge' to support the magnet and its movement system.

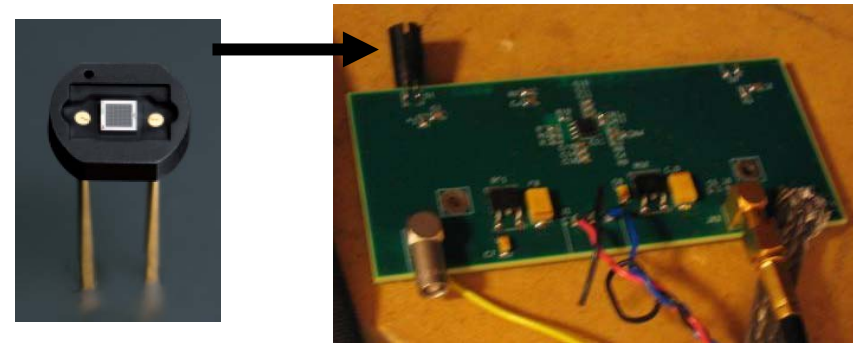


Integrated cards add the signals of 2 MPPCs and amplify the signal with a gain of 40. The cards provide regulated supply to the amplifiers.

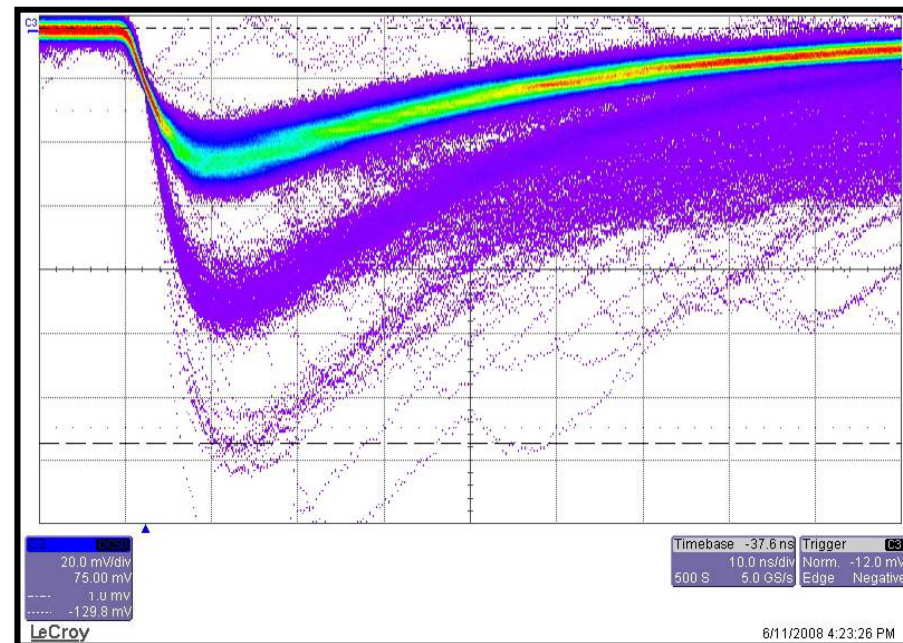
Typical signals of 50 mV per p.e. are obtained. Single rates at 200 mV threshold are below a kHz.

The Peletier thermoregulation can stabilize the temperature to 0.01°, and can follow changes of 10 degrees over 12 hours.

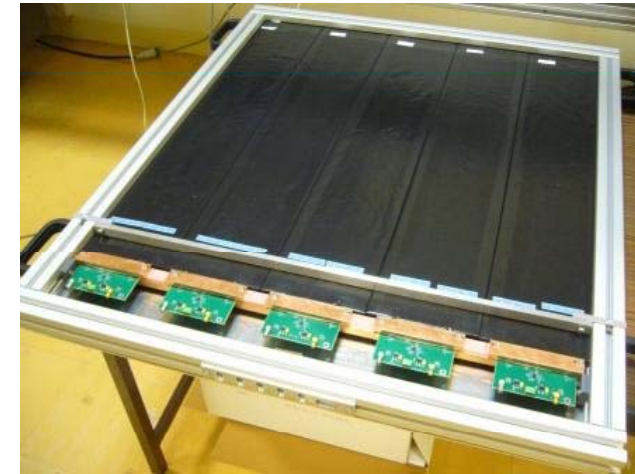
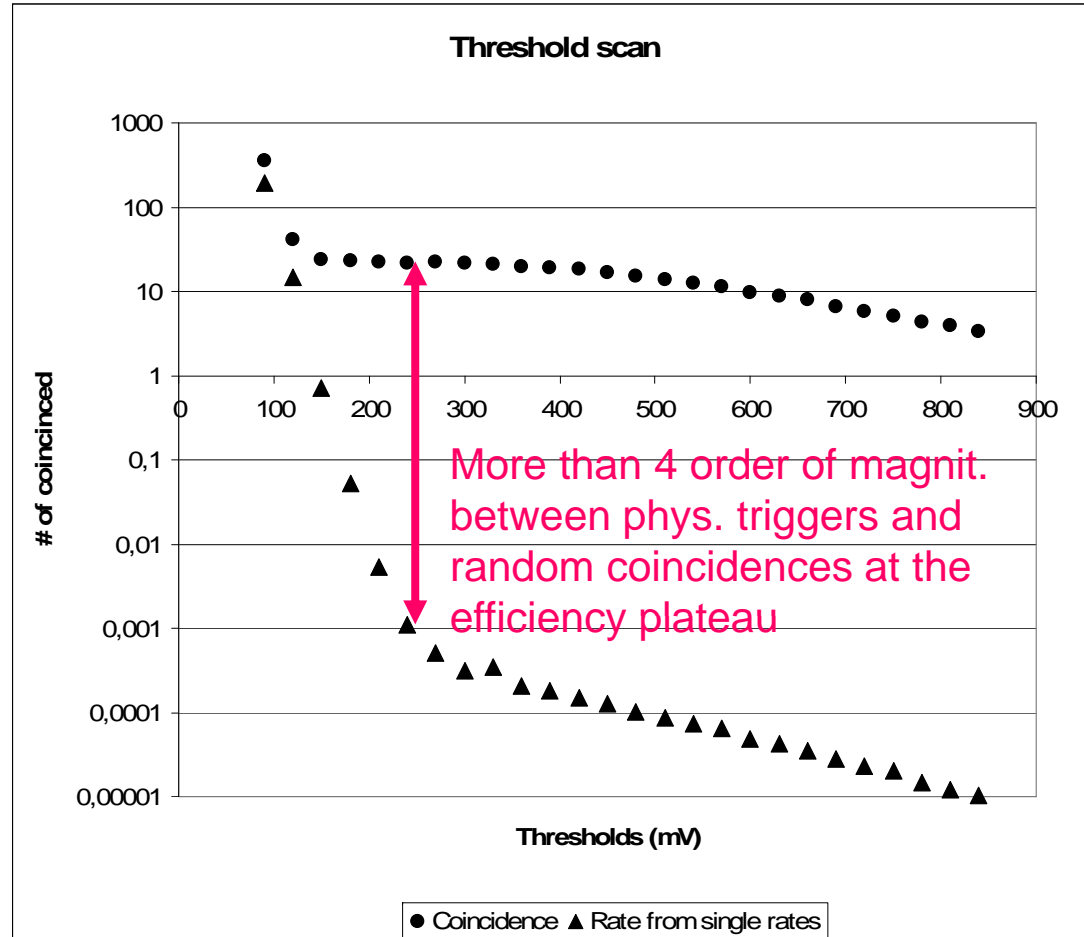
There is one supply cable per module and one signal cable per slab.



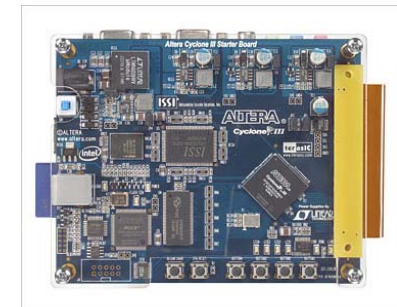
MPPC=SiPM (with Peletier effect thermoregulation)



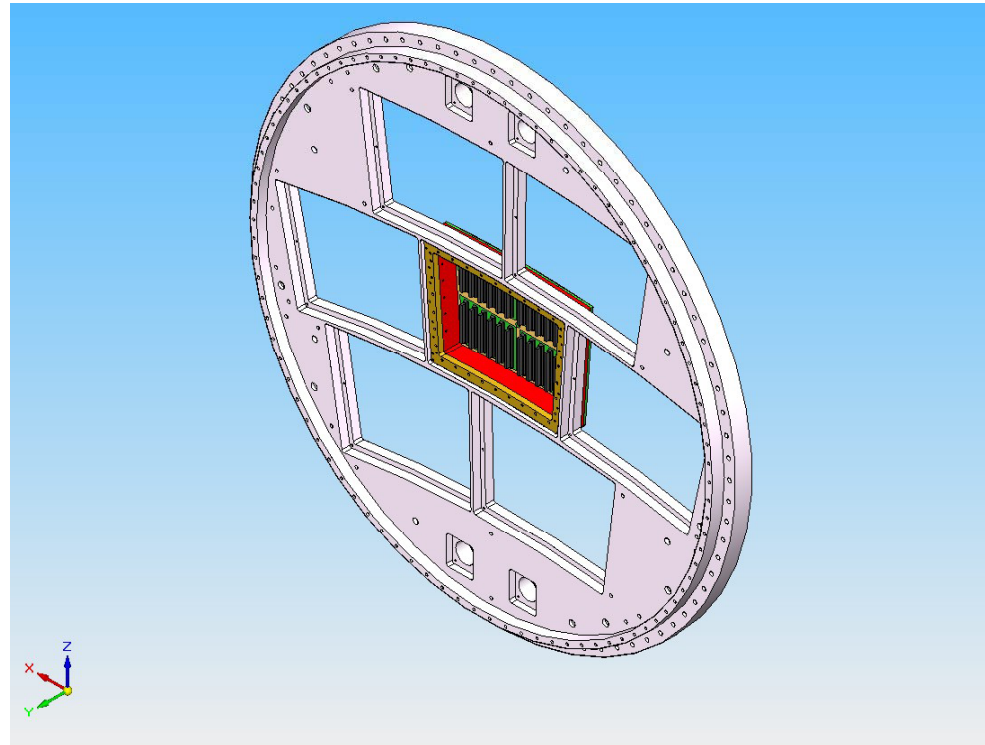
Large Prototype: a High-tech cosmic trigger



Installation at DESY July 7-10
next: FPGA logic



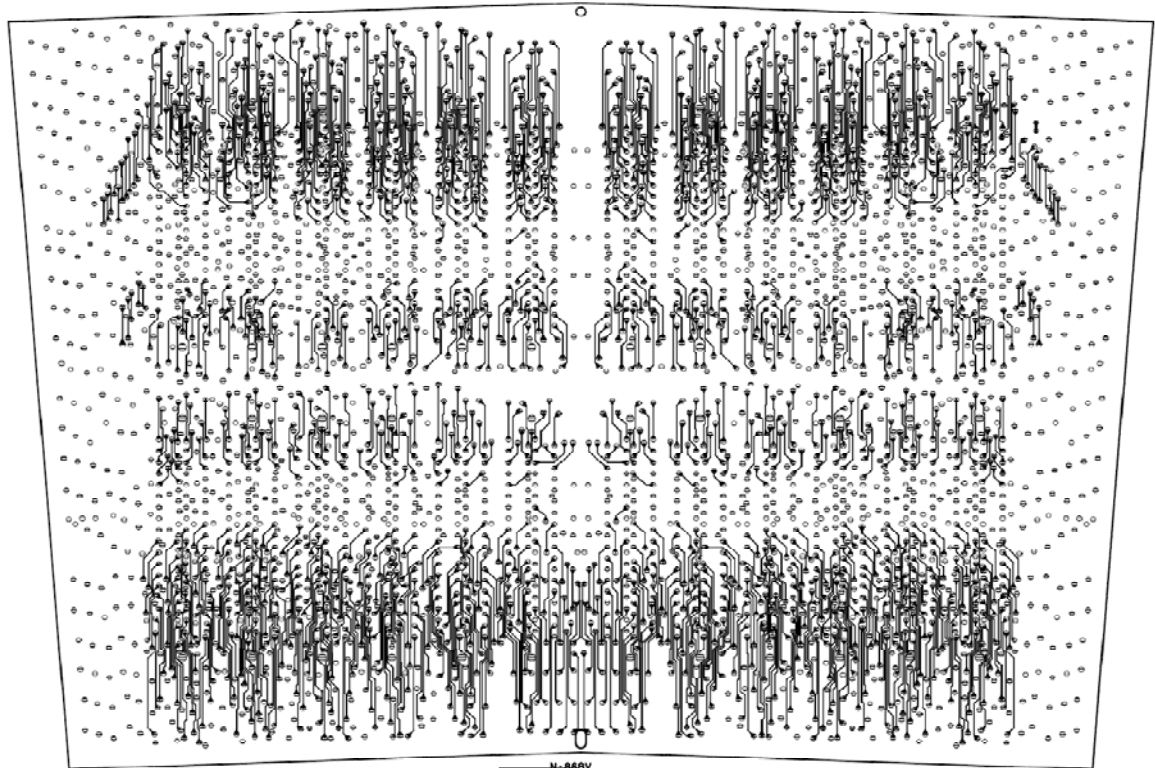
Panels: in 2008-2009: 1 panel at a time in the centre of the detector. Others are dummy. Also plans for trying a multichip InGrid+TimePix panel (see D. Attié's talk this morning)



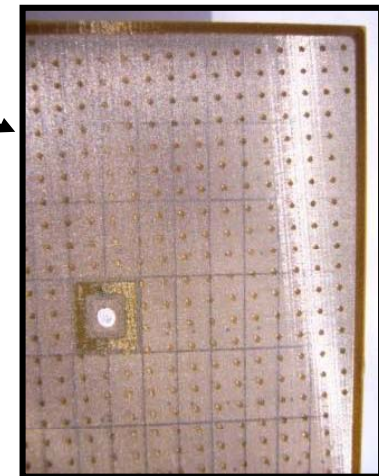
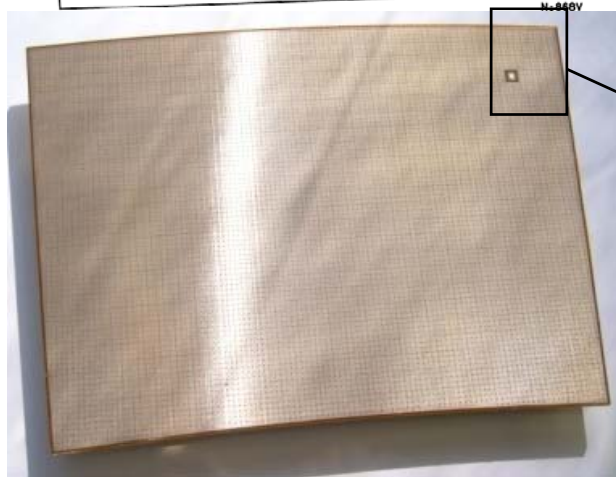
The panels

PCBs have been produced
4 with the Saclay routing in
6 layers (delivered early
June)

4 with the CERN routing
with 4 layers (August)



EUDET annual - Oct. 6, 2008



P. Colas - Large Prototype panels

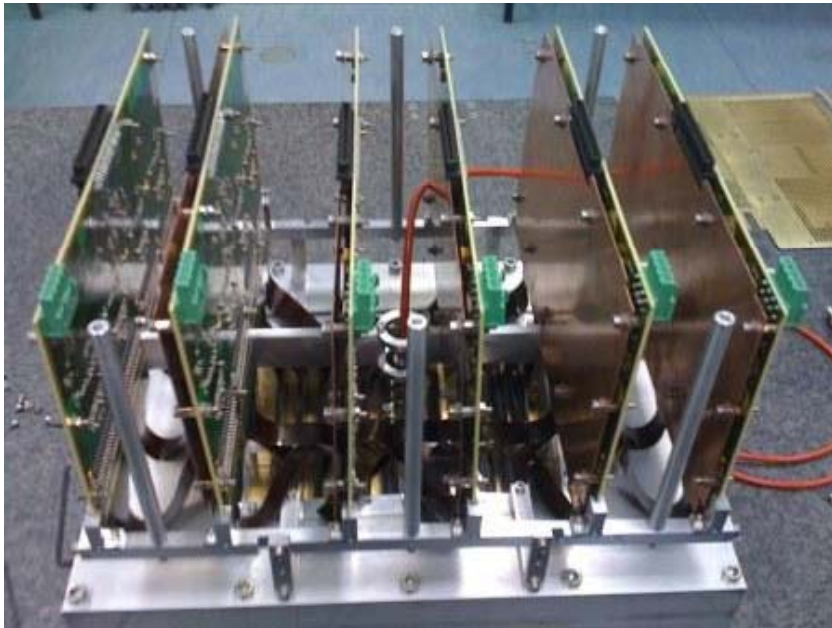
A first 'bulk Micromegas' panel (without resistive foil) and a second, with a resistive carbon-loaded kapton, have been produced at CERN,

(Rui de Oliveira)



Mechanical support of the electronics

Shielding, Faraday cage, flat cables, gasbox...



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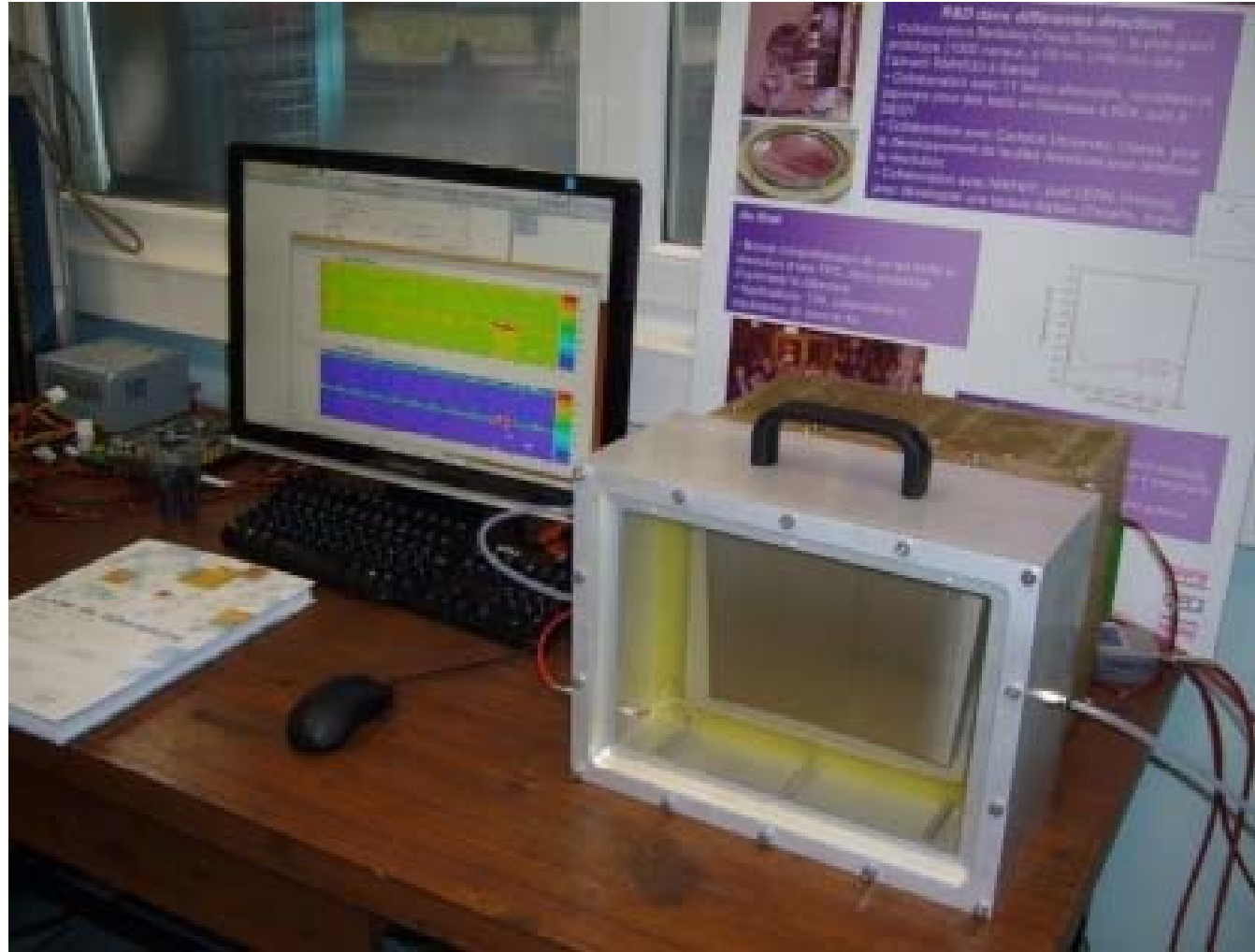
P. Colas - Large Prototype panels

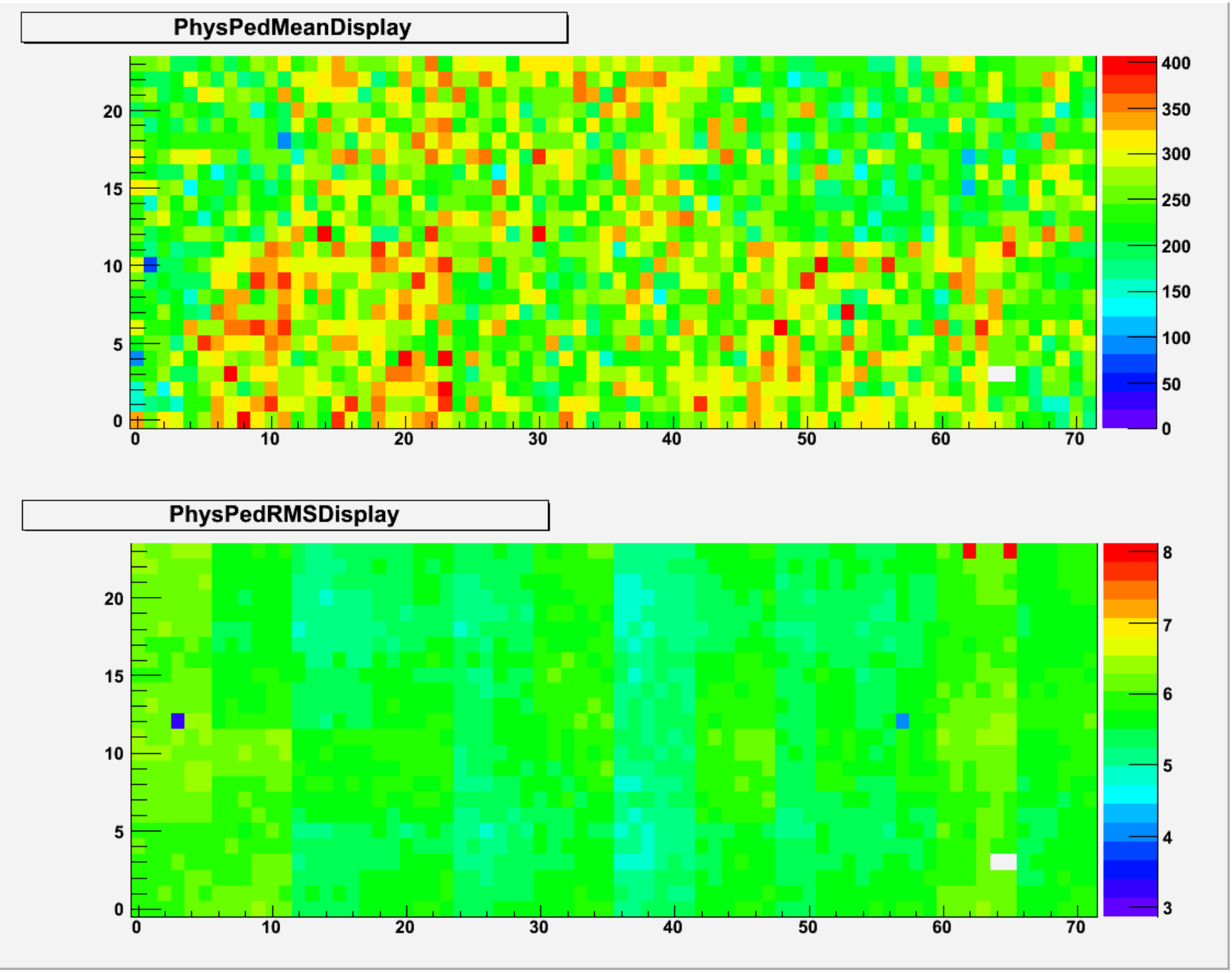


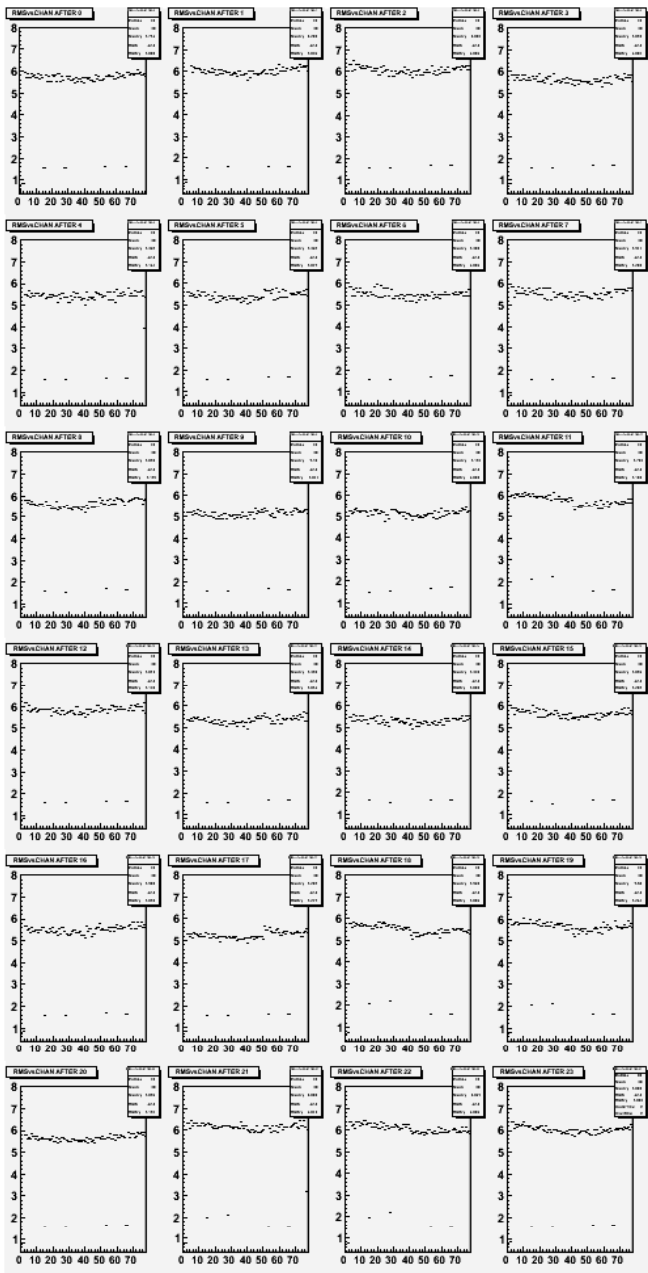
Test setup at Saclay

Tests in gas
were performed
in our lab

(one faulty pad
had to be
disconnected)

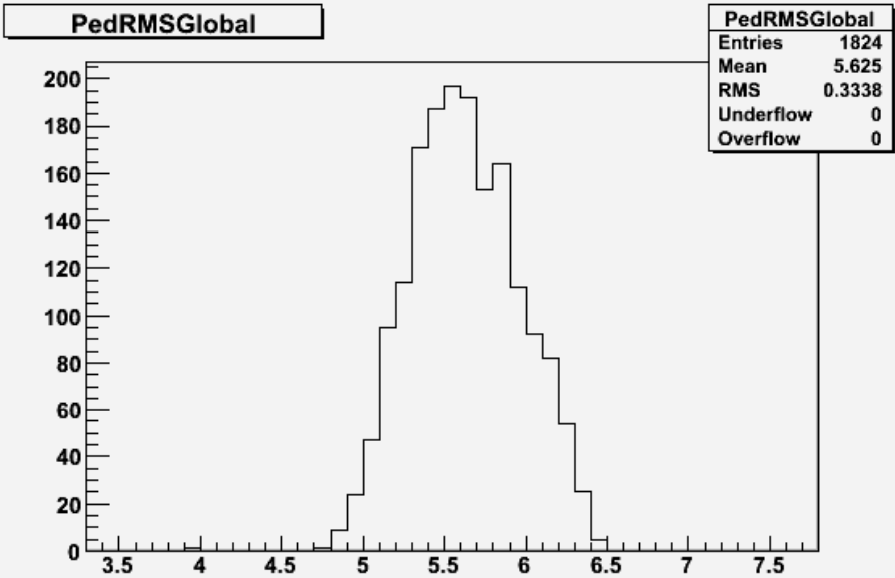
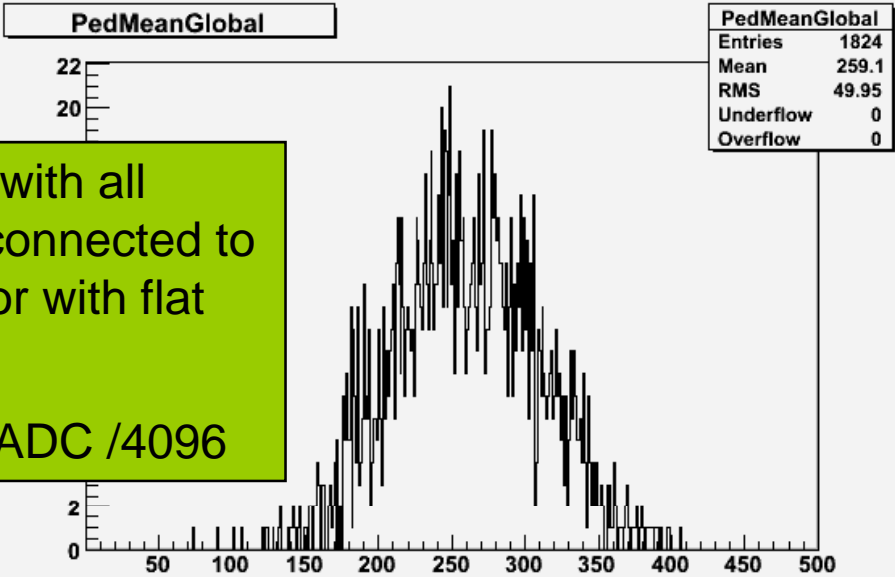




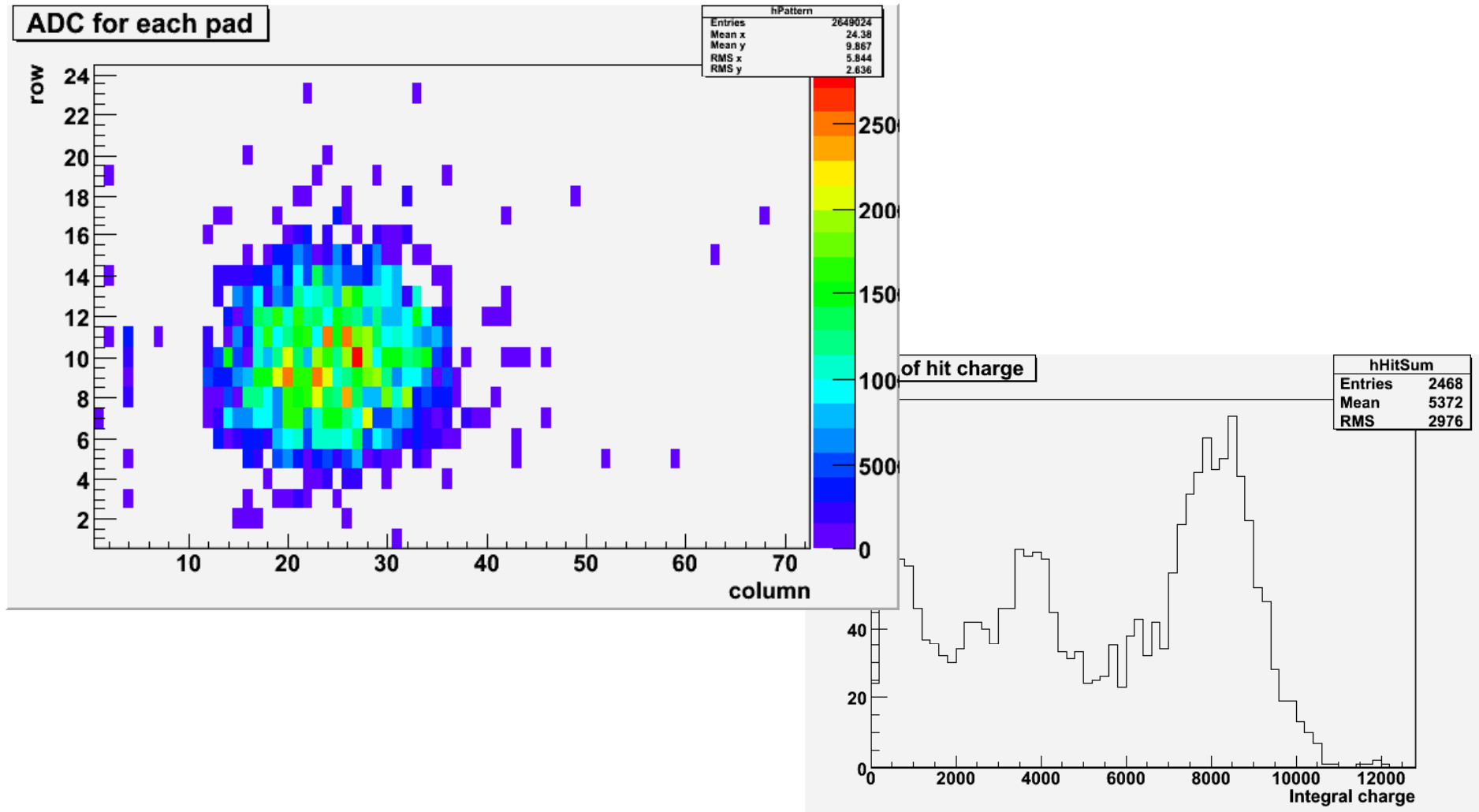


Pedestals with all channels connected to the detector with flat cables

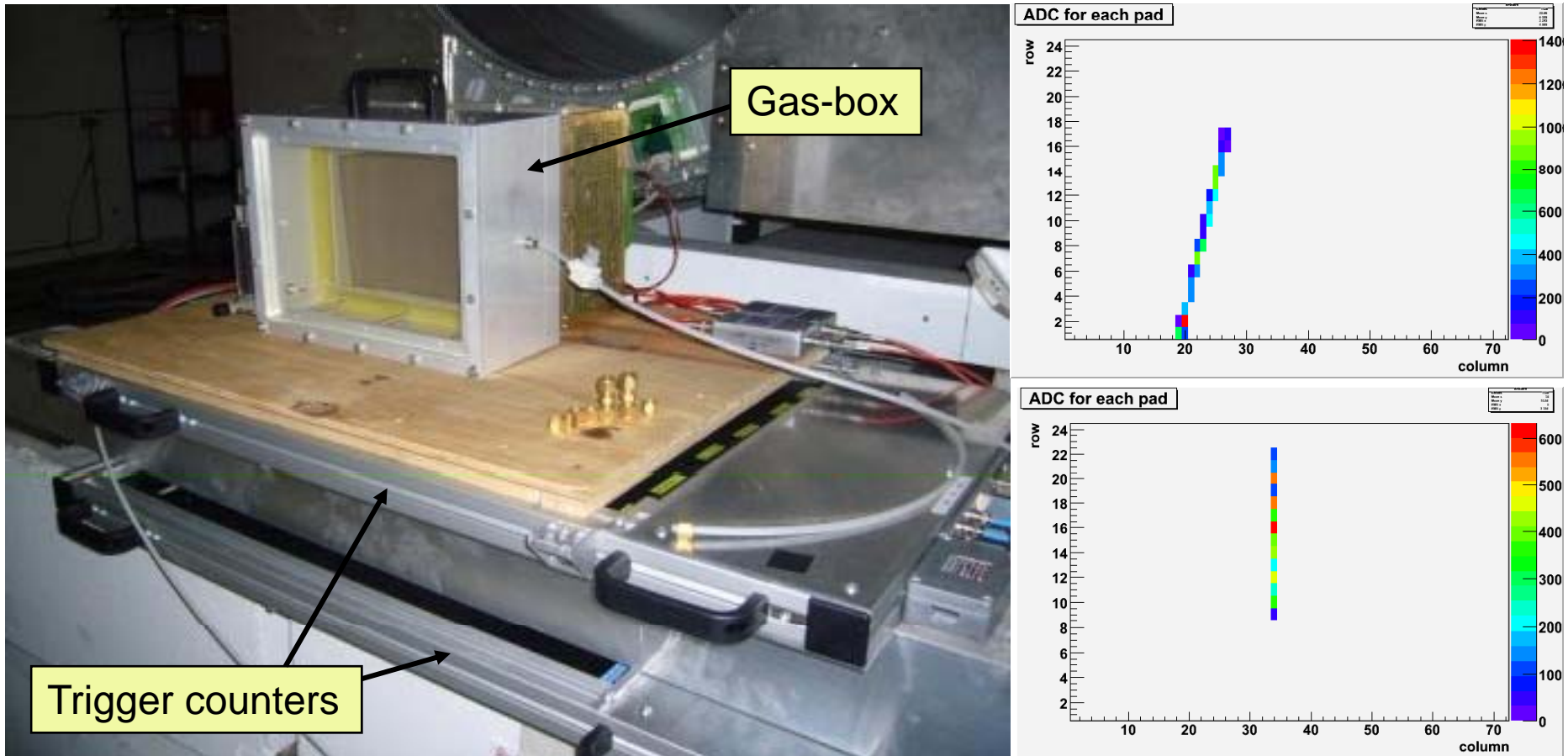
$\langle \sigma \rangle = 5.6 \text{ ADC} / 4096$



Tests at Saclay with a ^{55}Fe source

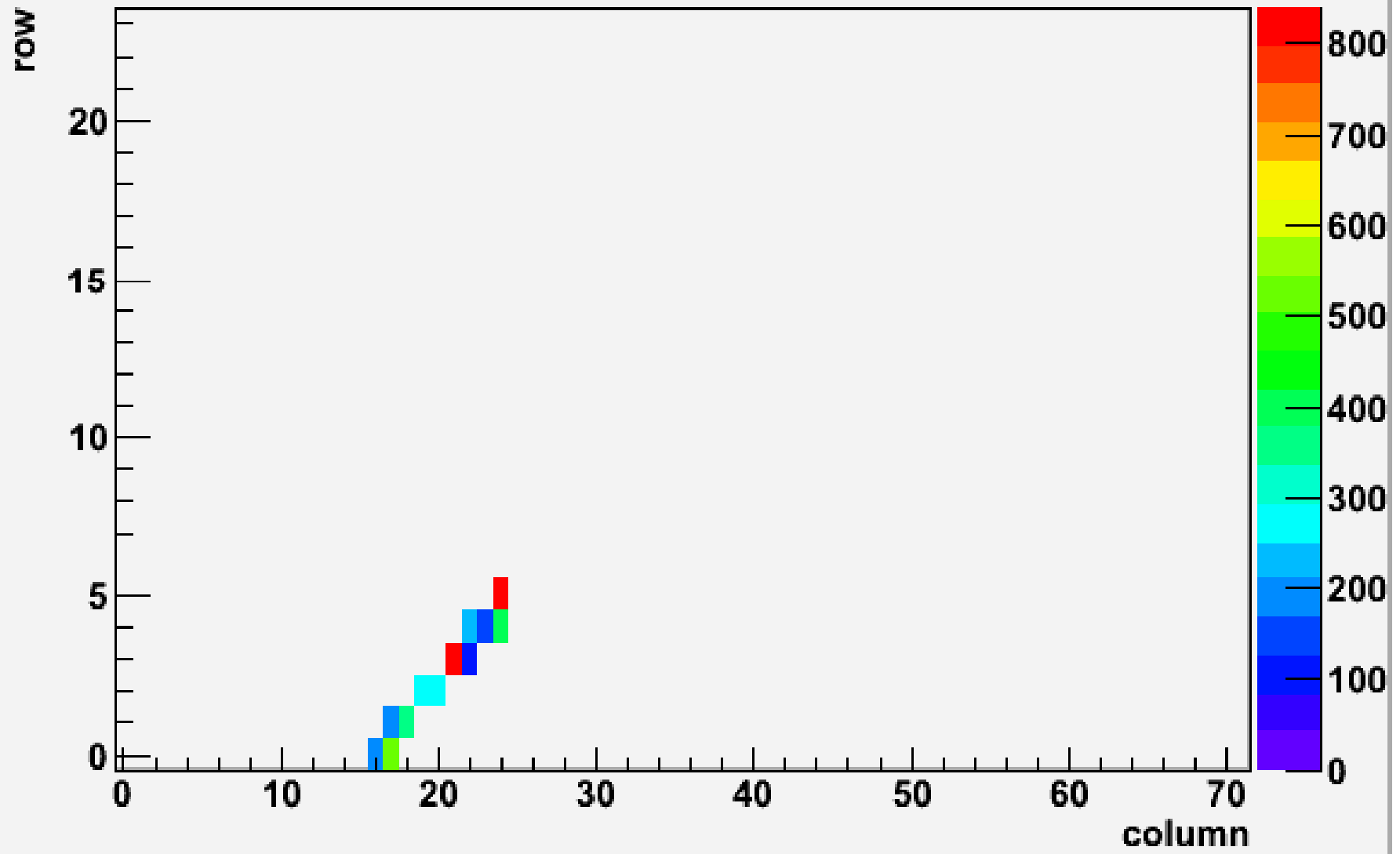


In-situ TEST at DESY



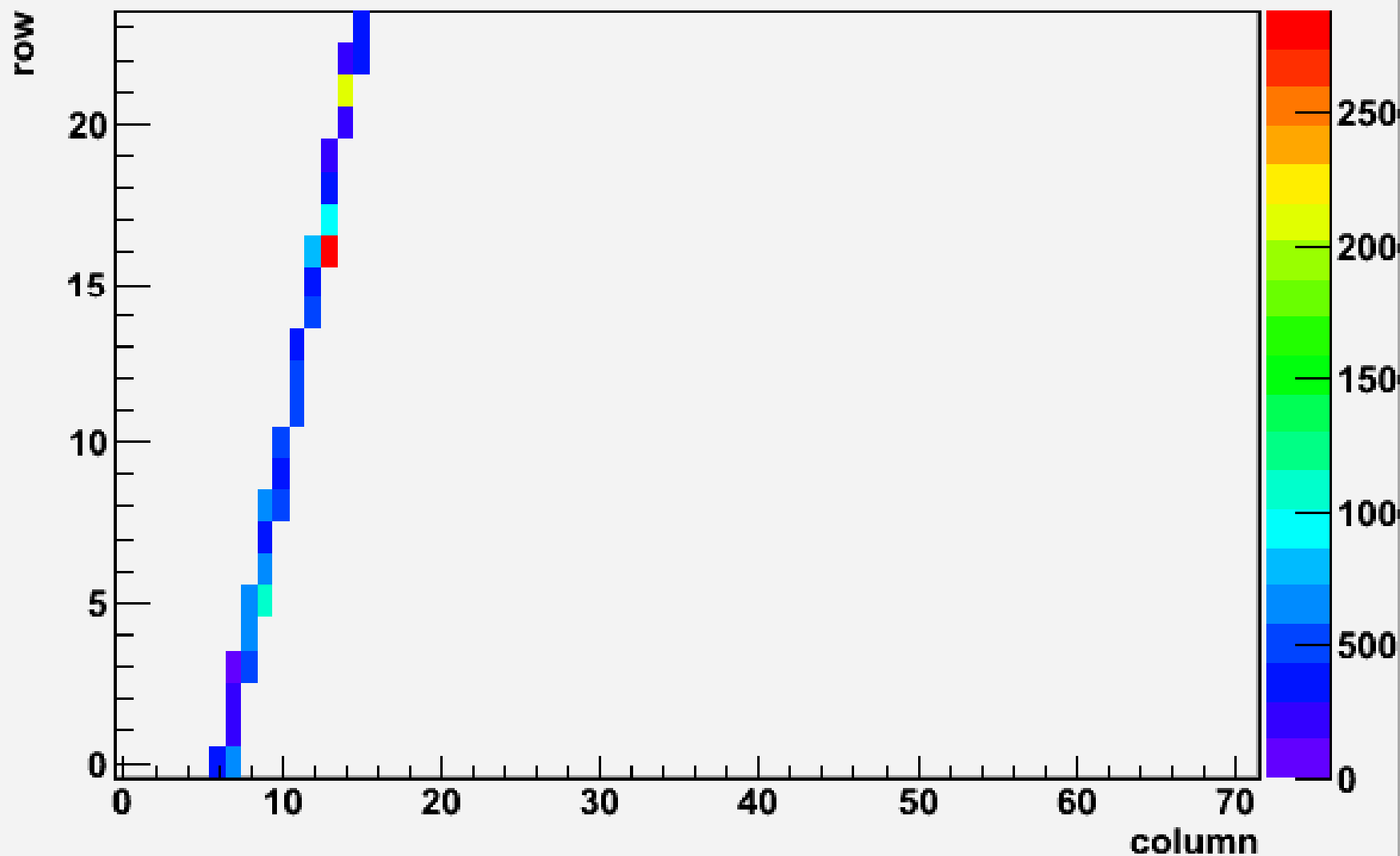
ADC for each pad

SUMMARY	
Mean x	20.89
Mean y	2.487
RMS x	2.728
RMS y	1.718

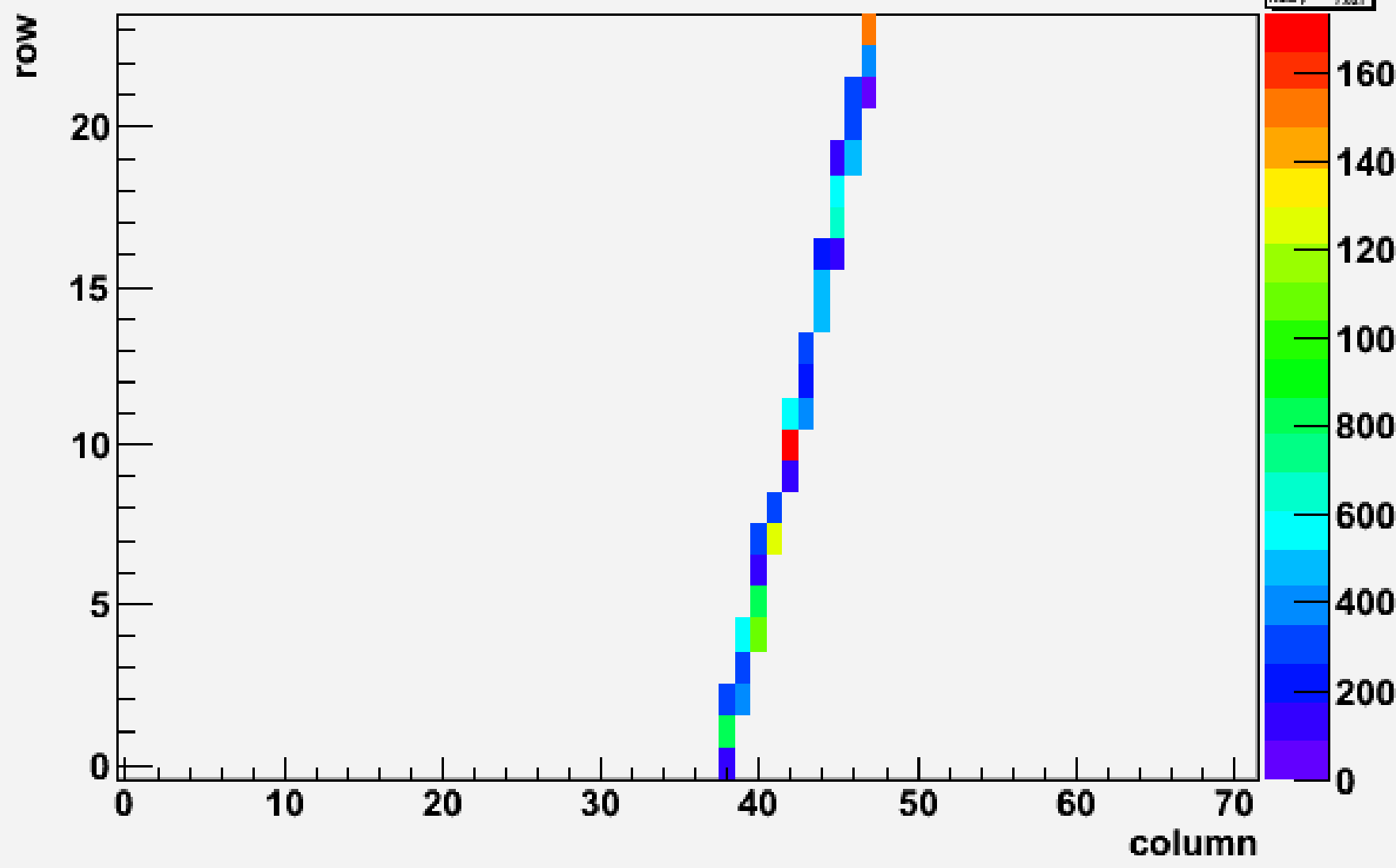


ADC for each pad

SUMMARY	
Entries	1120
Mean x	11.28
Mean y	12.28
RMS x	2.677
RMS y	0.78



ADC for each pad



Several techniques are being tested for the resistive coating

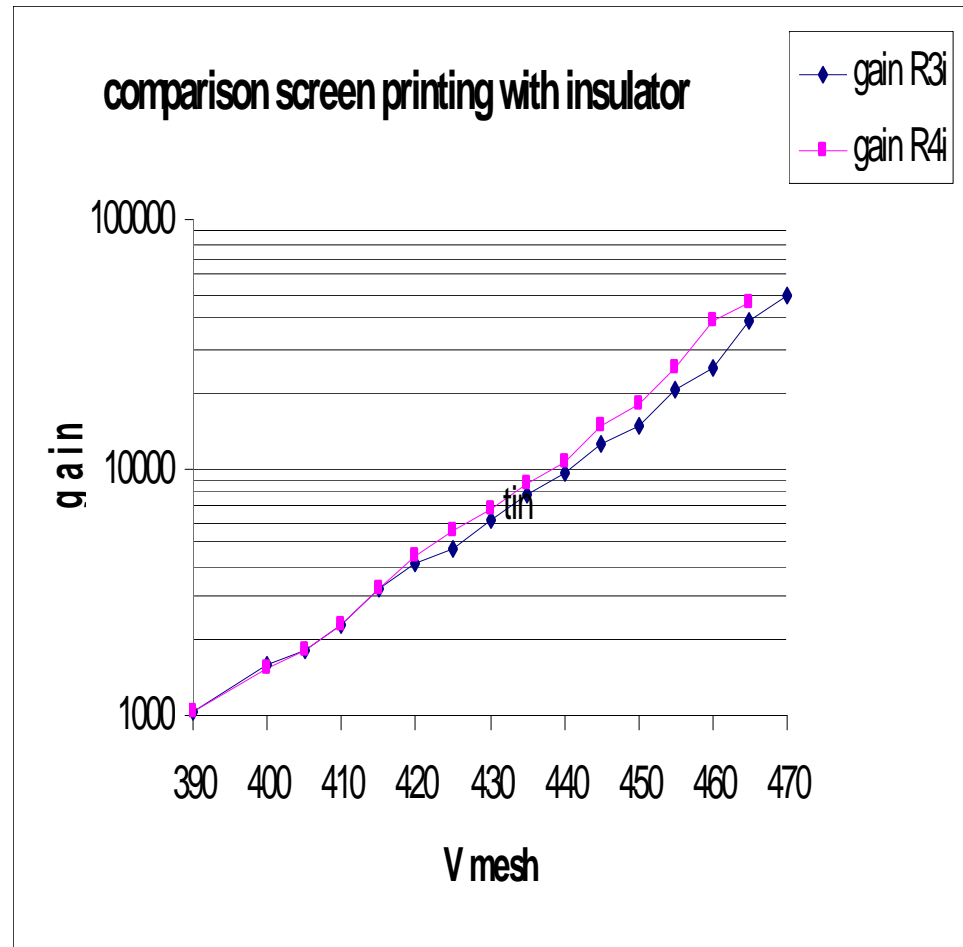
- 1) Carbon-loaded kapton. An old technique first tested in Carleton, using a Dupont film 1 MOhm/sq. Improvements on application of the resistive foil and switch to bulk.

First results promising. One panel recently produced.



2) Prepreg+ screen printing

This has been tried at CERN. 2 prototypes of 10x10 cm (2 and 8 MOhm/sq) have been tried at Saclay. There is not clear evidence that they are spark protected. Even one of the detector has been damaged by the HV during the test. Still such a layer will be applied to a CERN panel.



Plasma deposition of thin layers (N. Wyrsh, Neuchatel, used for SiProt)

Preliminary tests going on. Next step: make a small bulk 12x14 cm² with 2 layers of different resistivity, and then cover a PCB with pads and make a bulk out of it



Future plans



Take beam data in the magnet in the period of weeks 44-45-46 (+1?) depending on the field cage status. Then other periods with various PCBs in 2009.

Start R&D for electronics on a mezzanine PCB. Should be ready for early 2010.

- R&D to optimize protection compactness
- Development to test AFTER chips at the wafer level
- new card design

Make 7 fully equipped modules (250 Watts)

Start cooling and integration studies

