

Status of Saclay activities on TimePix

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EUDET

Detector R&D towards the International Linear Collider

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sacly



1. Micro TPC using single TimePix chip/Micromegas

- Data samples
- Description

2. Deliverable: TimePix panel for the ILC Large Prototype

- Description of the 2x4 matrix
- Tests and issues
- Current status and next steps

Conclusion

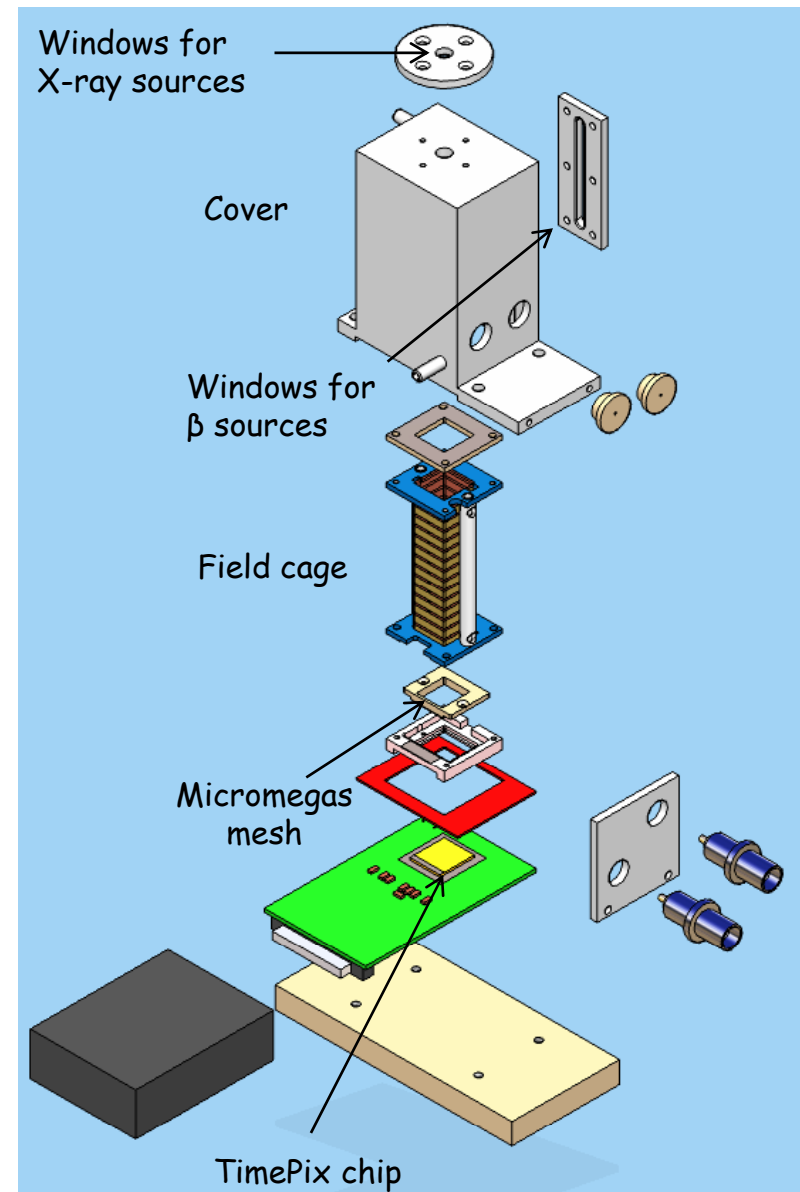
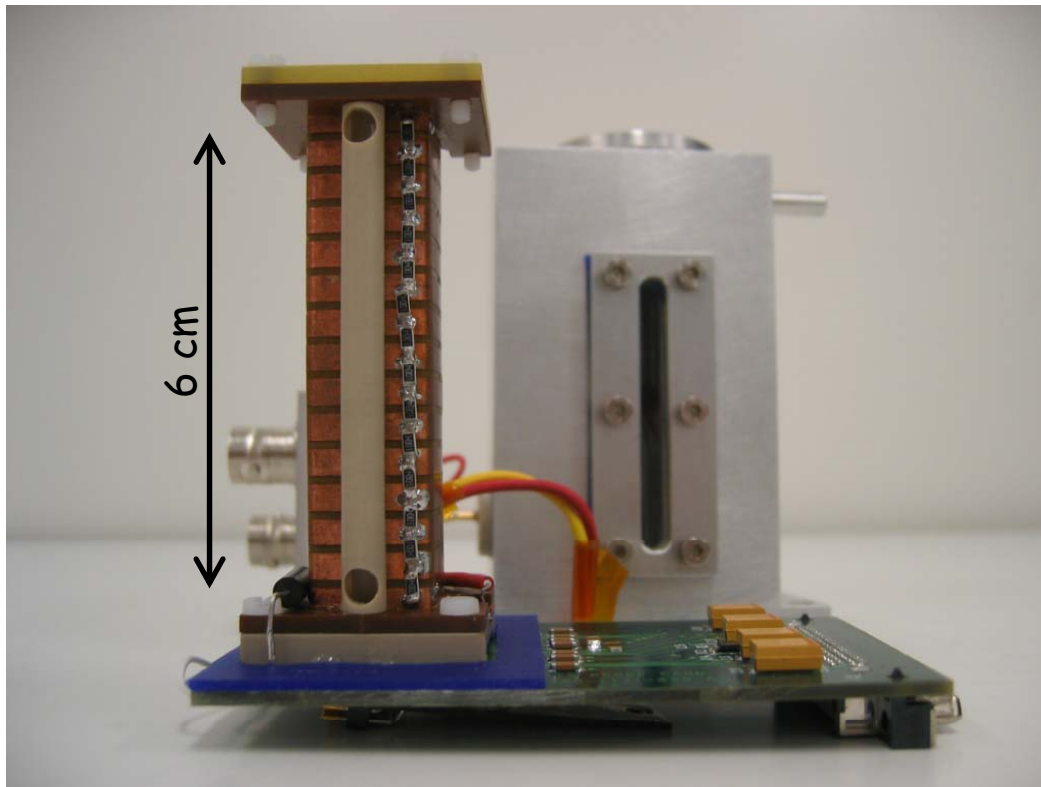


1. Micro TPC using single TimePix chip/Micromegas



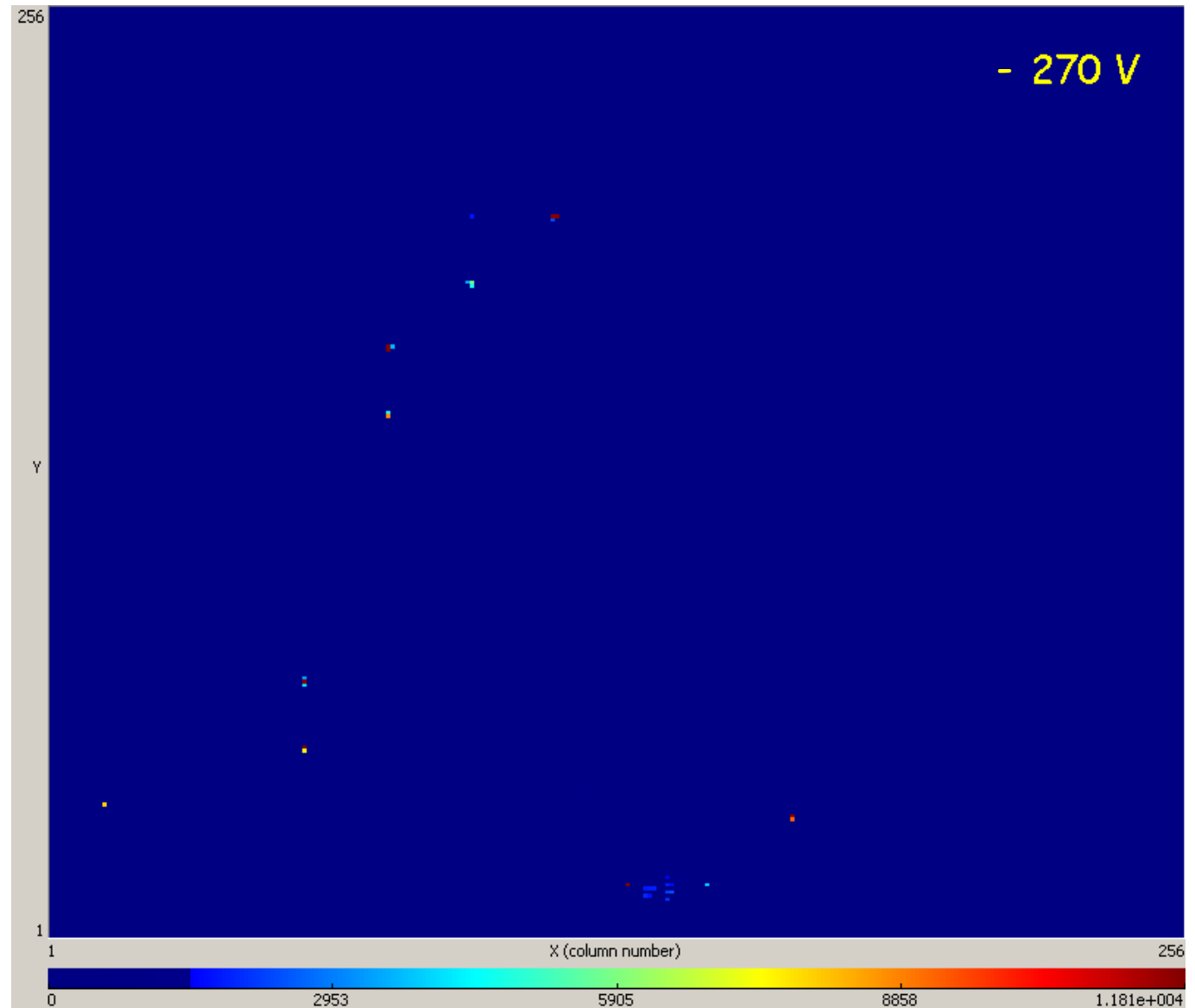
Micro-TPC using single TimePix chip/Micromegas

- Micro-TPC with a 6 cm height field cage
- Size : 4 cm × 5 cm × 8 cm
- Read out by MUROS or USB1.2 devices
- Two detectors are available now at Saclay





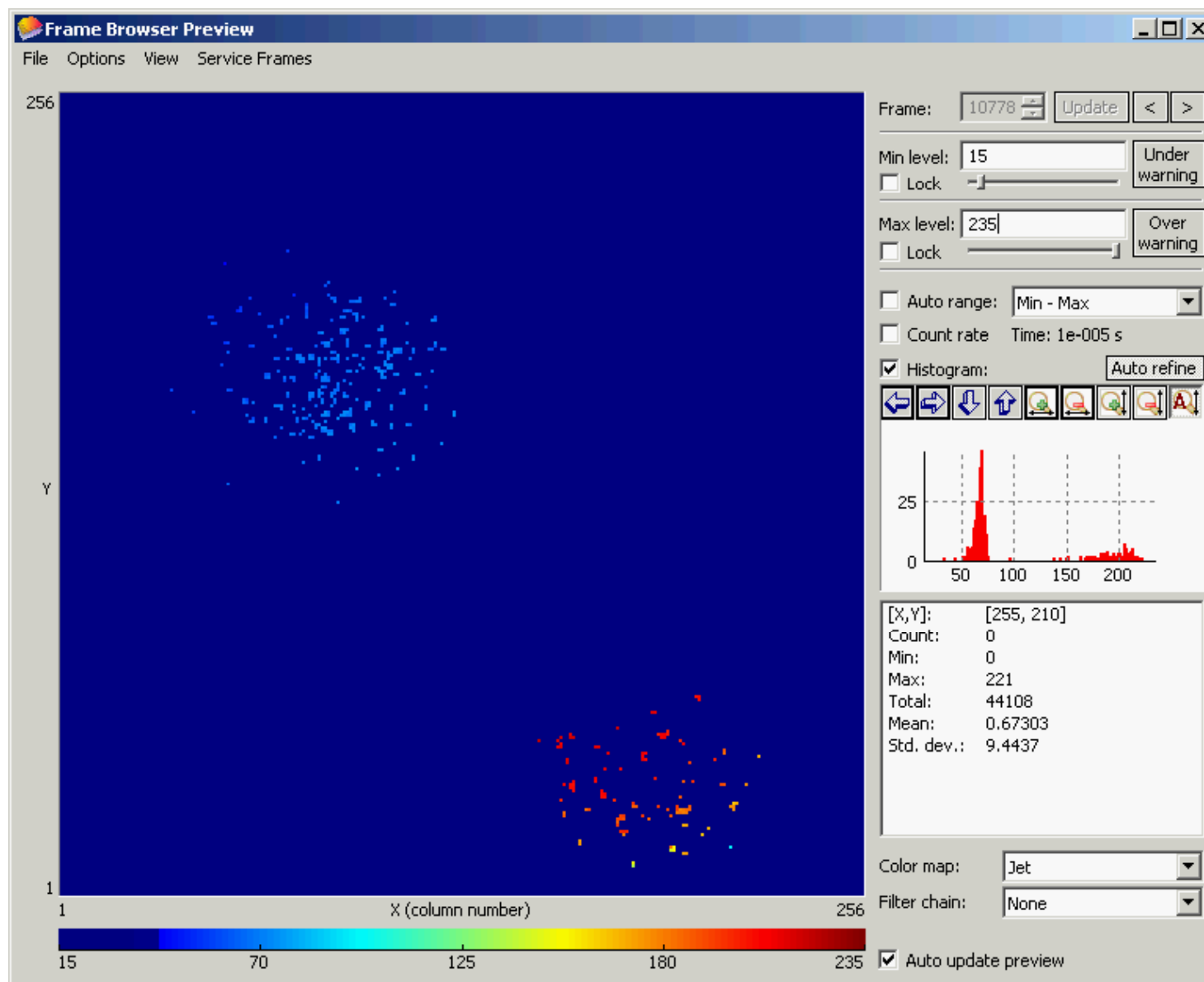
- TimePix chip
+ SiProt 20 μm
+ Micromegas
- ^{55}Fe source
- Ar/Iso (95:5)
- TOT mode
- $z = 60 \text{ mm}$
- $t_{\text{shutter}} = 1 \text{ s}$





Micro-TPC TimePix/Micromegas: Time mode

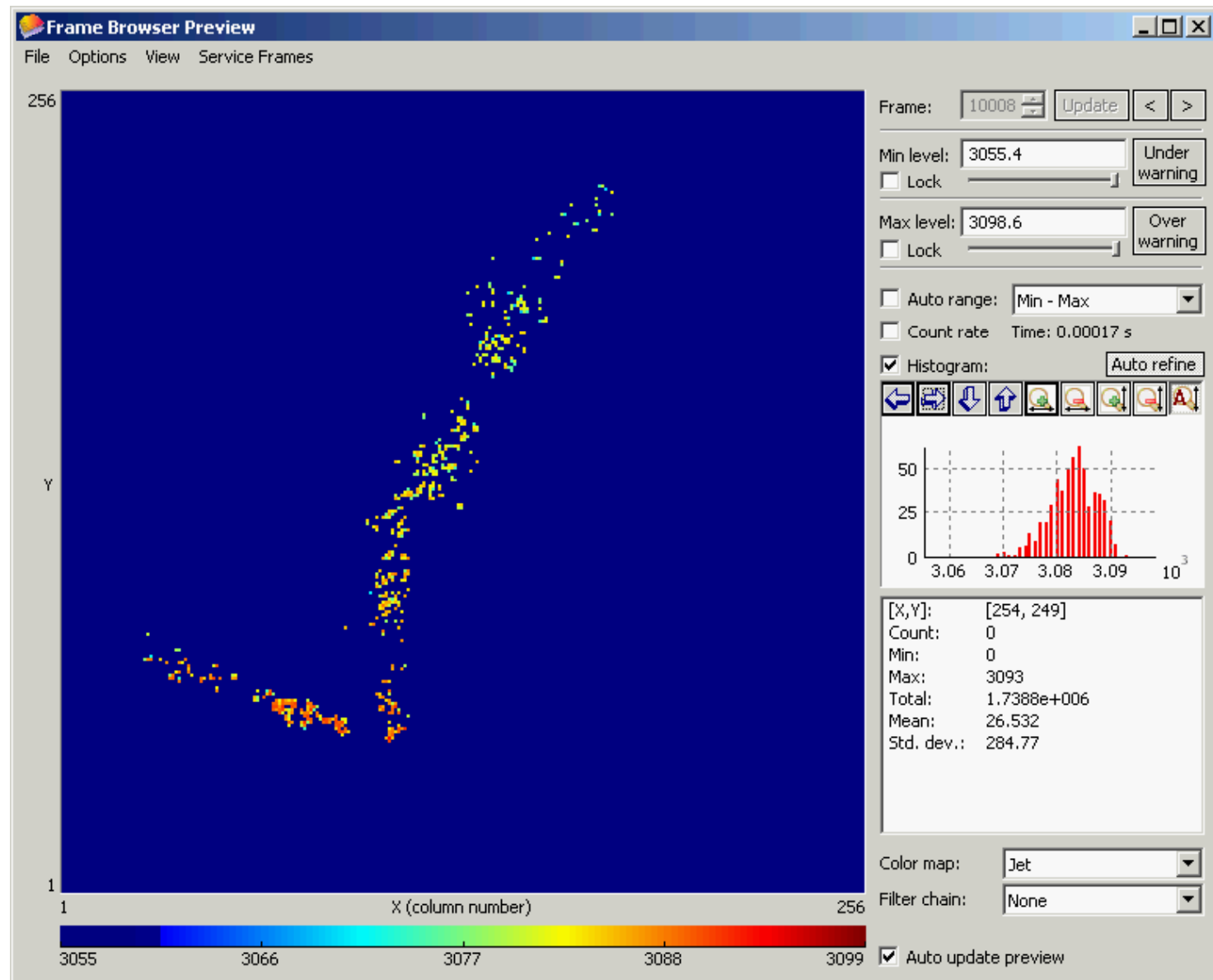
- TimePix chip
+ SiProt 20 μm
+ Micromegas
- ^{55}Fe source
- Ar/Iso (95:5)
- Time mode
- $z = 25$ mm
- $V_{\text{mesh}} = -340$ V
- $t_{\text{shutter}} = 283$ μs





Micro-TPC TimePix/Micromegas: Time mode

- TimePix chip
+ SiProt 20 μm
+ Micromegas
- ^{90}Sr source
- Ar/Iso (95:5)
- Time mode
- $z \sim 40$ mm
- $V_{\text{mesh}} = -340$ V
- $t_{\text{shutter}} = 180$ μs

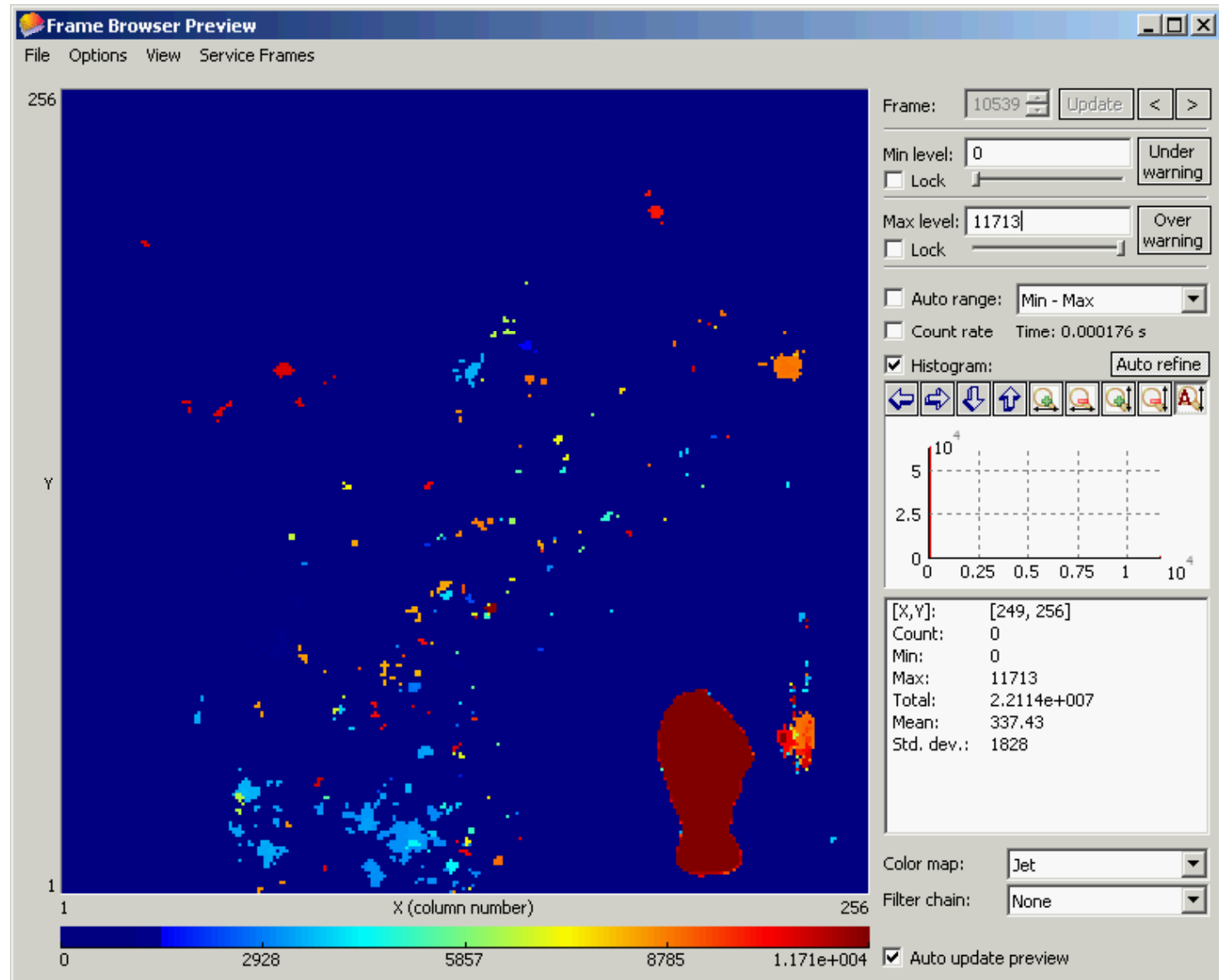




Micro-TPC TimePix/Micromegas

- TimePix chip
+ SiProt 20 μm
+ Micromegas
- ^{90}Sr source
- Ar \rightarrow He
- Time mode
- z \sim 40 mm
- $V_{\text{mesh}} = -340$ V
- $t_{\text{shutter}} = 180$ μs

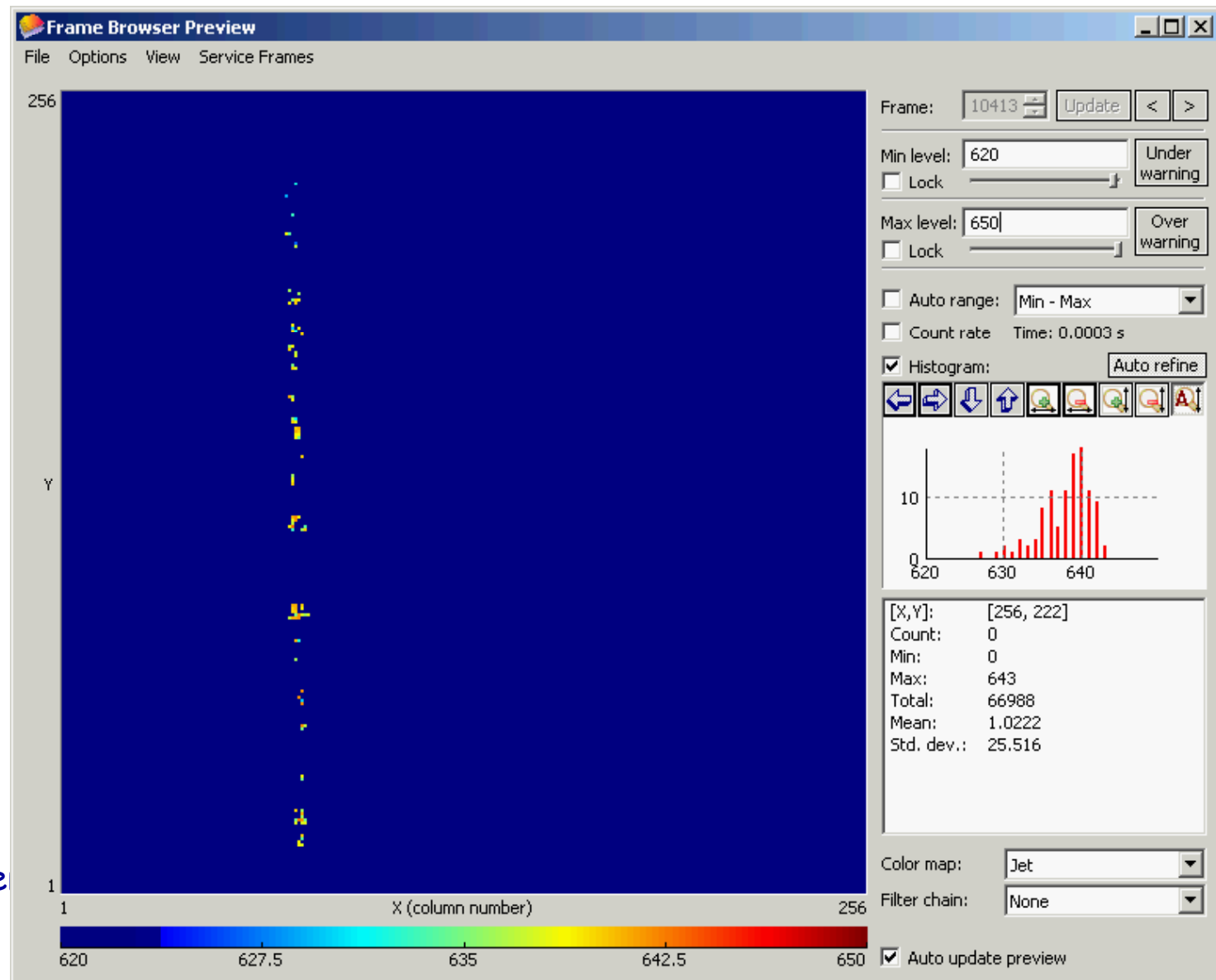
spark-proof !





Micro-TPC TimePix/Micromegas: Time mode

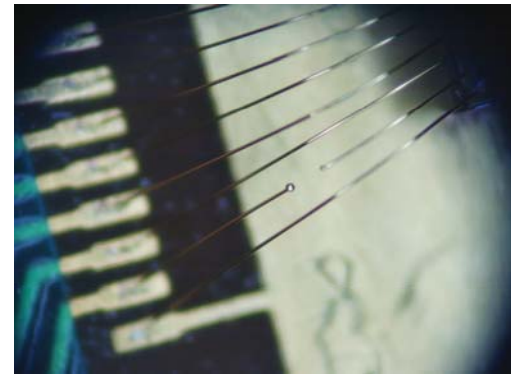
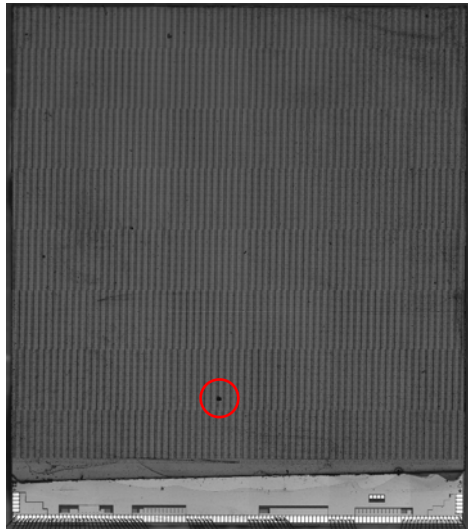
- TimePix chip
+ SiProt 20 μm
+ Micromegas
- Cosmic-rays
- He/Iso (80:20)
- Time mode
- $z \sim 0\text{-}6 \text{ cm}$
- $V_{\text{mesh}} = -450 \text{ V}$
- $t_{\text{shutter}} = 160 \mu\text{s}$
+ external trigger



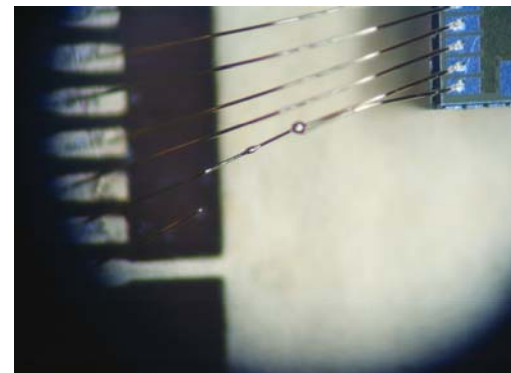


Limitation of the SiProt of 20 μm

- during a night-time run, the detector started to spark continuously
- in the morning it was still alive except for part of the column(s) where the spark was located in a spot (~ 4 pixels)
- a test in the air at 650V provokes a spark \rightarrow bonding wire melted



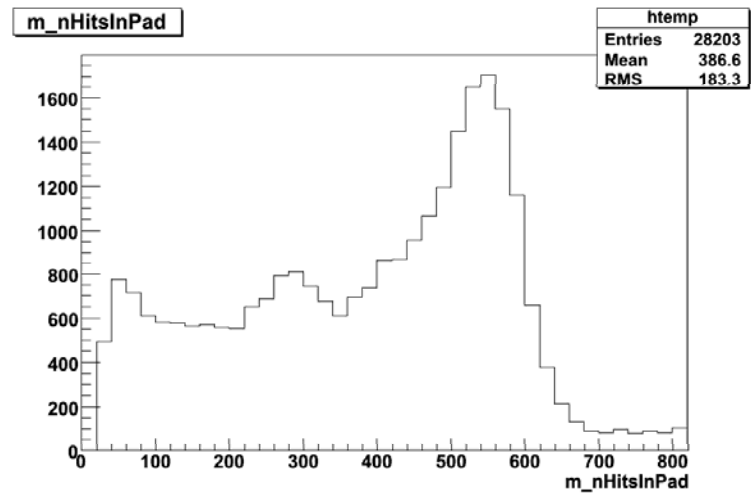
- After a all day of measurement we switched off the chip
- next day the chip was not recognized \rightarrow bonding wire melted



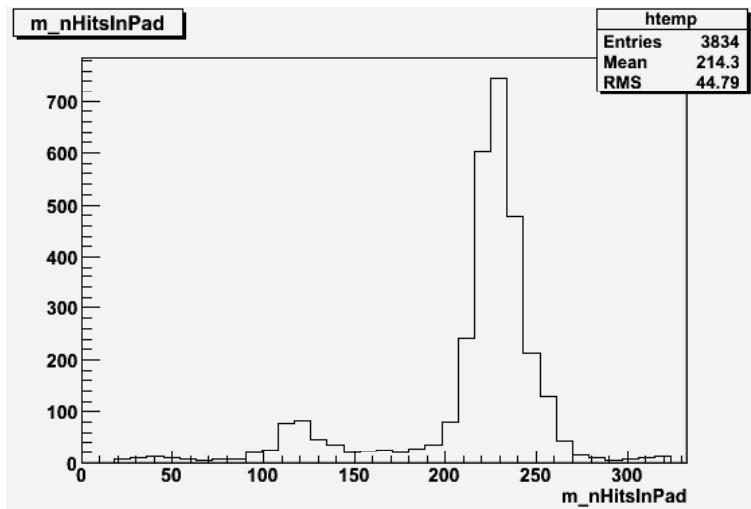


Histogram of all events for ^{55}Fe

- Gas: Argon + 5% Isobutane $\rightarrow \sigma_{\perp}$ big enough to separate electrons



- TimePix + 20 μm SiProt + Micromegas
 - cluster size per electron ~ 2.5
 - 5.9 keV at $\sim 580 e^-$
 - background from incomplete events



- TimePix + 15 μm SiProt + InGrid data from NIKHEF
 - cluster size per electron ~ 1
 - 5.9 keV line at ~ 226

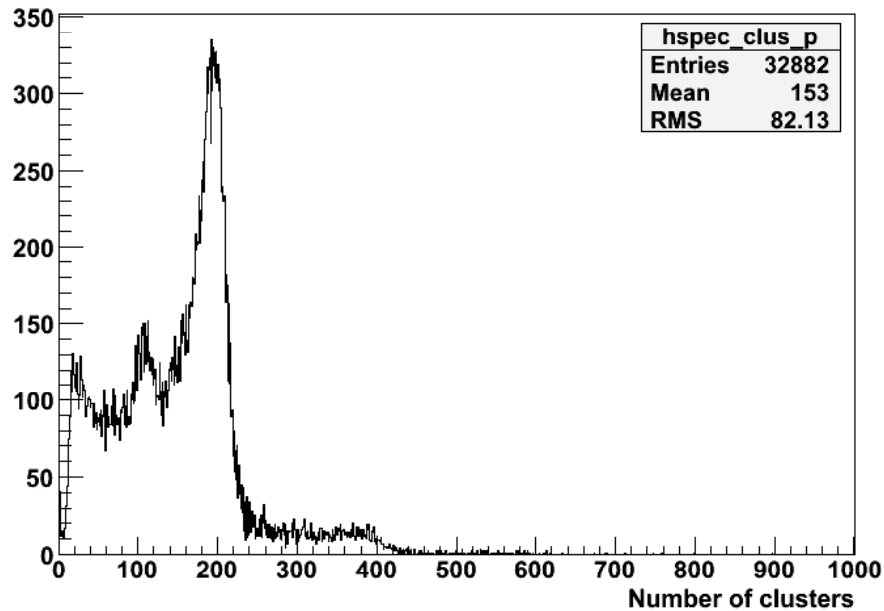


Cluster spectra for ^{55}Fe vs. SiProt

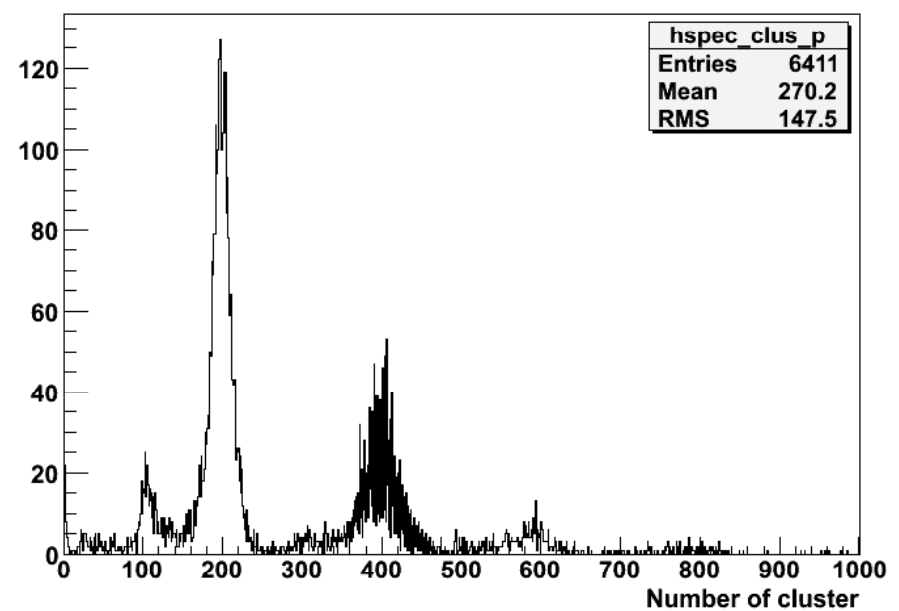
• SiProt 20 μm

• SiProt 15 μm

Spectrum of cluster of electrons



Spectrum of cluster of electrons



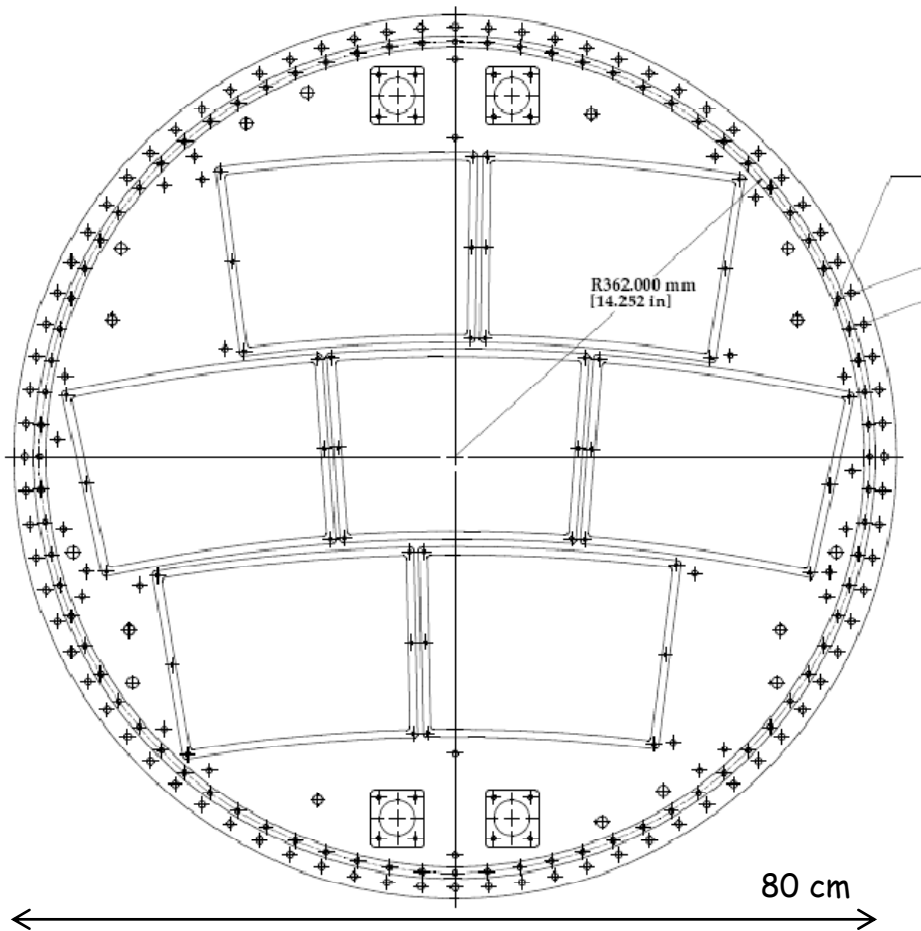


2. Deliverable: TimePix panel for the ILC Large Prototype



Micromegas panels for the ILC Large Prototype

- Endplate designed for 7 panels, $\phi = 80$ cm, arrived at DESY



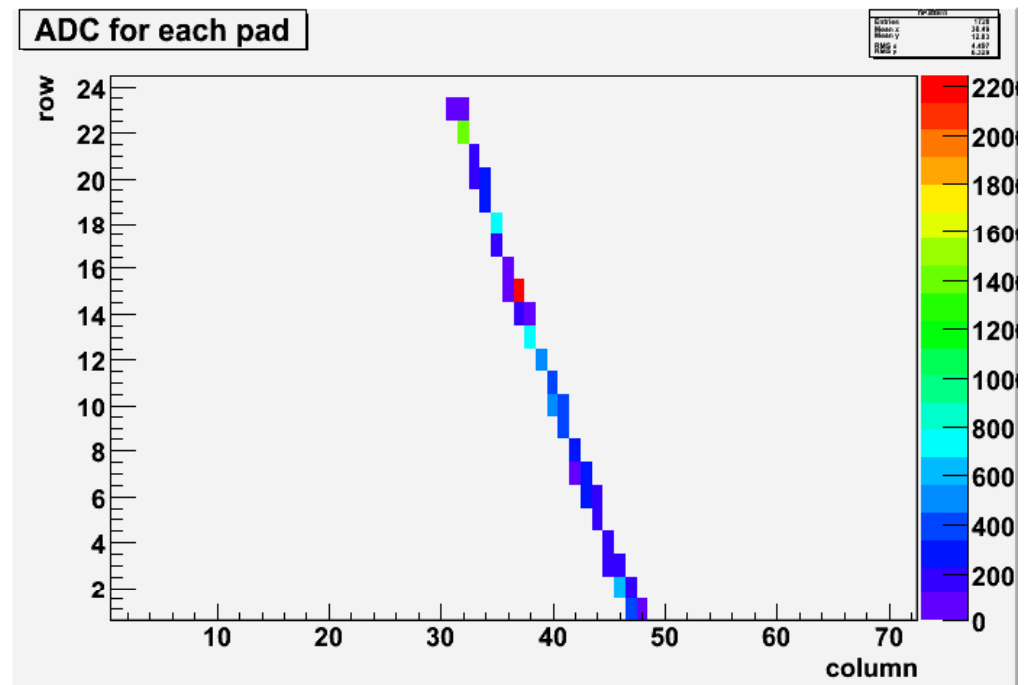


Micromegas panels for the ILC Large Prototype

- First standard Bulk Micromegas panel tested last week using cosmic trigger
- 7 panels using resistive anode planned for 2009
- See talk of Paul Colas



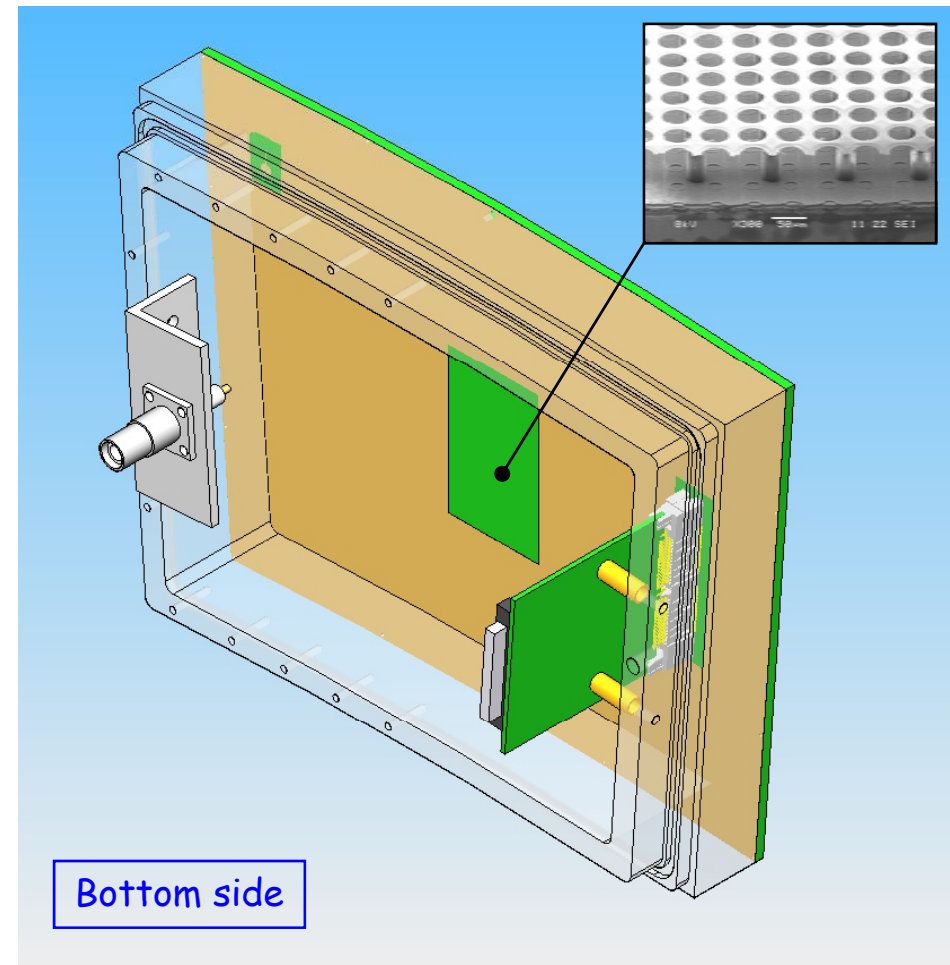
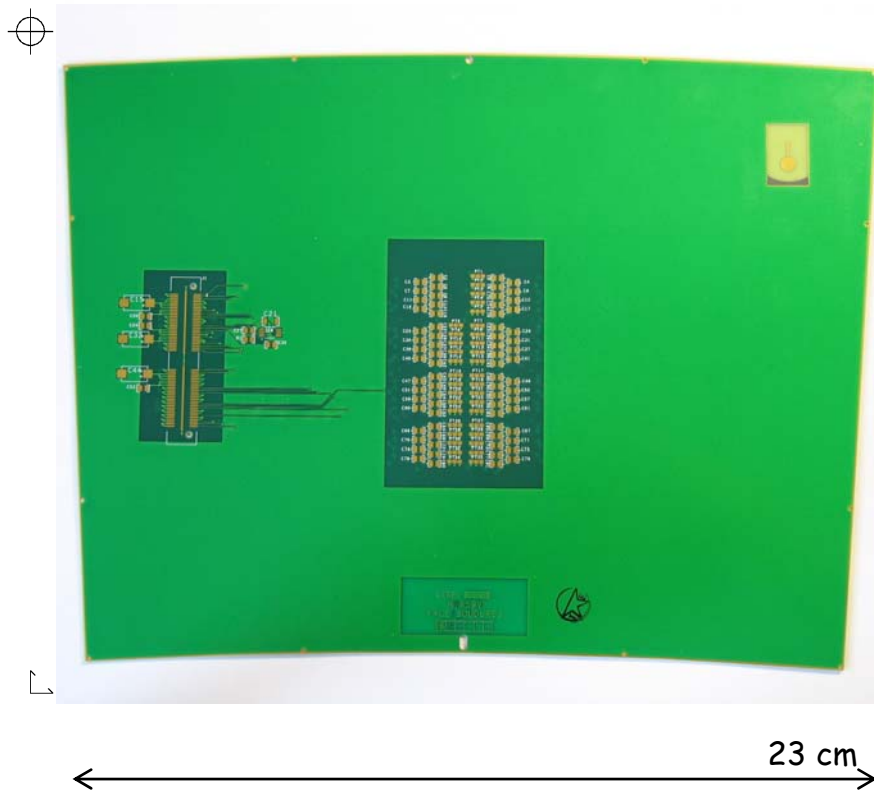
Gas box





TimePix panel for the ILC Large Prototype

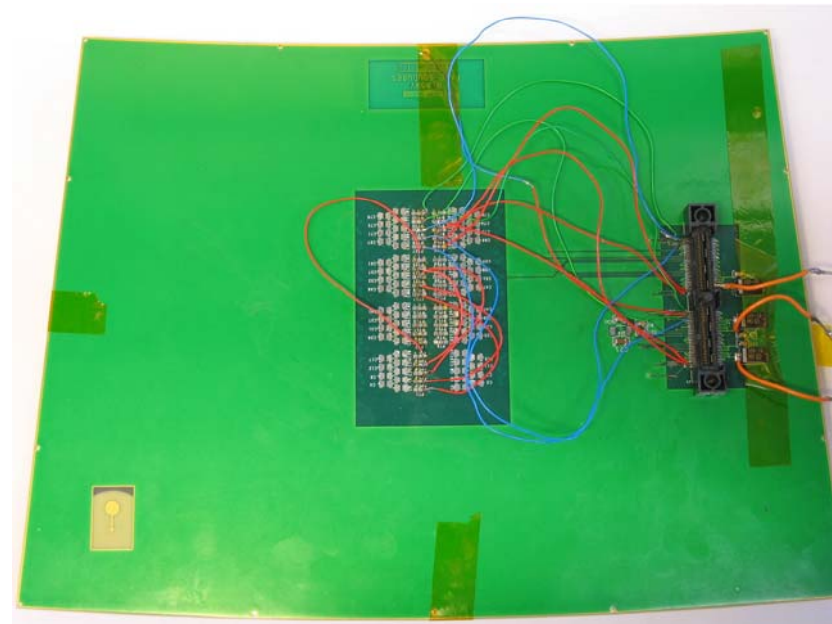
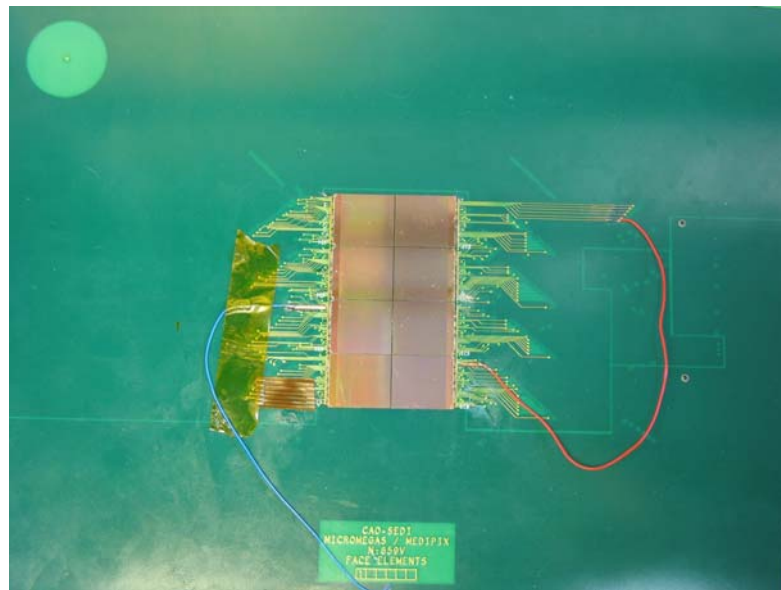
- Panel of a 2x4 TimePix chips matrix where only one bad chip can be bypassed
- Equipped later with InGrids (post-processing Micromegas) and copper plane
- Six-layer PCB → eight-layer
- Transfer card for cable





TimePix panel tests and issues

- 8 chips have been glued and bounded on the panel (connected in serial)
 - panel size larger than the wire bonding machine (600 wires to connect)
 - two chips got scratched by the factory
- Technical support from Xavier Coppolani
 - errors in the routing was found and corrected
 - MUROS + standard connectivity (2 m VHDCI cable) not adapted





- Power consumption of 8 chips is about 1.2 A (supplied in parallel)
 - external power supplies V_{DDA} , V_{DD} & V_{DDLVD5} were provided (~ 2.2 V)
 - currents were monitored and equalized

Next steps

- We will replace the first and the last chips of the matrix
- Validation needed before evolution to a new PCB
 - Mezzanine to facilitate the wire bonding with possibility to do it at Saclay
 - Power regulators on PCB near the chips (1 or 2 to supply 4 chips)
 - Possibility to choose or bypass any chip



Conclusions

- Micro-TPC TimePix chip/Micromegas is a demonstrator for the digital TPC
- Ultimate resolution for a TPC thanks to the single electron sensibility
Micro-TPC is an excellent tool to characterize gas mixture
 - statistics of primary electrons and clusters
- Deliverable panel of 2x4 TimePix + Ingrid is in progress and should be tested with the Large Prototype at DESY in 2009
- Still some technologic issues: how to improve the readout of the chips
 - **Power consumption:** on PCB power regulators?
 - Mezzanine



The TimePix collaboration



• NIKHEF



*Harry van der Graaf
Yevgen Bilevych
Max Chefdeville
Lucie De Nooij
Martin Fransen
Jan Timmermans
Jan Visschers*

• Saclay CEA/DAPNIA



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Paul Colas
Xavier Coppolani
Arnaud Giganon
Yannis Giomataris
Marc Riallot*

• Univ. Twente/Mesa+



*Jurriaan Schmitz
Victor Blanco Carballo
Cora Salm
Sander Smits*

• FREIBURG

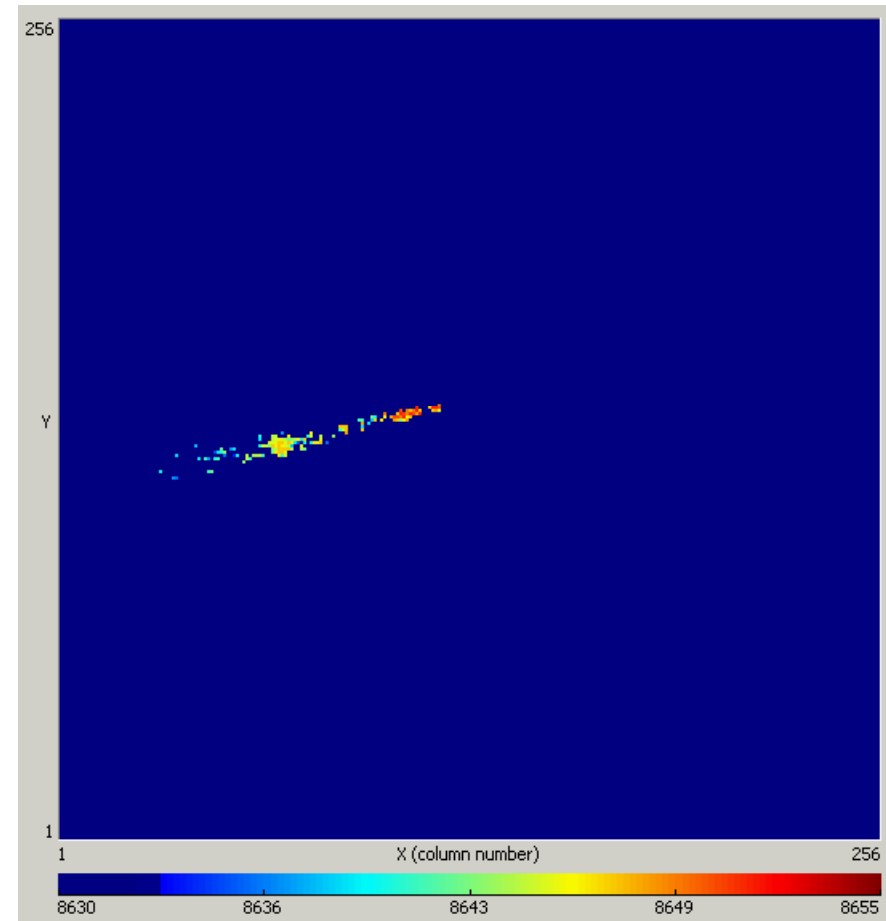


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β^- from ^{90}Sr source in He/Isobutane 80:20

Thank you for your attention