

The pixel telescope DAQ

Daniel Haas/Emlyn Corrin

DPNC Genève

EUDET Annual Meeting 2008

NIKHEF, Amsterdam

Outline

- JRA1 DAQ Hardware
- JRA1 DAQ Software
- Offline Software
- Achievements
- User integration
- The 'final' DAQ
- Roadmap



The JRA1 DAQ scheme (HW)

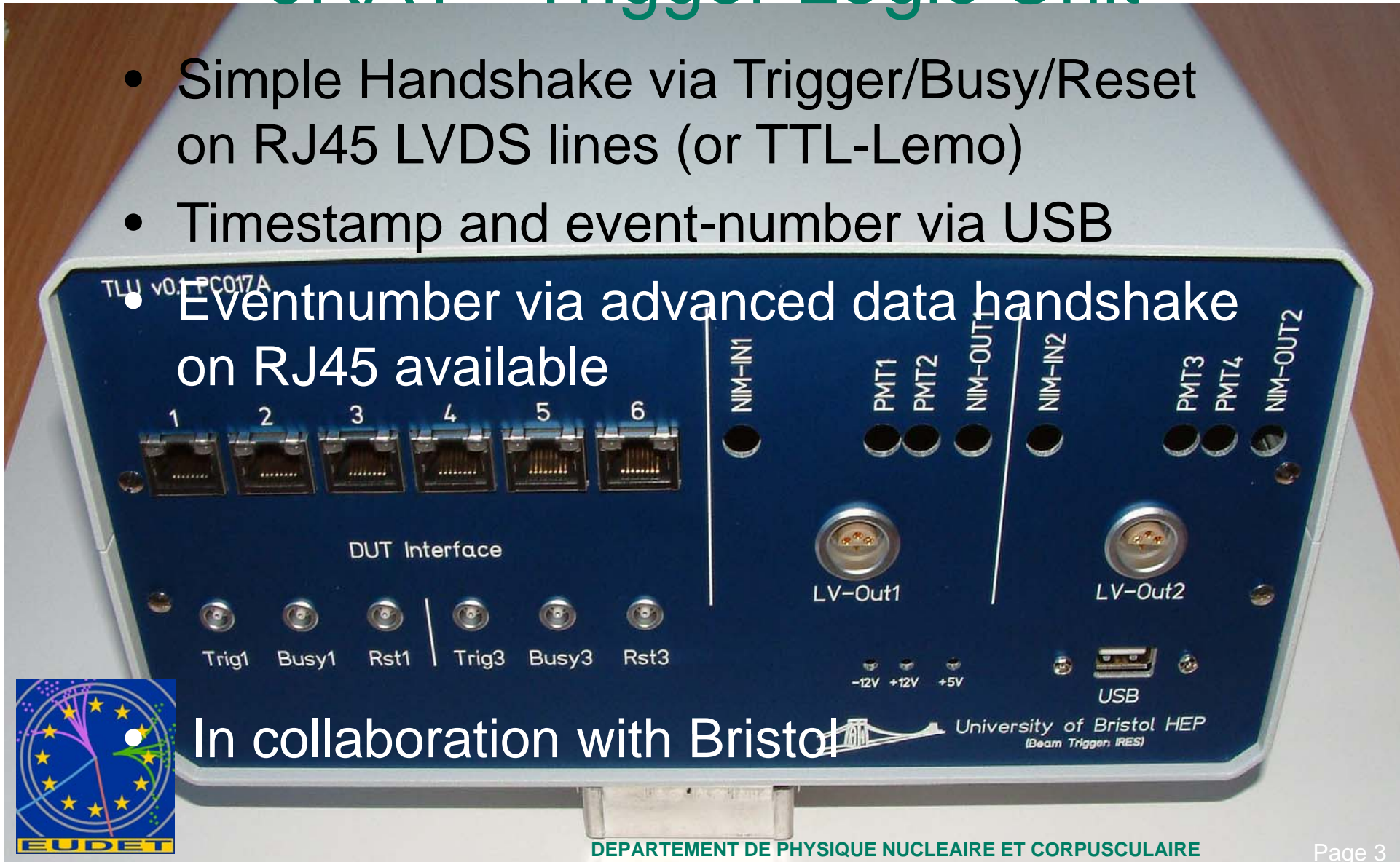
QuickTime™ and a
decompressor
are needed to see this picture.



JRA1 - Trigger Logic Unit

- Simple Handshake via Trigger/Busy/Reset on RJ45 LVDS lines (or TTL-Lemo)
- Timestamp and event-number via USB

• Eventnumber via advanced data handshake on RJ45 available



In collaboration with Bristol University of Bristol HEP (Beam Trigger IRES)

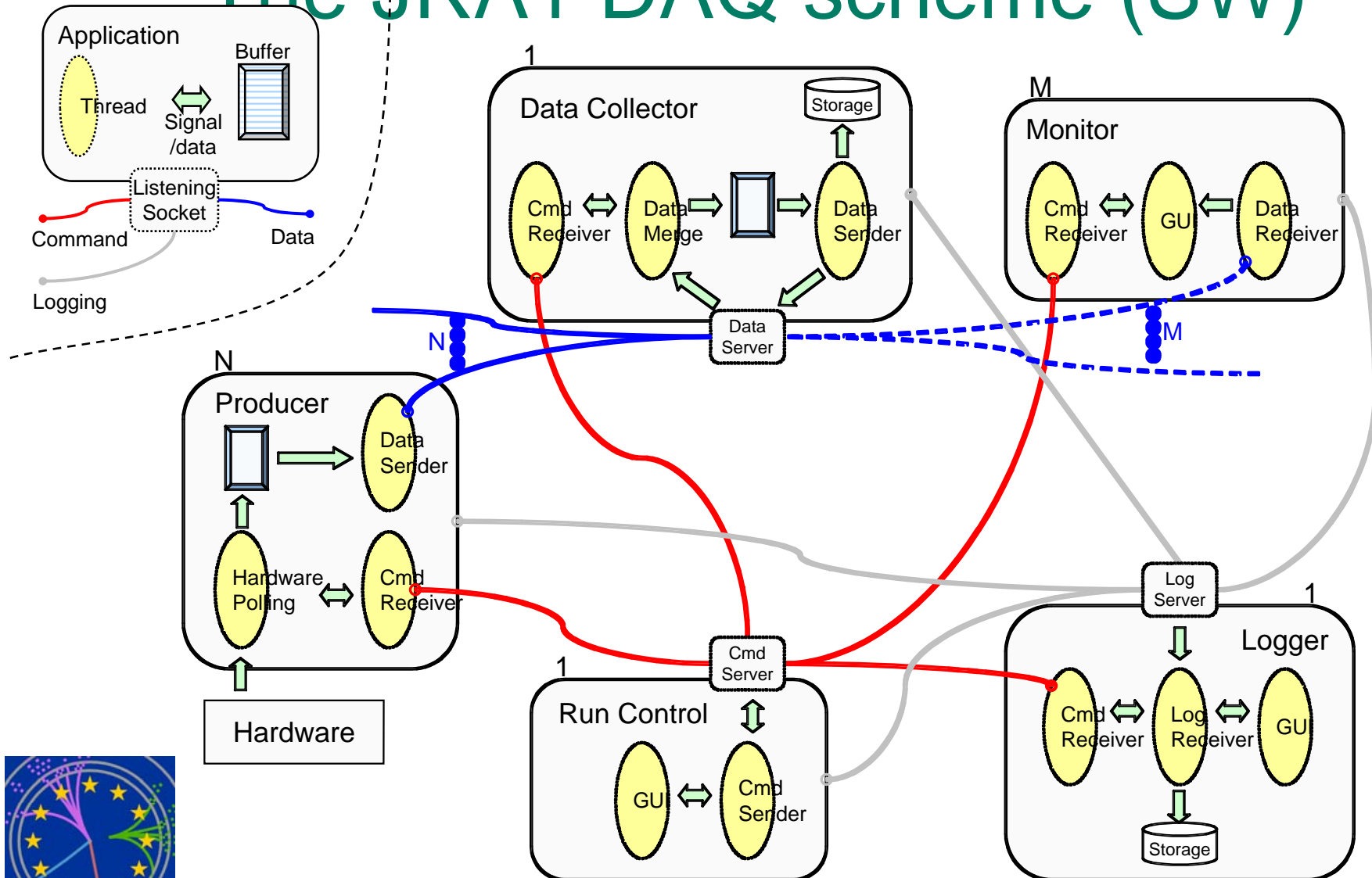


JRA1 - EUDRB

- VME based readout card for our telescope (analog) sensors and to apply zero suppression
- Upgradeable to 'final' digital chip
- Data is bundled on VME CPU and sent to main DAQ



Key: The JRA1 DAQ scheme (SW)



The JRA1 DAQ scheme (SW)

QuickTime™ and a
decompressor
are needed to see this picture.

from P. Roloff



QuickTime™ and a
decompressor
are needed to see this picture.

from P. Roloff



QuickTime™ and a
decompressor
are needed to see this picture.

from P. Roloff



QuickTime™ and a
decompressor
are needed to see this picture.

from P. Roloff



QuickTime™ and a
decompressor
are needed to see this picture.

from P. Roloff



Current Achievements & Goals

- Implemented DAQ Architecture is robust, multi-platform, scalable, simple-to-use and adoptable to different users

see <http://projects.hepforge.org/eudaq>
and <http://www.eudet.org>

- Offline processing fully on the GRID, using 'standard' ILC software
- Lots of documentation now available
- Current Speed achieved:
~600 Hz (2 boards/Mimotel)
in ZS mode
- Goals (for FP6):

- 1 kHz
- more documentation (code)

Goals are (nearly) achieved



User integration

- Creating new Producers for users is harder than it needs to be
- Currently each Producer requires it's own Event data type, but they all do the same thing
- Need to provide a generic RawDataEvent (similar to universal reader)
 - Can store arrays of raw data of variable size
 - Has a tag with the format of the data (EUDRB / DEPFET etc.)



Get ready for final chip

- EUDRB + newly designed digital daughter card (Baseline):
- Current VME driver could transfer data from 6 cards at around 1 kHz
- To achieve more, we need:
 - decoupling of input/output buffer in EUDRB (boards should be ready for the next frame immediately after having finished the current frame)
 - multi-event buffer in the EUDRB and 2e SST



Roadmap

- Next 6-9 months should bring final readout
- We are busy to get ready for this
- If other JRAs want to use our DAQ, they should provide manpower for implementation changes (we are willing to help)
- We should discuss requirements (dedicated meeting with TPC after this meeting)

