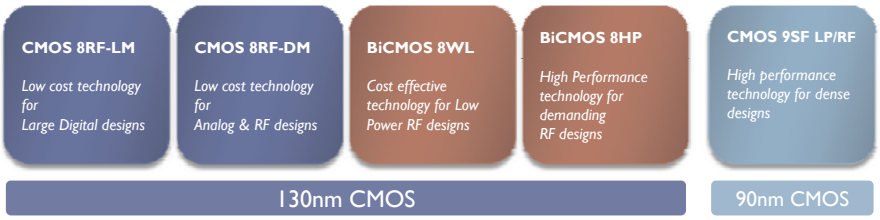
EUDET Report - MICELEC Activities Design Tools Status

Overview of Technologies



- Base and Digital Design Kit installed in 7 labs.
- Future technologies can be negotiated with the same manufacturer, once the necessity arise.

Access to Technology Data

- What you need to start designing.

- Distributed by CERN

Technology	Process	Distributable	
CMOS8RF-LM	130nm	Foundry PDK	Digital Kit
CMOS8RF-DM	130nm	Foundry PDK	
BiCMOS8WL	130nm (SiGe)	Foundry PDK	
BiCMOS8HP	130nm (SiGe)	Foundry PDK	
CMOS9SF	90nm	Foundry PDK	

Foundry PDK : Physical Design Kit for Analog and full custom design.

Digital Kit : Design Kit that supports Digital design.

New Design Kit Functionalities 1/2

Preliminary information

- Design Environment Setup
  - Integrates foundry PDKs, and Physical IP libraries.
  - Initialises the CAE tools design environment (env. variables, files, and directory st to meet the target technology configuration. (ex. BEOL options).
  - No additional coding or scripting necessary.
  - Configuration management per designer and per project.
- Analog & Mixed Signal (AMS) methodology.
  - Top-down design Partitioning.
  - Top-down mixed-Signal Simulation & design Concept Validation
    - Concurrent use of behavioural models, transistor-level schematics and simulation testbenches.
  - Multiple power supply management.
  - Semi-automated Flow for digital implementation
  - Hierarchical design Floorplaning and Physical Assembly
  - Design Performance Validation and Physical Verification

New Design Kit Functionalities 2/2

- Automated Digital Flow
  - RTL-to-GDSII path, for rapid development of larger digital designs.
  - Based on platform independent tcl-code.
  - GUI and command mode interfaces.

Preliminary information

- IP integration workflow
  - Ability to seamlessly integrate IP from multiple sources in the Design Kit.
  - Generates all necessary data structures "views" need by the CAE tools.
- Compatible to "Europractice" CAE tools distribution.
- What CERN could provide to EUDET users:
  - Training courses
  - Maintenance through CERN
  - Technical Support

IP Blocks in 130 nm

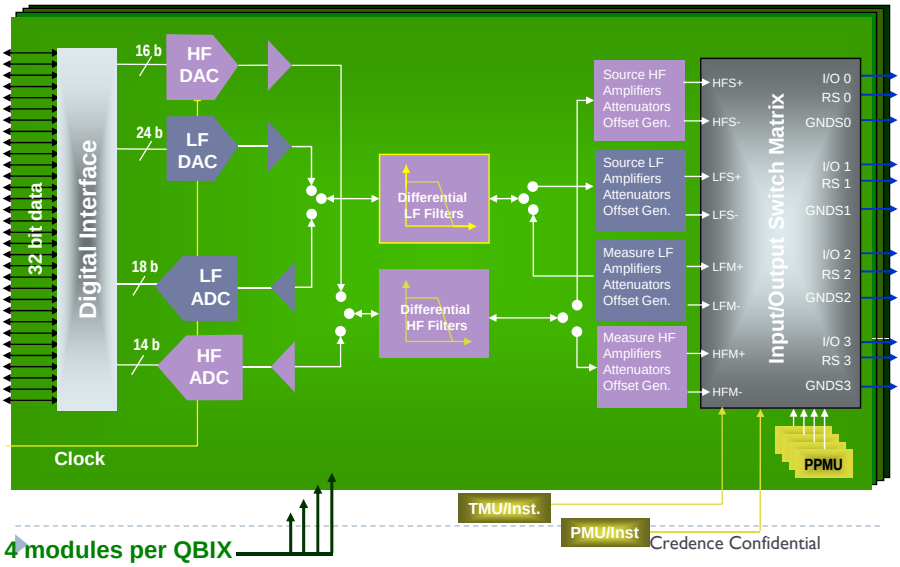
- Several blocks designed exist, some need to be "packaged" in a distributable form
  - LVDS transceivers (Layout)
  - DLL
- Serial links
  - HDLC protocol chip (Verilog)
  - 7/8 bit protocol chip (Verilog)
- Full I2C Slave interface (Verilog & Layout)

IC Tester

- CERN has available an IC tester which could be used by designers in the community for professional characterization of ASICs
  - Specifications:
    - 192 channels @ 200 MHz (or ½ at 2 x spee
    - Analog capabilities (see next slides)
    - DUT Power Supplies up to 6 Amp
- Training courses can be (and have been) organized

IC tester photo

QBIX Analog Module – Block diagram



QBIX Addresses Major Applications