IN2P3

Omega

LAL LAL IPN Orsay

EUDET FEE status

C. de LA TAILLE

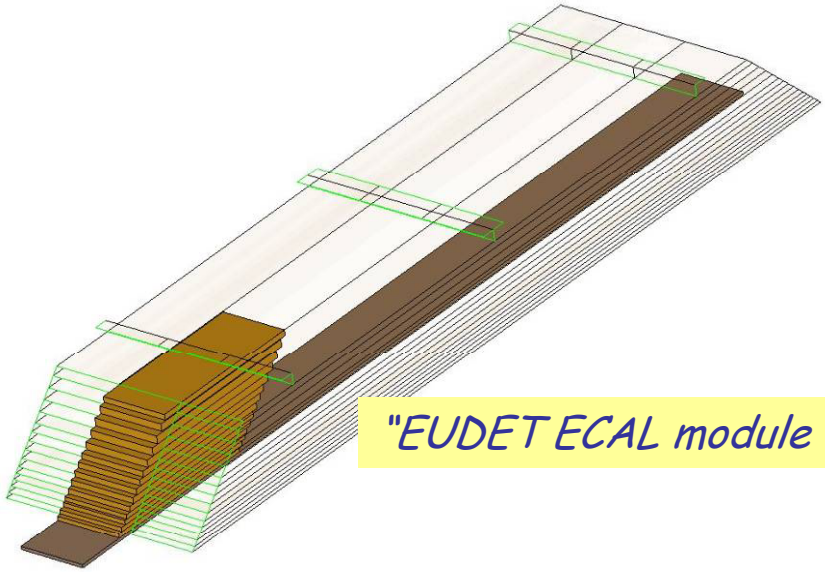
CALICE Calorimeter for ILC

EUDET

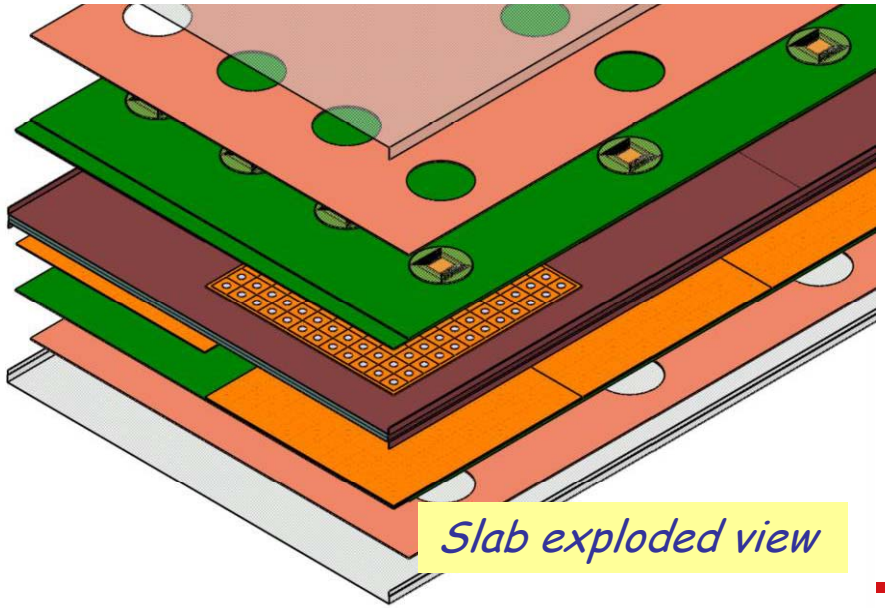
Orsay MicroElectronic Group Associated

EUDET module FEE : main issues

- 2nd generation ASICs
  - Self triggering
  - Digitization & on-chip processing
  - Multi-chip serial readout
  - Power pulsing
- "stictchable" motherboards
  - Minimize connections between boards
- No (few) external components
  - Reduce PCB thickness to <800µm
  - Digital activity with sensistive analog front-end
- Pulsed power issues
  - Electronics stability
  - To be tested in beam
- Interface to new DAQ
- Low cost and industrialization are the major goal



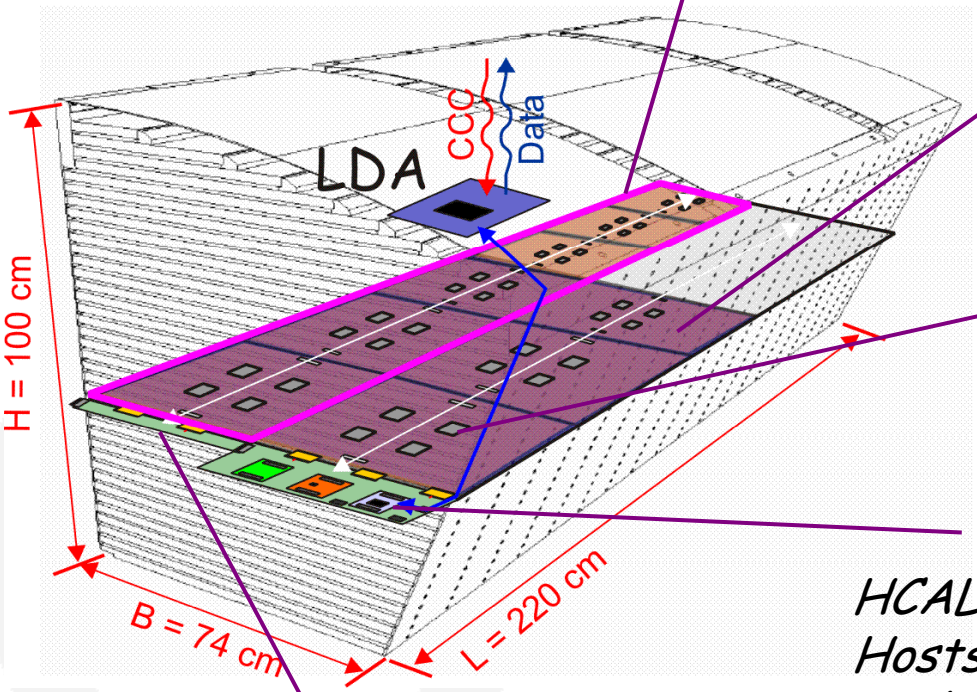
"EUDET ECAL module



Slab exploded view

Barrel HCAL architecture

1/16 of barrel half



AHCAL Slab
6 HBUs in a row

Front end ASICs embedded
Interfaces accessible

HBU
HCAL Base Unit
12 x 12 tiles

SPIROC
4 on a HBU

HEB
HCAL Endcap Board
Hosts mezzanine modules:
DIF, **CALIB** and **POWER**

HLD
HCAL Layer Distributor

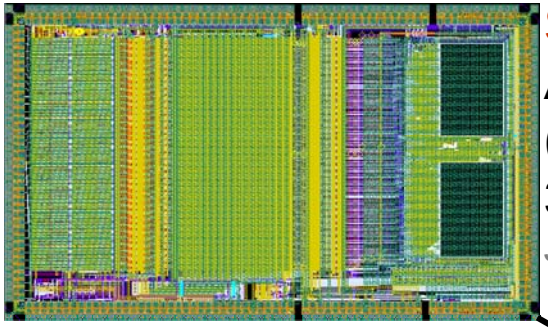
Power:
40 µW / channel

Heat:
T grad. 0.3K/2m
Time constant: 6 d

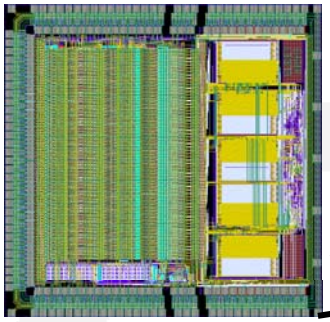
P.Goettlicher (DESY)

The front-end ASICs : the ROC chips

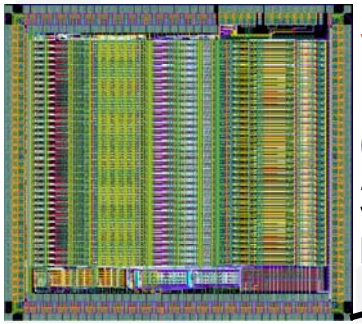
- Technological prototypes : full scale modules (~2m)
- ECAL, AHCAL, DHCAL



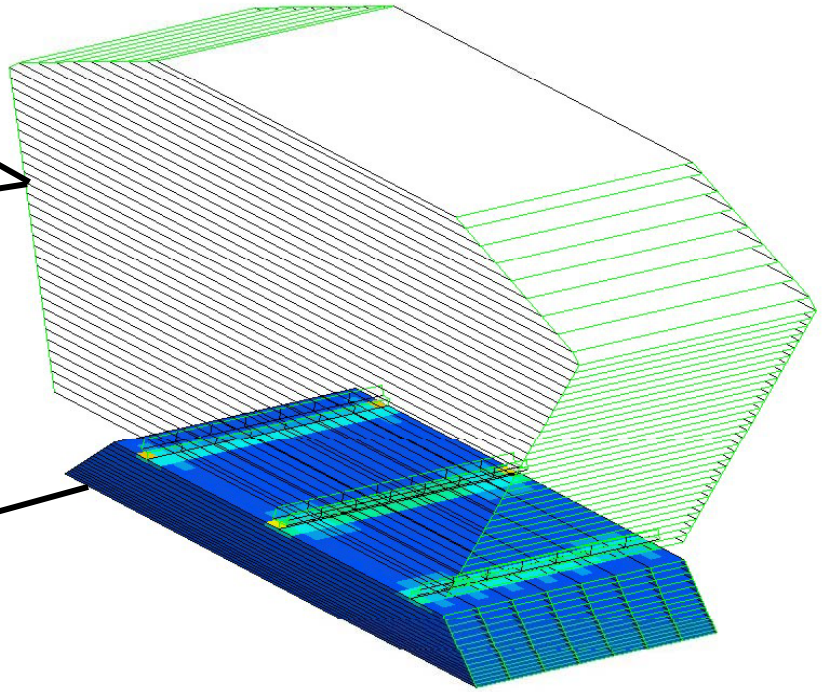
SPIROC
Analog HCAL
(SiPM)
36 ch. 32mm²
June 07



HARDROC
Digital HCAL
(RPC, µmegas or GEMs)
64 ch. 16mm²
Sept 06

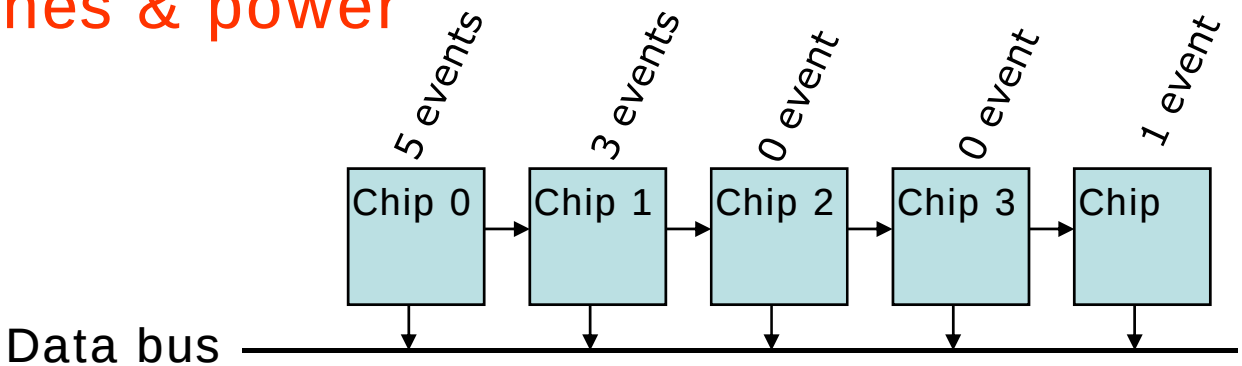


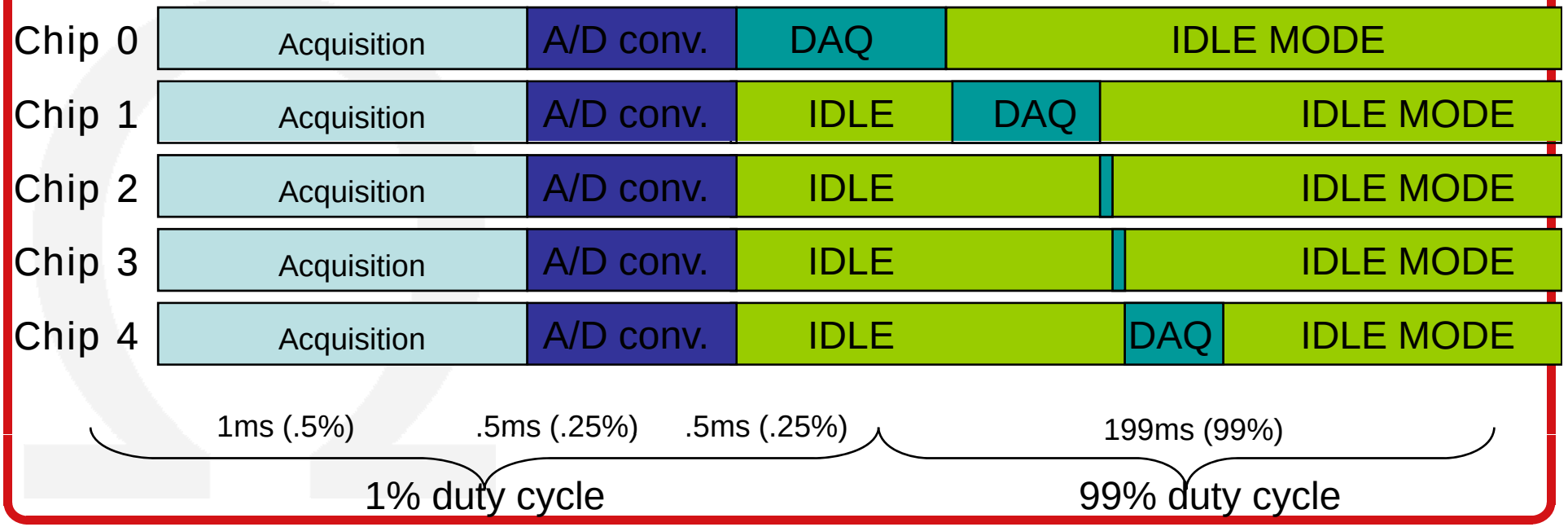
SKIROC
ECAL
(Si PIN diode)
36 ch. 20mm²
Nov 06



Read out : token ring

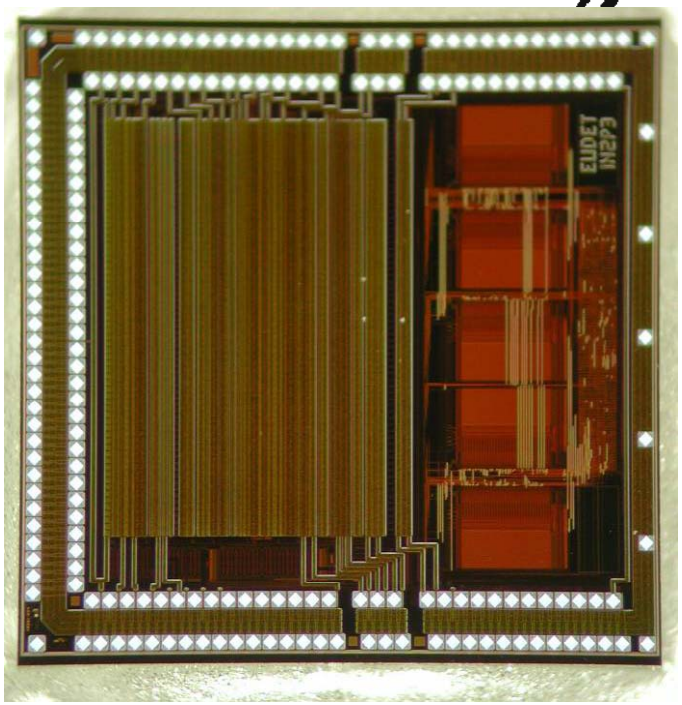
- Readout architecture common to all calorimeters
- Minimize data lines & power



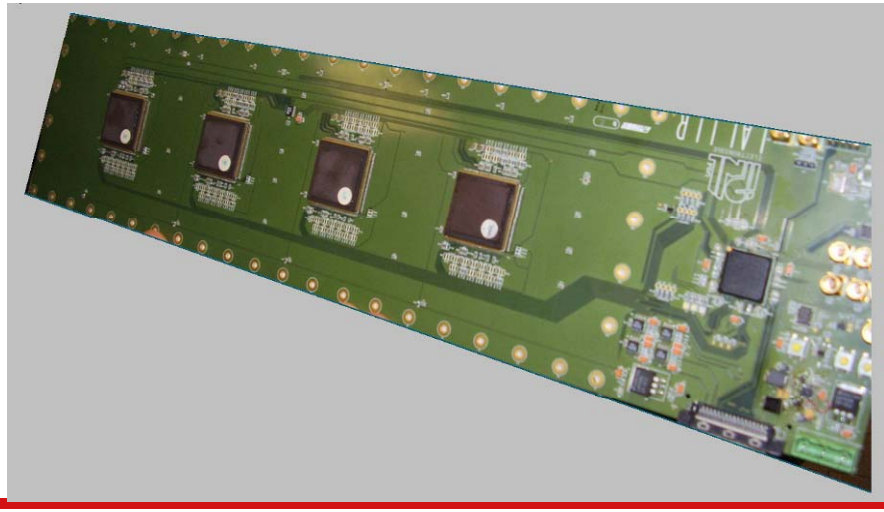


DHCAL chip : HaRDROC

- Hadronic Rpc Detector Read Out Chip (Sept 06)
  - 64 inputs, preamp + shaper+ 2 discris + memory + Full power pulsing
  - Compatible with 1st and 2nd generation DAQ : token ring readout of up to 100 chips
  - 1st test of 2nd generation DAQ and detector integration

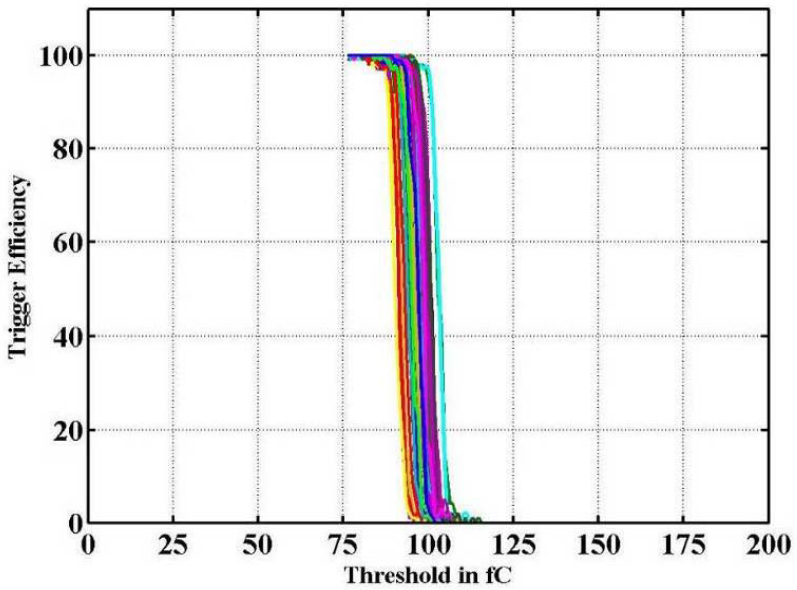


- Collaboration with IPNL/LLR/Madrid/Protvino/
  - 1m³ scalable detector
  - Production of 5000 chips in 2009

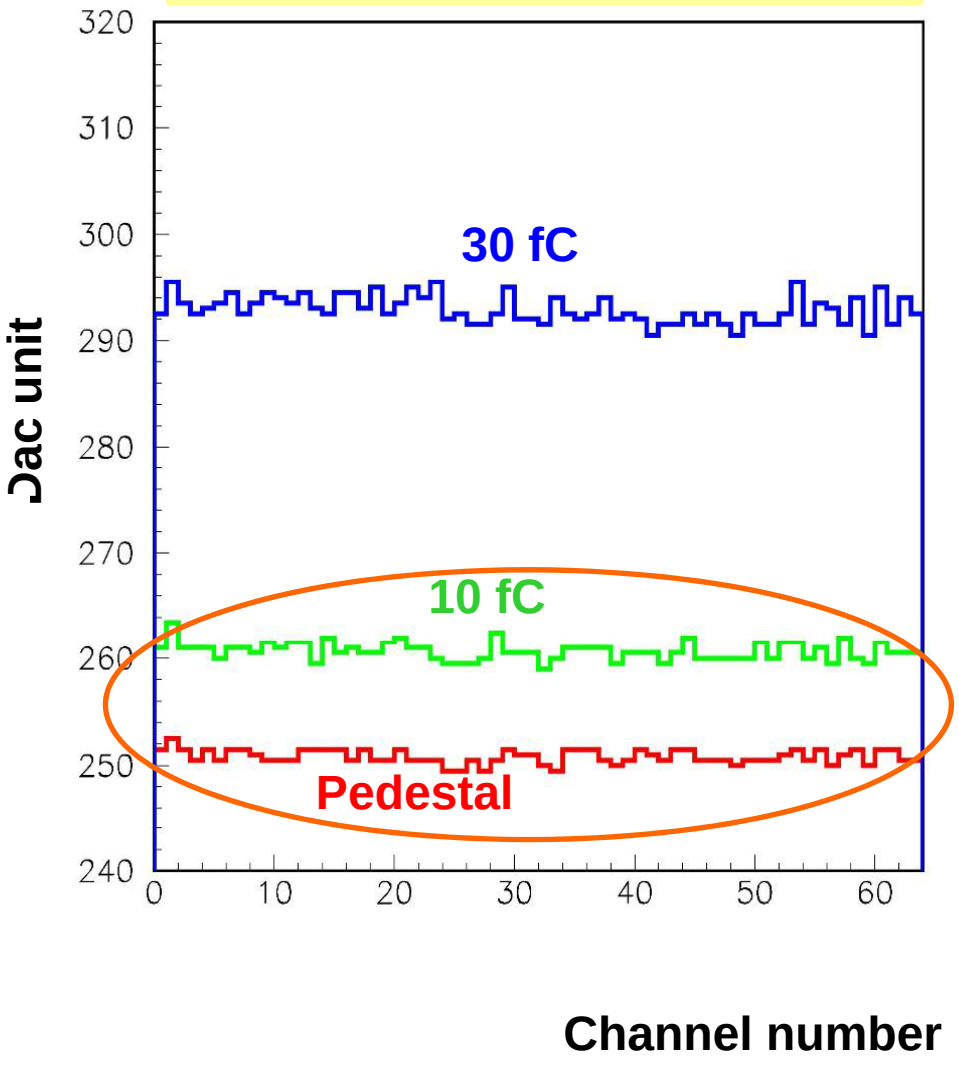


S-curves of 64 channels

- 10 bit DAC for threshold,
- Noise ~ 1 UDAC (2mV)
- Pedestal dispersion : 0.4 UDAC rms
- Gain dispersion 3% rms
- Crosstalk : < 2%

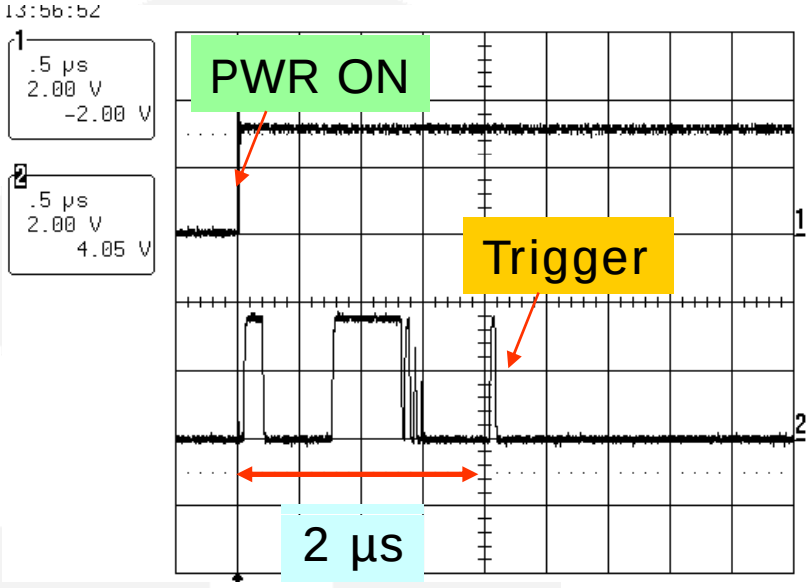


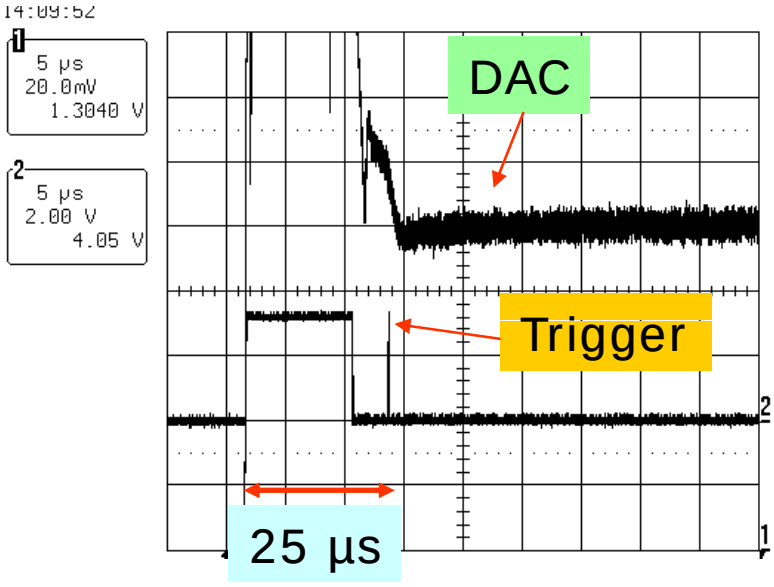
50% trigger versus channel number

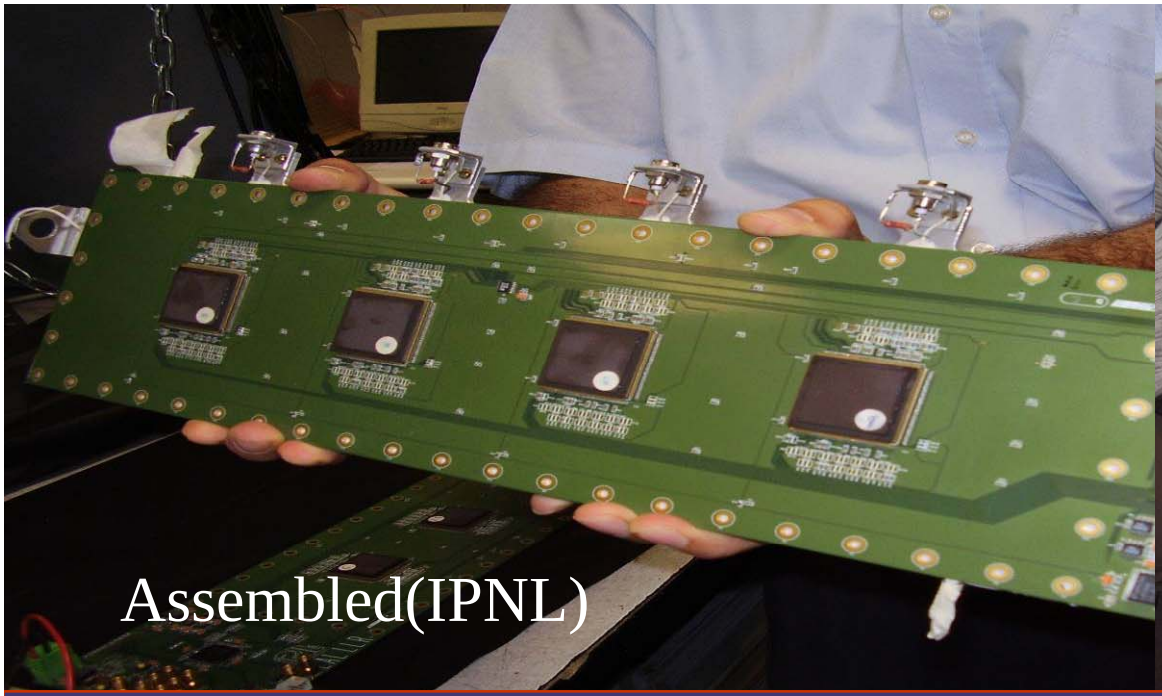


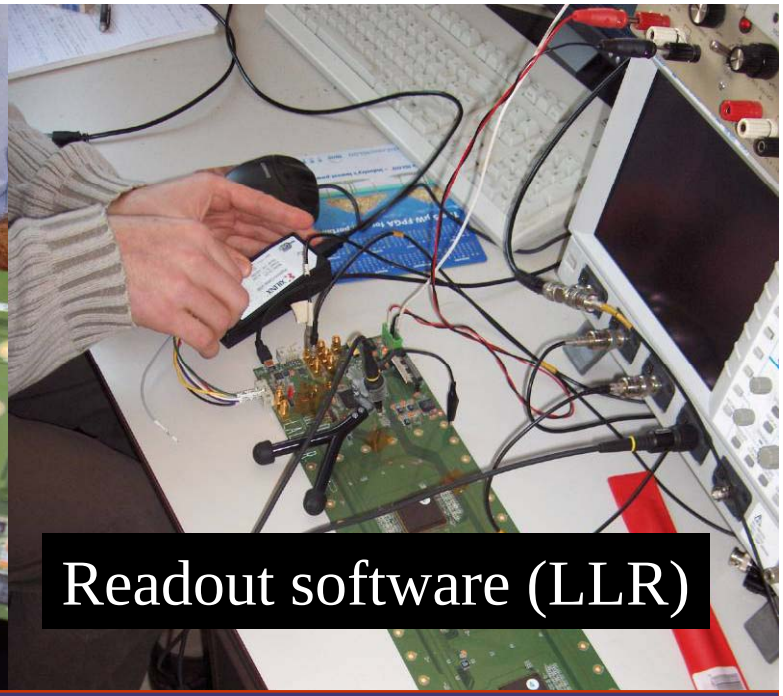
Power pulsing : « Awake » time

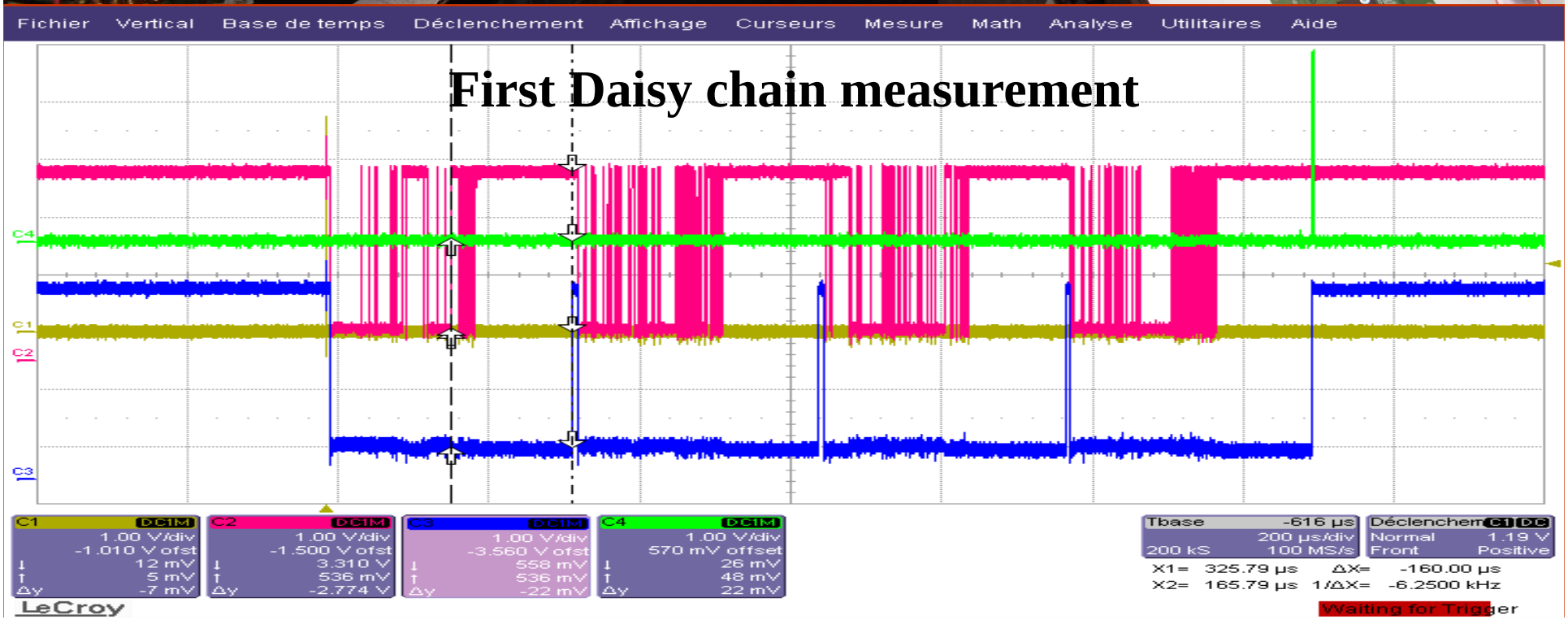
- PWR ON: ILC like (1ms,199ms)
- All decoupling capacitors removed : difficult compromise between noise filtering and fast awake time
- Awake time :
  - Anaog part = 2 us
  - DAC part = 25 us
- 0.5 % duty cycle achieved, now to be tested at system level






Assembled(IPNL)


Readout software (LLR)


Fichier Vertical Base de temps Déclenchement Affichage Curseurs Mesure Math Analyse Utilitaires Aide
First Daisy chain measurement
C4
C1
C2
C3
C1 DC1M 1.00 V/div -1.010 V ofst 12 mV 5 mV Δy -7 mV
C2 DC1M 1.00 V/div -1.500 V ofst 3.310 V 536 mV Δy -2.774 V
C3 DC1M 1.00 V/div -3.560 V ofst 558 mV 536 mV Δy -22 mV
C4 DC1M 1.00 V/div 570 mV offset 26 mV 48 mV Δy 22 mV
Tbase -616 µs 200 µs/div 200 kS 100 MS/s
Déclenchem C1 DC Normal 1.19 V Front Positive
X1= 325.79 µs ΔX= -160.00 µs
X2= 165.79 µs 1/ΔX= -6.2500 kHz
LeCroy
Waiting for Trigger

Beam test [I. Laktineh CALOR 08]

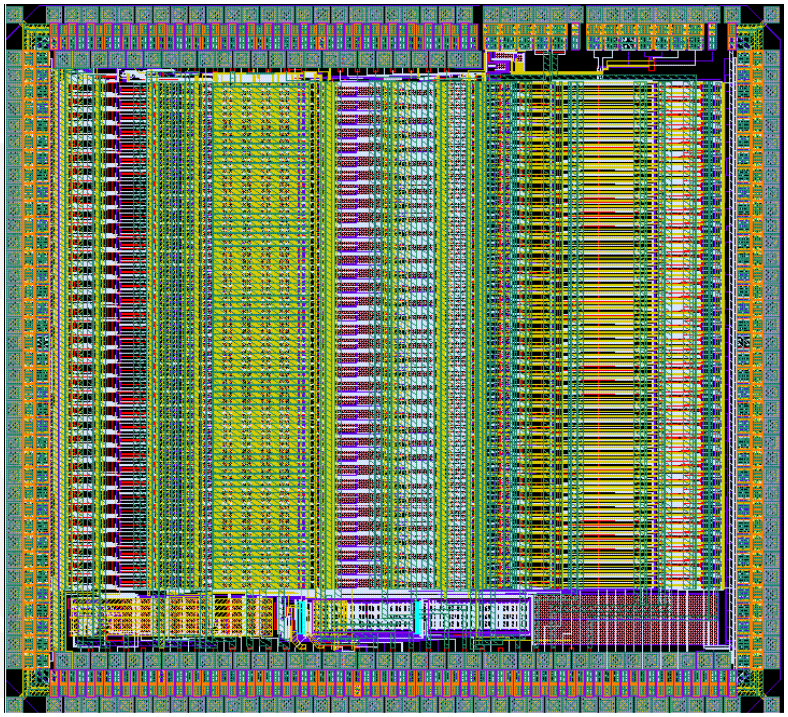
Final confirmation of the success of our electronic readout system will be coming soon with the beam tests with 5 fully equipped detectors (32×8 pads each):

10-17 July :
beam test@ps-cern
3-11 August :
beam test@sps-cern

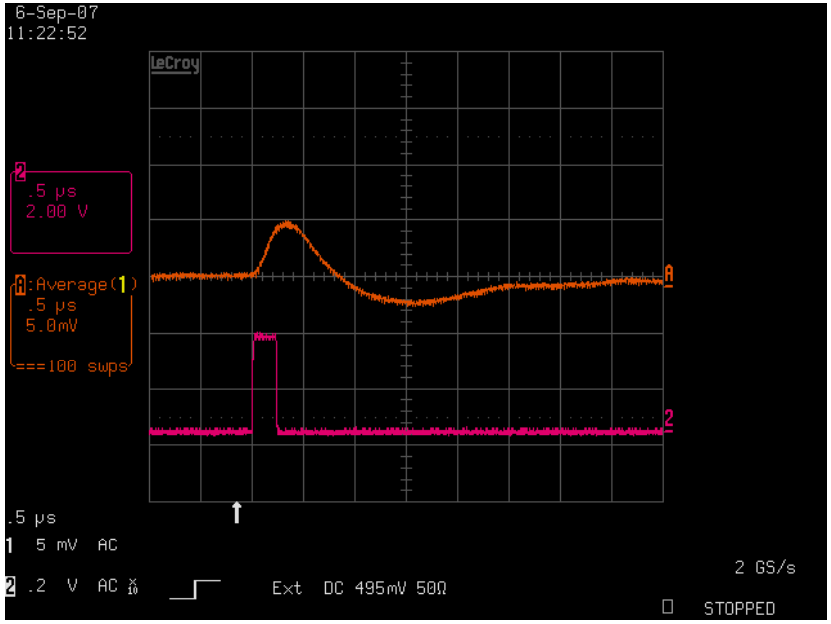
To study:
* Efficiency and multiplicity
vs:angle, position, particle multiplicity
* but also the first phase of the Hadronic shower

SKIROC for W-Si ECAL

- Silicon Kalorimeter Integrated Read Out Chip (Nov 06)
  - 36 channels with 15 bits Preamp + bi-gain shaper + autotrigger + analog memory + Wilkinson ADC
  - Digital part outside in a FPGA for lack of time and increased flexibility
  - Technology SiGe 0.35µm AMS. Chip received may 07

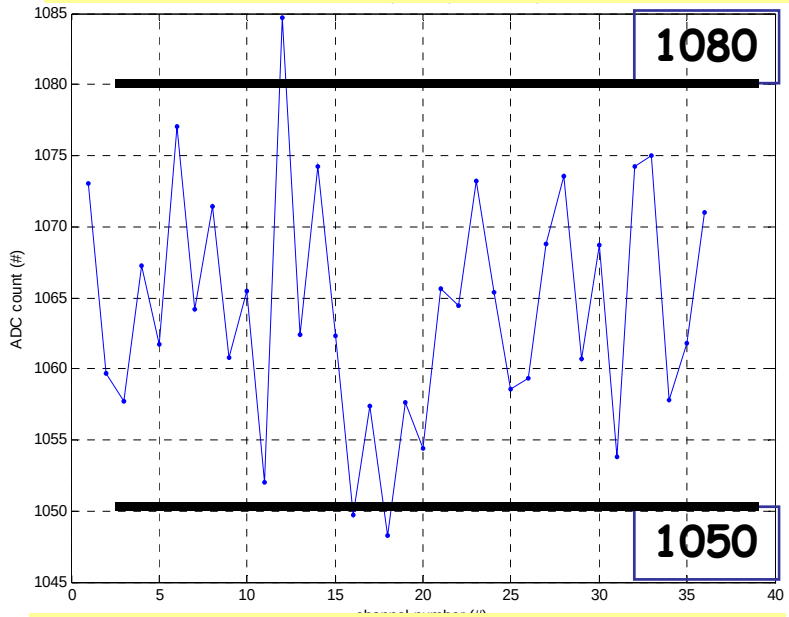


1 MIP in SKIROC

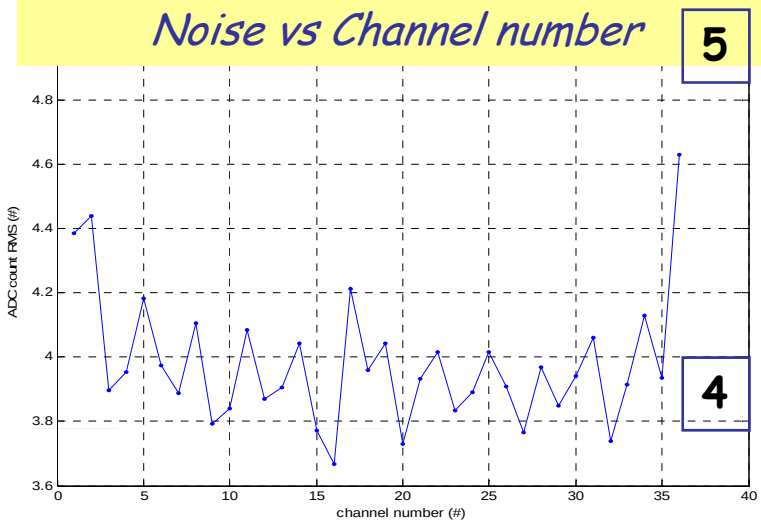


12 bit Wilkinson ADC performance

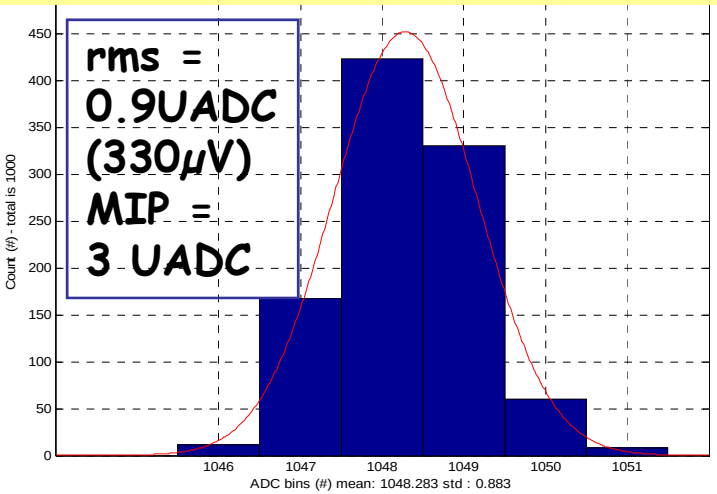
Pedestal value vs Channel number



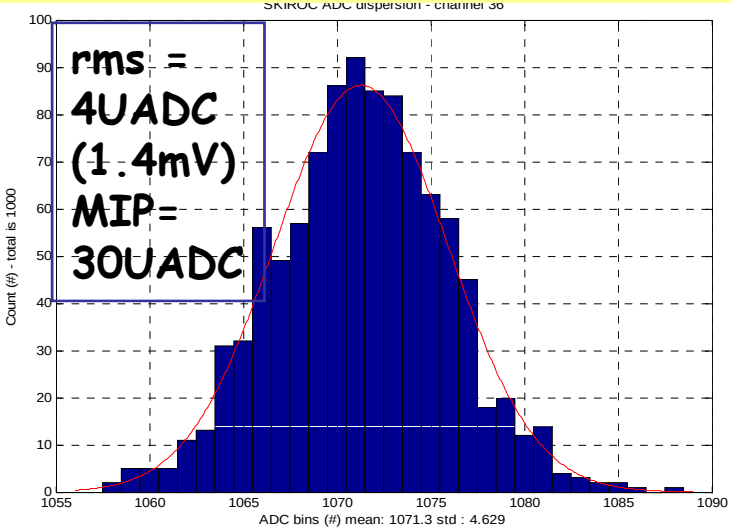
Noise vs Channel number



Noise in low gain shaper

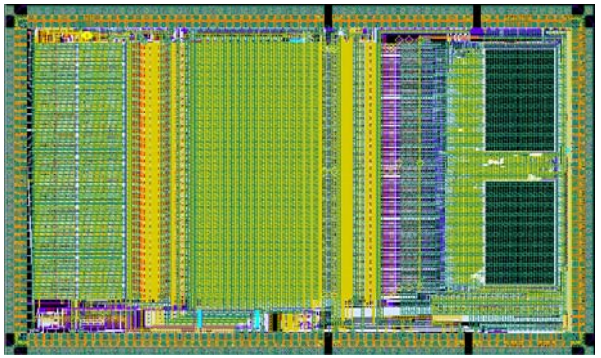


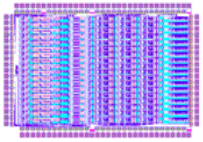
Noise in high gain shaper



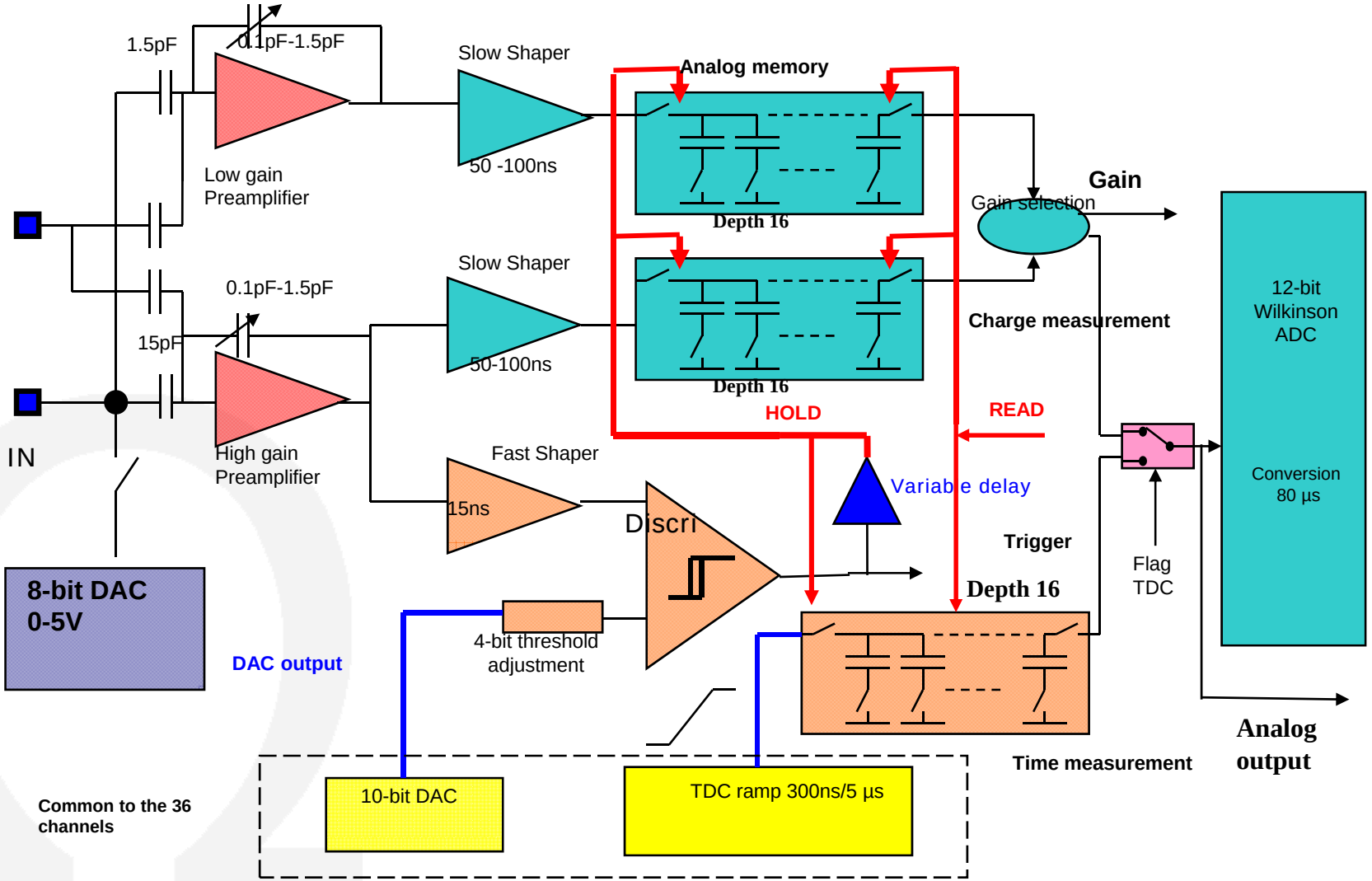
SPIROC main features

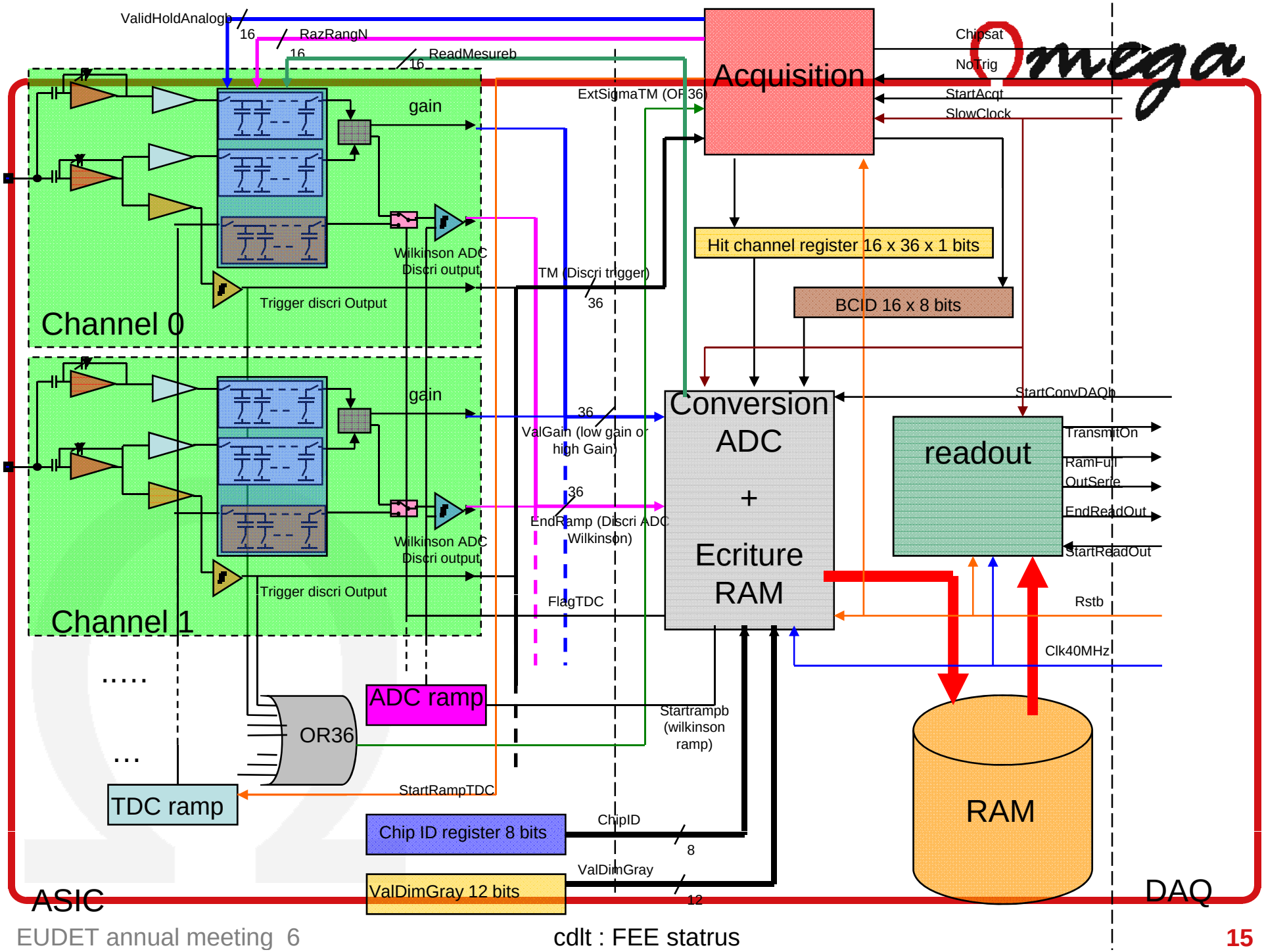
- Internal input 8-bit DAC (0-5V) for individual SiPM gain adjustment
- Energy measurement : 14 bits
  - 2 gains (1-10) + 12 bit ADC 1 pe → 2000 pe
  - Variable shaping time from 50ns to 100ns
  - pe/noise ratio : 11
- Auto-trigger on 1/3 pe (50fC)
  - pe/noise ratio on trigger channel : 24
  - Fast shaper : ~10ns
  - Auto-Trigger on ½ pe
- Time measurement :
  - 12-bit Bunch Crossing ID
  - 12 bit TDC step~100 ps
- Analog memory for time and charge measurement : depth = 16
- Low consumption : ~25µW per channel (in power pulsing mode)
- Individually addressable calibration injection capacitance
- Embedded bandgap for voltage references
- Embedded 10 bit DAC for trigger threshold and gain selection
- Multiplexed analog output for physics prototype DAQ
- 4k internal memory and Daisy chain readout





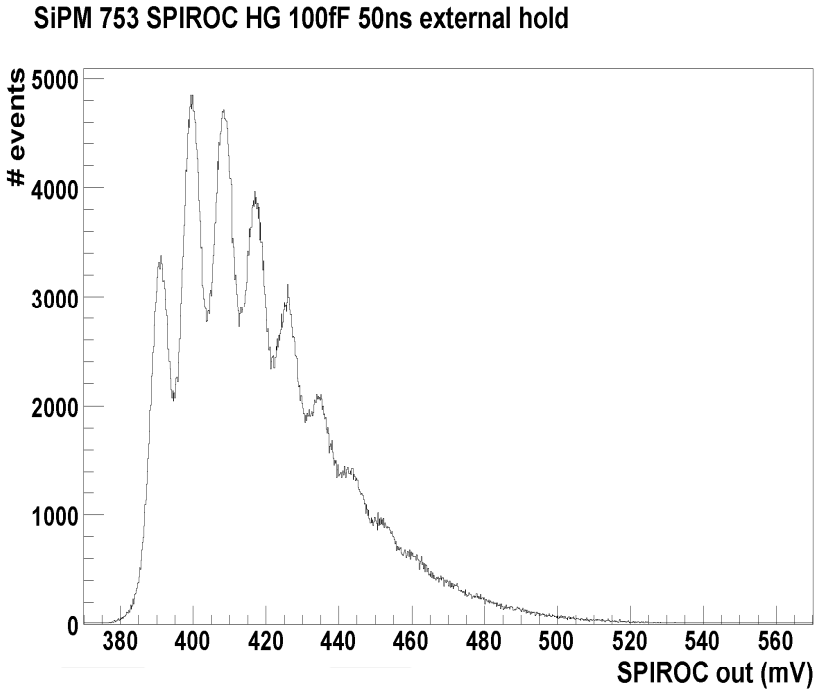
SPIROC : one channel

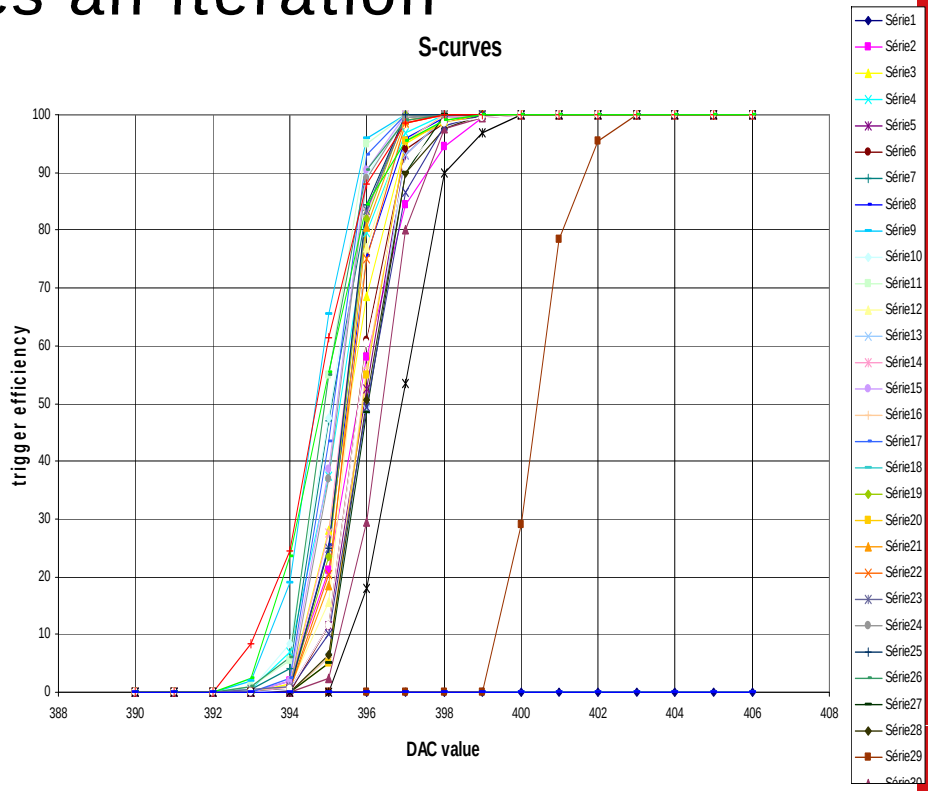



ValidHoldAnalogb
16
RazRangN
16
ReadMesureb
16
Acquisition
Omega
ChipSat
NoTrig
StartAcqt
SlowClock
ExtSigmaTM (OR 36)
gain
Wilkinson ADC
Discri output
Trigger discri Output
Channel 0
TM (Discri trigger)
36
Hit channel register 16 x 36 x 1 bits
BCID 16 x 8 bits
gain
Wilkinson ADC
Discri output
Trigger discri Output
Channel 1
36
ValGain (low gain or high Gain)
36
EndRamp (Discri ADC Wilkinson)
FlagTDC
Conversion ADC + Ecriture RAM
StartConvDAQb
readout
TransmitOn
RamFull
OutSerie
EndReadOut
StartReadOut
Rstb
Clk40MHz
.....
...
OR36
ADC ramp
Startrampb (wilkinson ramp)
TDC ramp
StartRampTDC
Chip ID register 8 bits
ChipID
8
ValDimGray
ValDimGray 12 bits
12
RAM
ASIC
DAQ

SPIROC1 performance

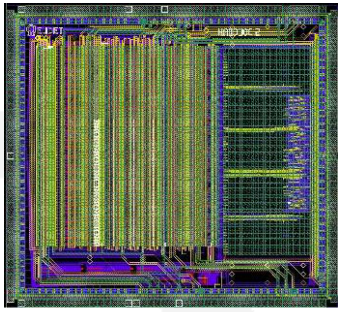
- Good analog performance
  - Single photo-electron/noise = 8
  - Auto-trigger with good uniformity
  - Complex chip : many more measurements needed
- bug in the ADC necessitates an iteration

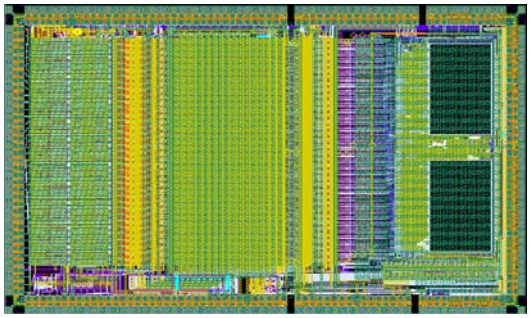




Activities in 2008 (1)

- 2 chips submissions
  - HaRDROC2 (june 08) final chip before production
  - SPIROC2 (june 08) : fixed ADC and slow control bug
  - Can emulate SKIROC and be used for ECAL
  - Fulfils EUDET milestone (M36) on ECAL and AHCAL FE ASIC

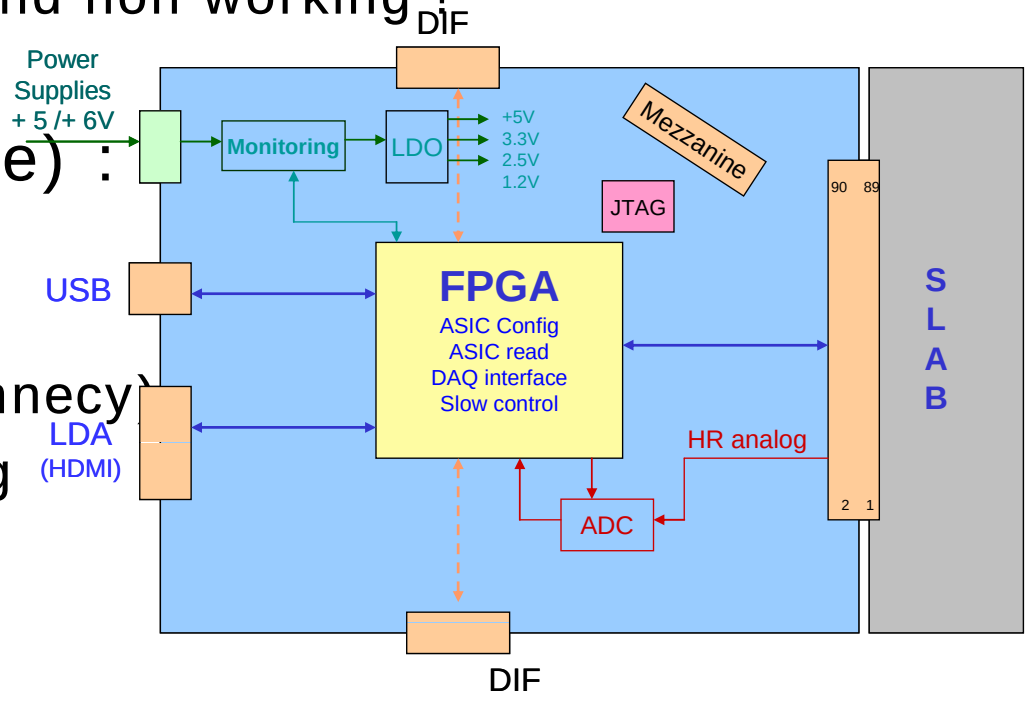




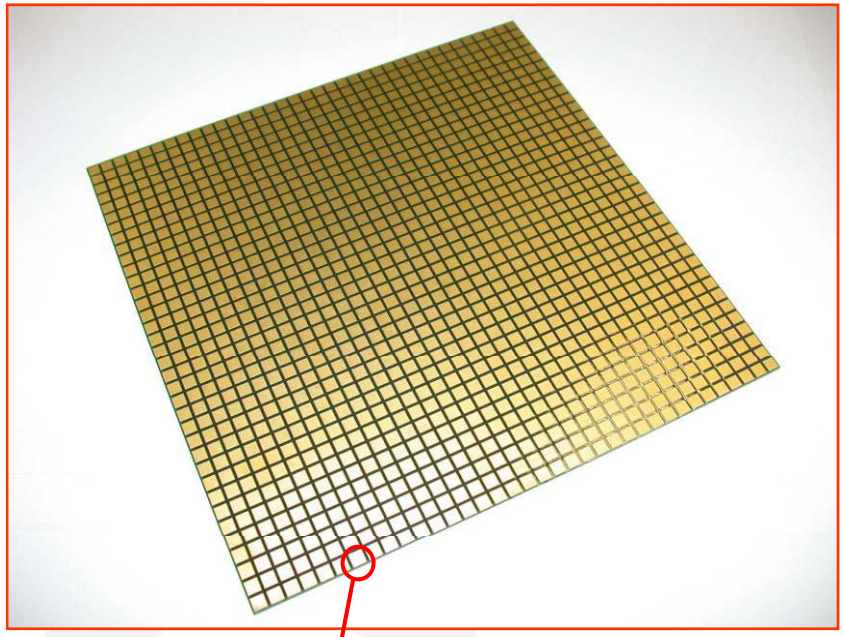
- Large activity on ASIC measurements
  - Validation of readout scheme with HaRDROC (Lyon, LLR, Orsay)
  - Analog characterization of SPIROC (DESY+Orsay)
  - ADC characterization on SKIROC1 (Clermont,Orsay)

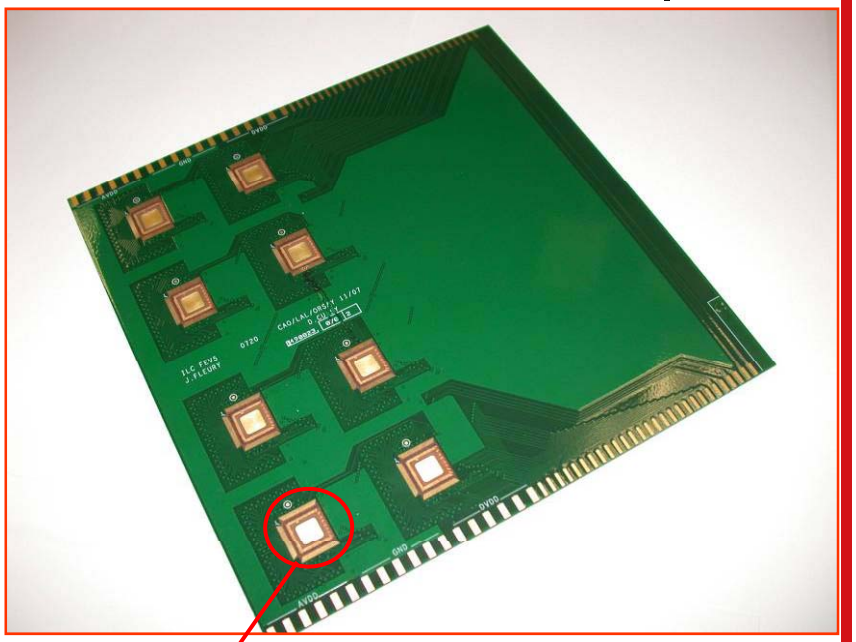
Activities in 2008 (2)

- Front End boards
  - ECAL, DHCAL & AHCAL (see slides fm R. Poeschl and F. Sefkow)
  - Essential for detector mechanics finalization
  - Difficulties with ECAL prototype FEV5 (chip on board, minimal thickness…) => ~6 months delay experienced by present manufacturer and non working !
- DIF (detector InterFace) :
  - ECAL : UK
  - AHCAL : DESY
  - (not EUDET DHCAL : Annecy)
  - See slides from M. Wing

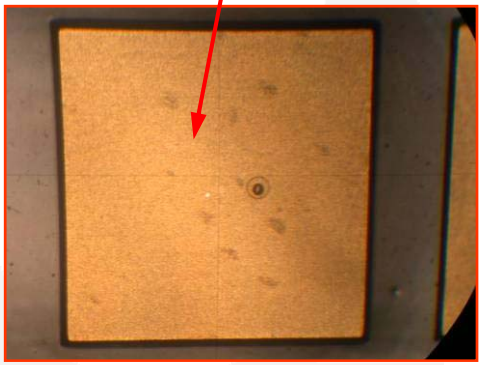


FEV5 : new PCB for ECAL

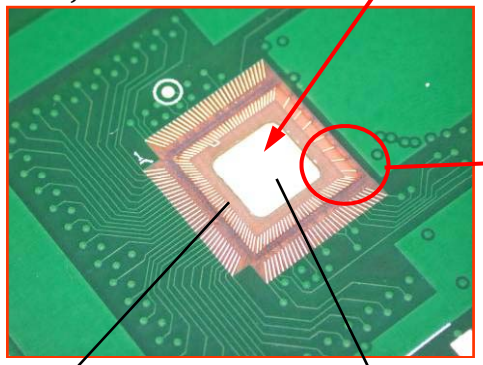


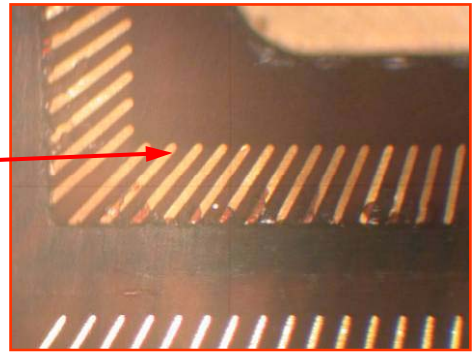


Global dimensions :
180*180 mm, thickness 1.2mm



pixel dimensions : 4*4 mm





0.15mm <depth<0.17mm

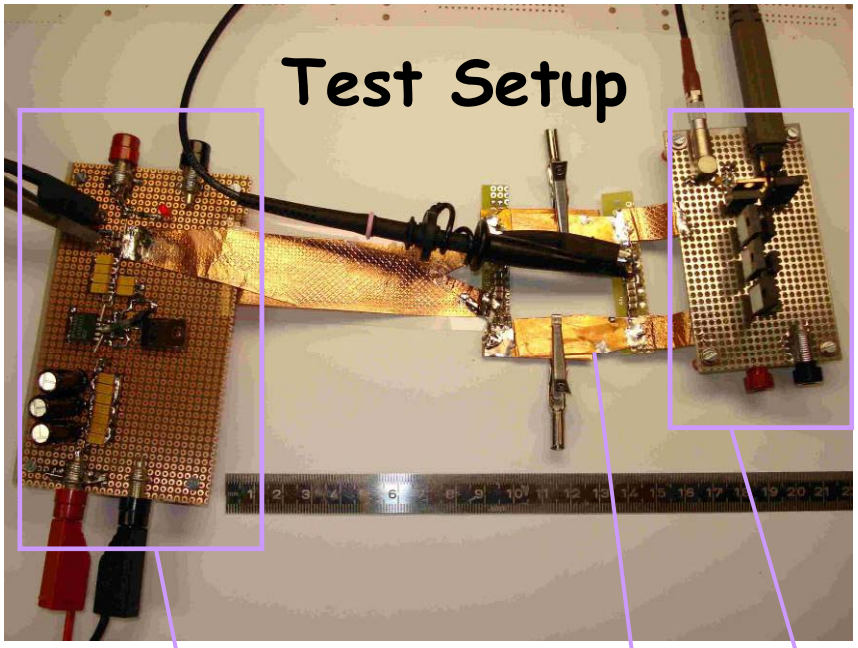
0.6mm< depth<0.7mm

Next steps

- ASICs
  - One engineering run with HARDROC2, SPIROC2 and SKIROC2 spring 2009 financed by CALICE
  - Will be used to populate the EUDET Calorimeter infrastructure
- Front-End boards
  - Difficulties with ECAL prototype FEV5 started in january 08
  - Will proceed to FEV7 with SPIROC2 in oct 08 to meet M36 FEB EUDET milestone, but no guarantee
- Readout
  - Readout Scheme validated on DHCAL with HARDROC
  - First DIFs coming now. Tests starting. Interface to DAQ proceeding [M. Wing]
- Power supplies
  - Looked at by DESY [M. Reinecke]. Important system issues.
- Testbeam

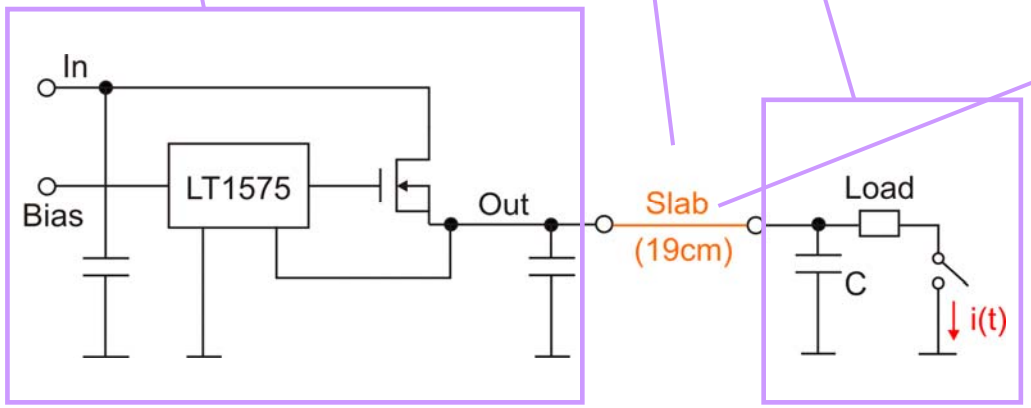
Power cycling test setup

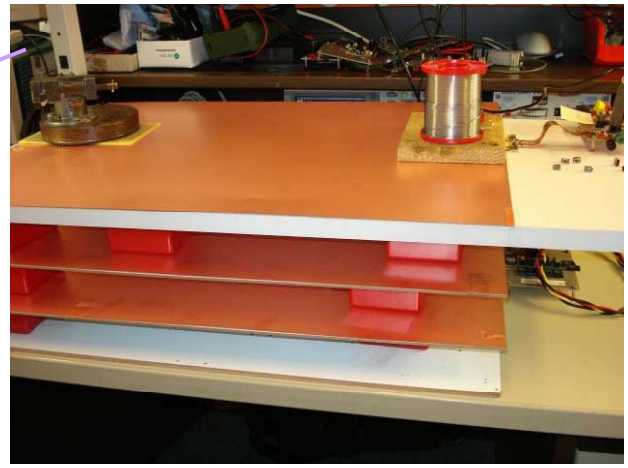
FE



Settling time (Load side):
Voltage within 50mV of final value.
Aim: reasonable values for efficient power cycling (< 50µs)

Overshoot : 0.5 to 5 V
Aim: Protection of devices, stable register settings.





EUDET FEE meetings

- London 8 jan 08
  - ~ 40 participants
- Orsay 2 jun 08
  - Also ~ 40 participants
- Also CALICE meetings :
  - Argonne march 08
  - Manchester sept 08

- Important to coordinate many construction and testing activities
- EUDET web repository for firmware and VHDL code

Summary

- 2nd prototypes of HARDROC (DHCAL) and SPIROC (AHCAL+ECAL) submitted in june 08, expected this week = EUDET Milestone (M36)
- Readout part validated with HaRDROC
- Power pulsing tests performed on HaRDROC
- Front-end boards first prototypes
  - Difficulties with ECAL boards FEV5 : go to FEV7 directly
- DAQ interface (DIF boards) prototyped

- One engineering run with all 3 chips (ECAL, DHCAL and AHCAL) spring 2009 : can be used as « production run »
- Expect busy construction period end 08- beg 09