JRA2-SITRA status Annual Report 2008

A. Savoy-Navarro (LPNHE) on behalf of the JRA2-SiTRA

Partners: HIP Helsinki, LPNHE-Paris, Charles University Prague, IFCA-Santander,
Associates: CNM Barcelona, IEKP-Karlsruhe, HEPHY Vienna, IFIC Valencia, Obninsk State University
And contributions: University of Barcelona, CERN Bonding Lab and Microelectronics, Torino University and INFN
also within the SiLC R&D Collaboration framework

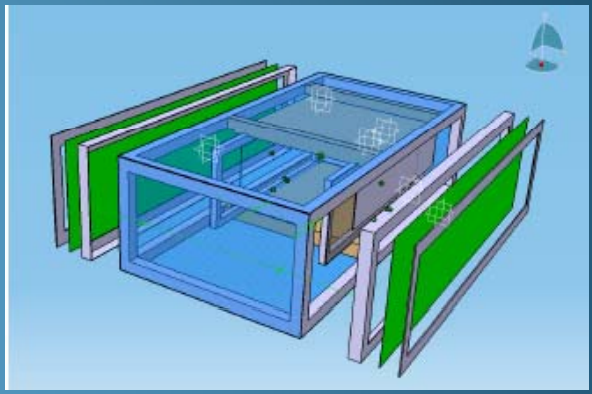
(Following the presentation at the SC by Z. Doležal, Sept 2, 2008)

Milestones and Deliverables(Past)

Milestone Deliverable	Deadline	Status
Convection cooling system prototype	22	Ready
Motorised 3D table	24	Ready
Central tracker prototype	24	Ready
FE chip version 1	24	Ready

Convection Cooling System Prototype

(LPNHE +OSU) Eudet-Memo-2007-52



	Preamp	Shaper	Zero suppr.	Pipe-line	Total Analog	ADC	Logic	Total Digital
180nm/ch	90	180			270			
130nm/ch	148	148	198	10	575	66		
Common				100		5	96	101

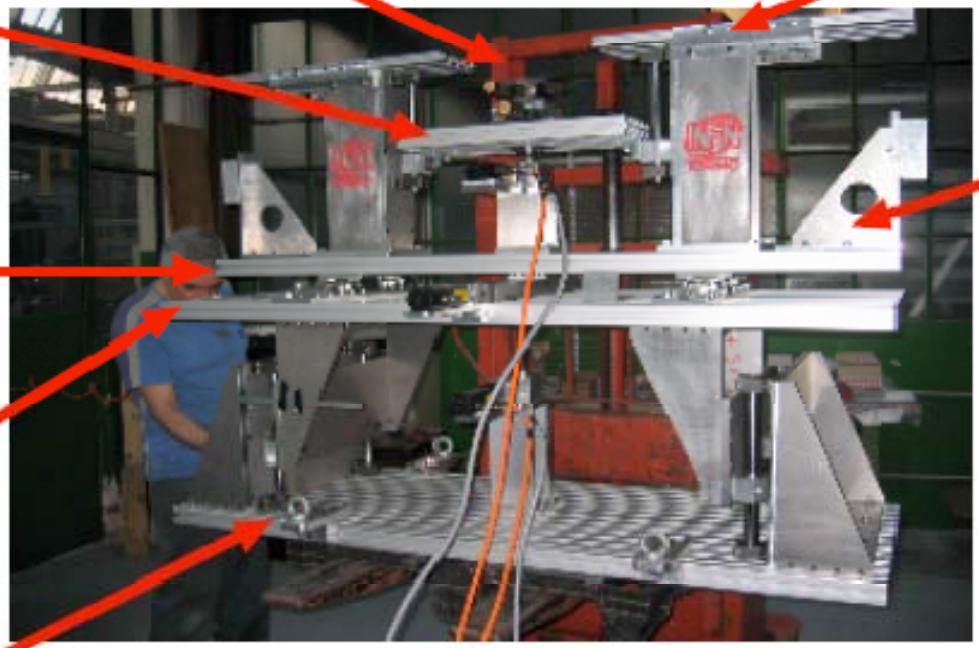
SiTR_130-4 results: ~ 0.6mWatt/ch
No power cycling included
→Main problem: power dissipation from neighbors

Motorized 3D Table (Torino)

- suitable for testing Silicon sensors, pixel and microstrips in a beam test,
- DUT can be moved and rotated with respect the beam line.
- built in a modular way, so that it can arrange different types of DUT, with alignment telescopes or without.
- 5 motors are controlled remotely via RS232, to set positions and angles, via LabVieW application

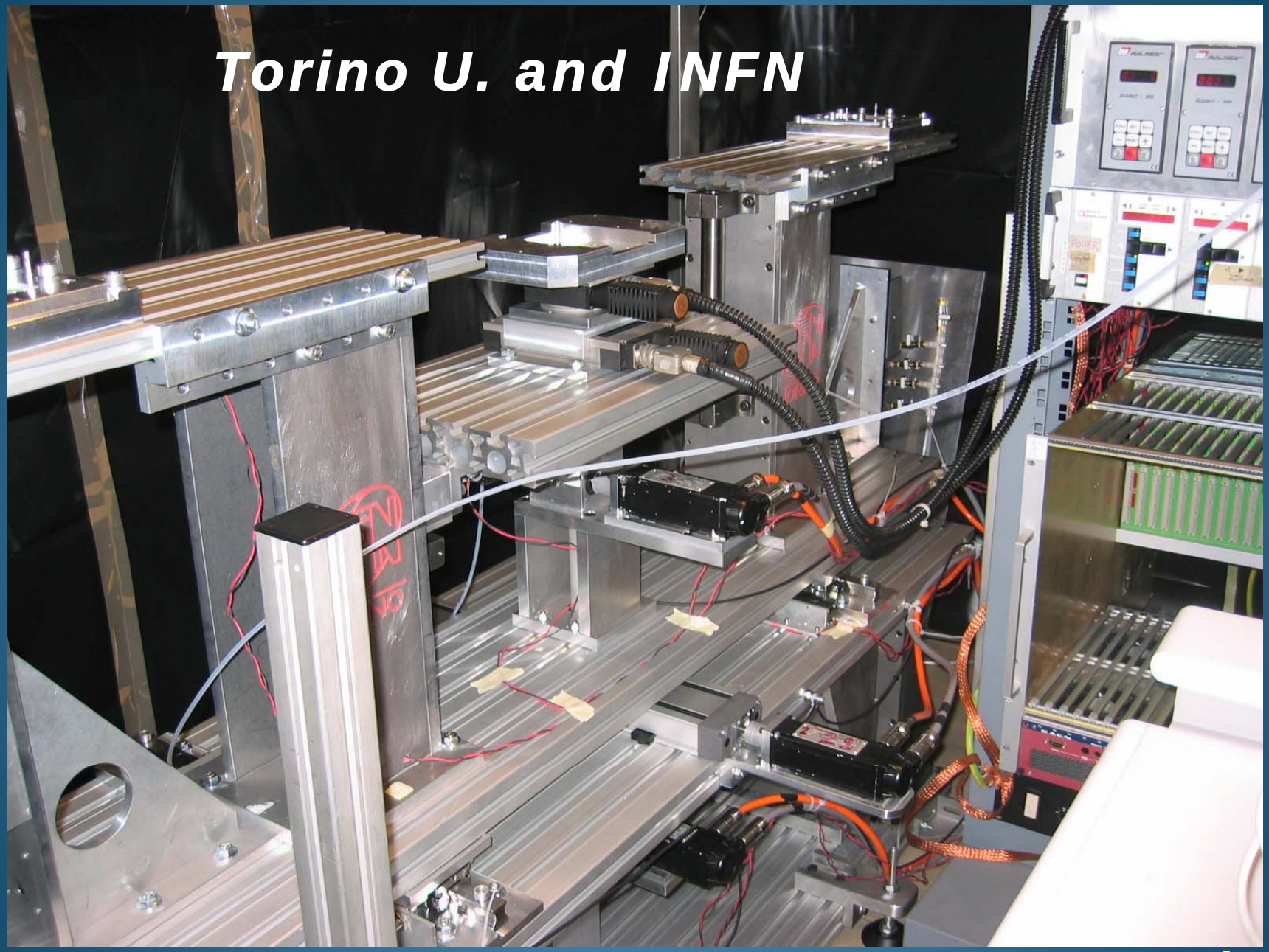
- Eudet-Memo-2007-59

Torino U. And INFN



Movements:
Base A DZ=28 cm
Base B DY=20cm
Base C DZ=16cm
Support D, DY=5cm,Dphi=+-90^{O}

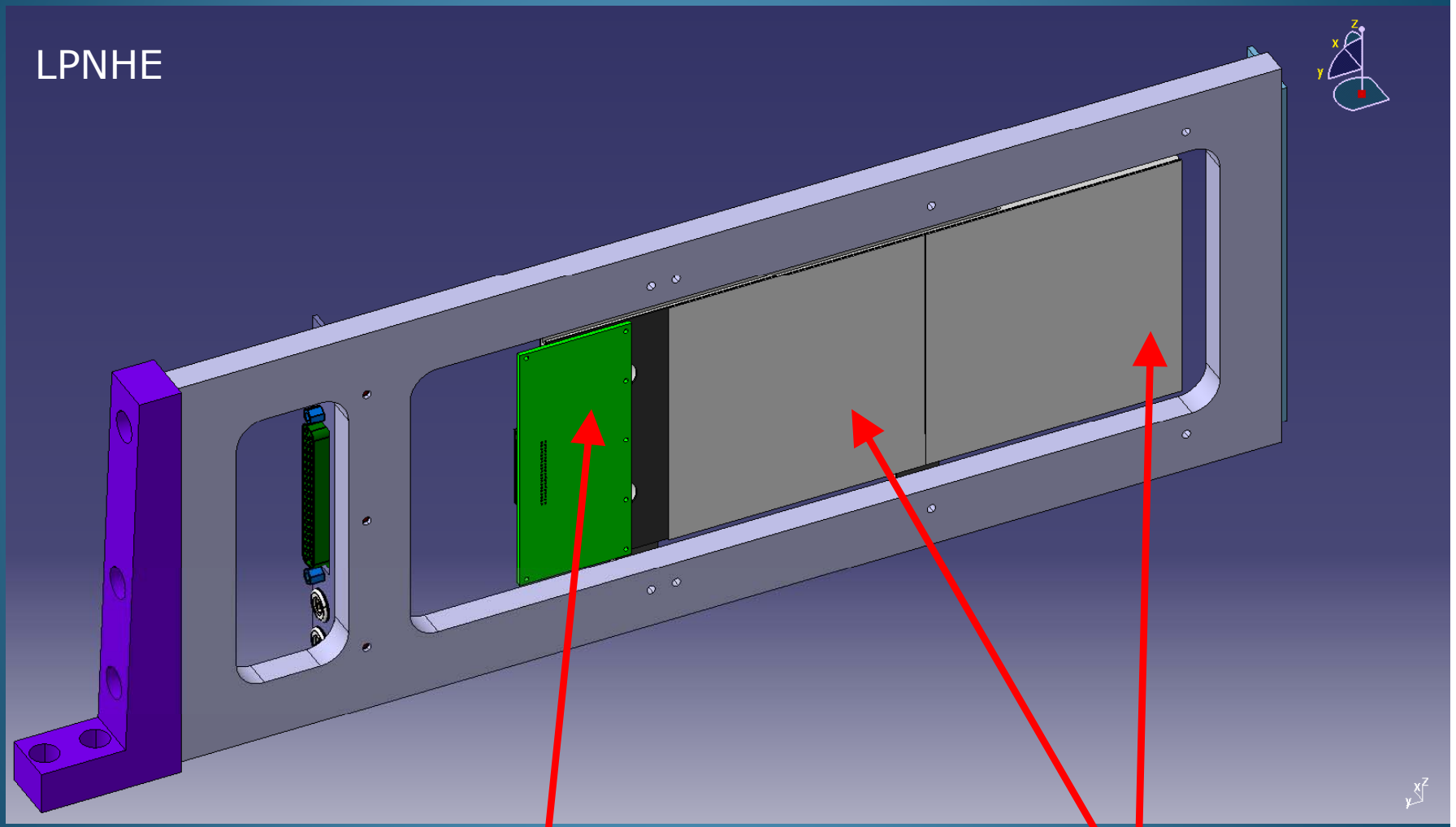
Torino U. and INFN



Central tracker prototype

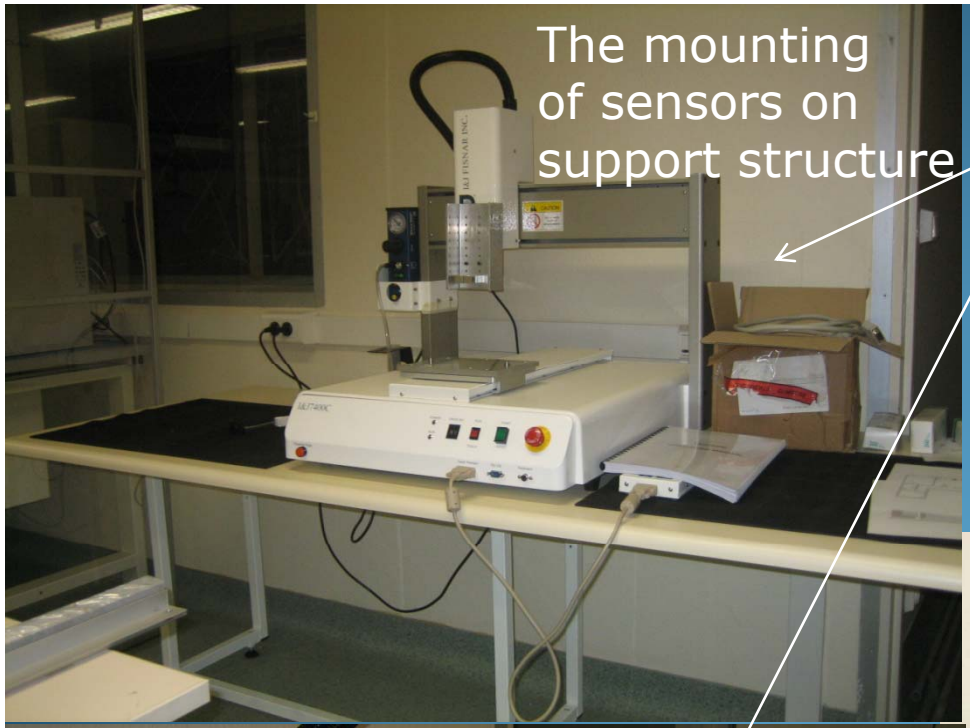
- Several detecting module prototypes have been assembled with sensors and electronics
- Tested at Lab test bench
- Beam test at DESY and CERN

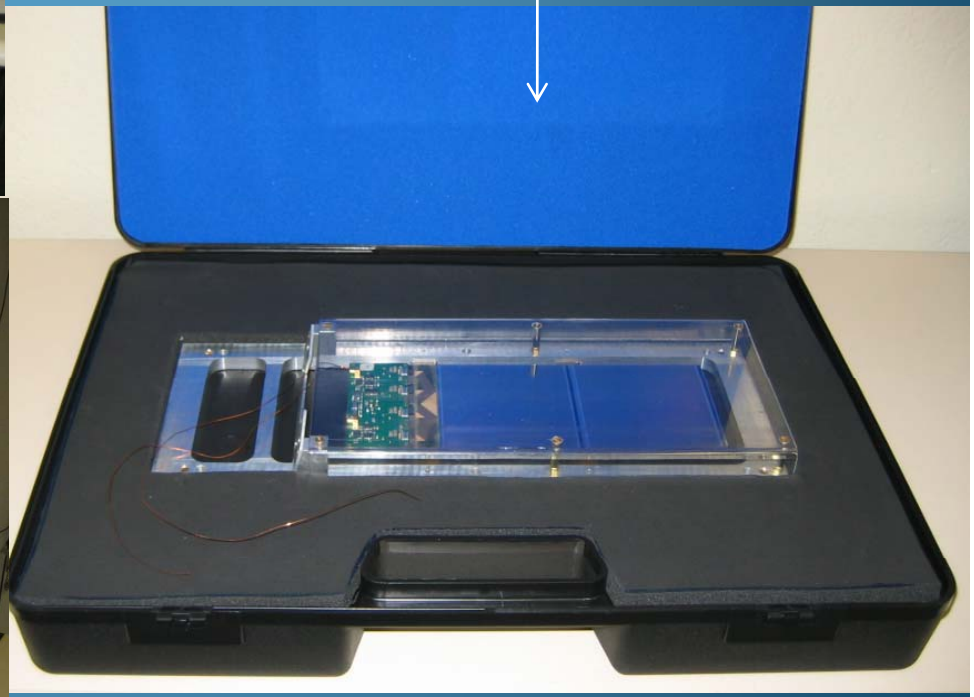
Module prototype (mechanical design)



The fabrication and the module

(LPNHE)



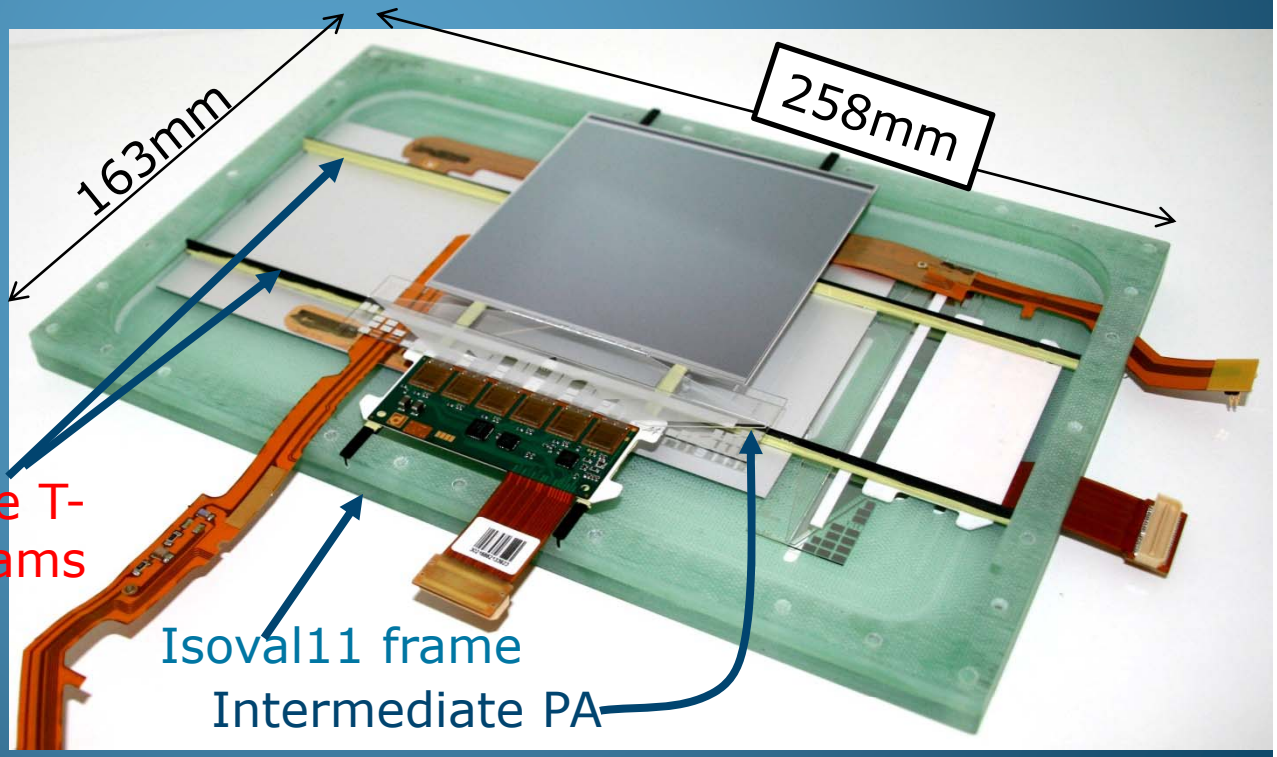


See A. Charpy's talk at JRA2-SiTRA

MODULES BUILT for LPTPC *(IEKP+HEPHY)*

- aluminium on quartz **Intermediate Pitch Adapter** to connect the CMS R2 pitch of 143 μm to the readout strips of the HPK Sensor with a pitch of 50 μm - Helsinki Institute of Physics (HIP)
- two **carbon fibre T-beams** are the backbone of each silicon detector – 2 rectangular beams from SECAR Technologies glued together
- **Isoval11 frame**: a composite of resin epoxy reinforced with a woven fibreglass mat

Total thickness: 18mm



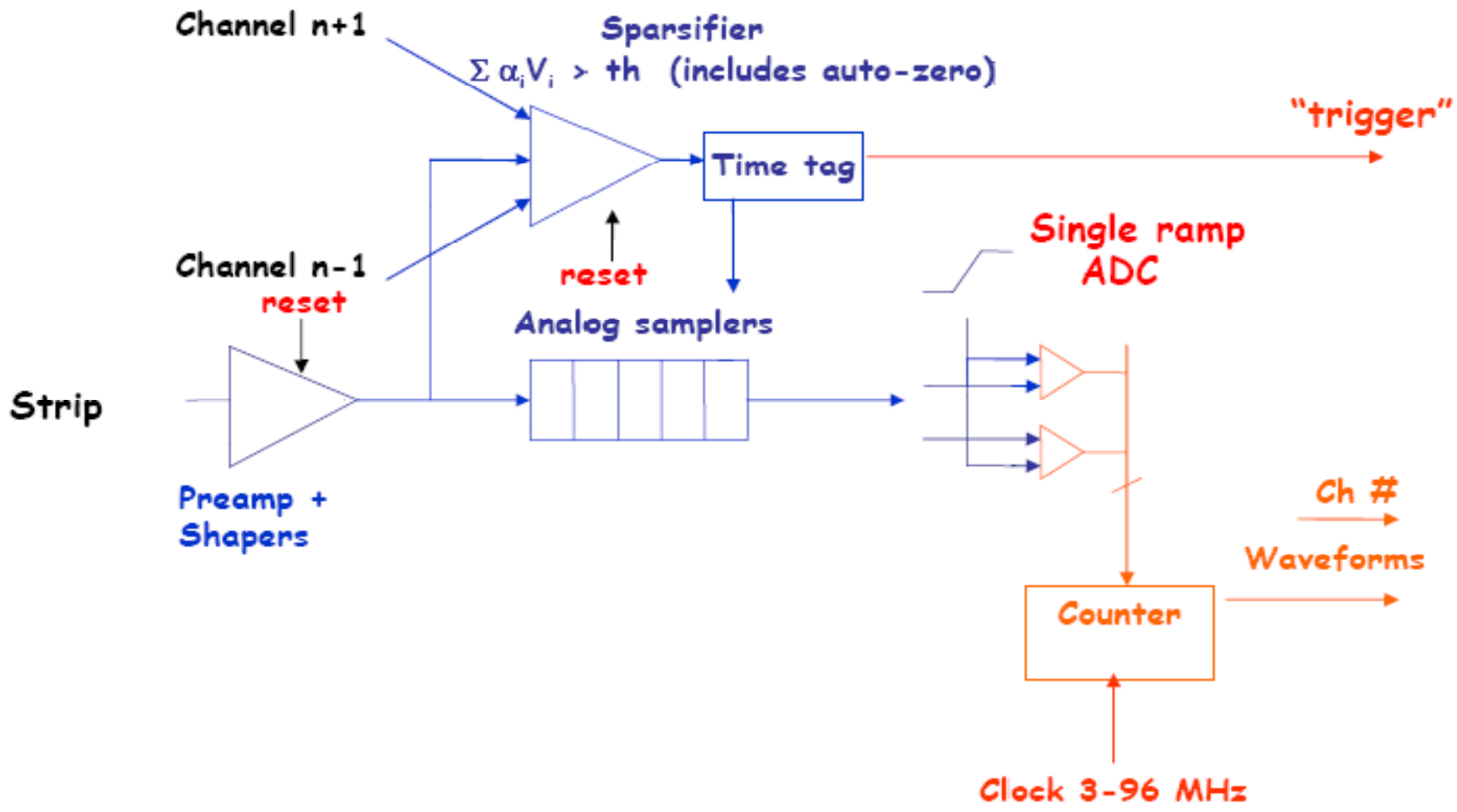
See S. Haensel's talk at JRA2-SiTRA

FE Chip version 1 *(LPNHE)*

See T.H. Pham's talk at JRA2-SiTRA

- After first prototype in 180 nm technology, 4-channel SITR-130_4 chip was designed in 130 nm and produced
- The chip was fully tested both standalone and with a strip sensor attached
- Based on the test results version 2 has been designed and submitted
- Version 1 documented in EUDET-Memo-2007-29

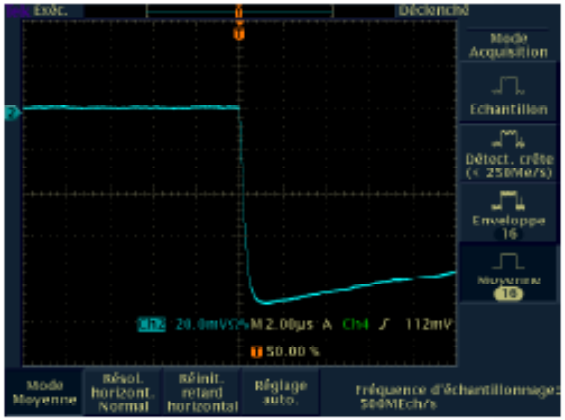
4-channel Chip



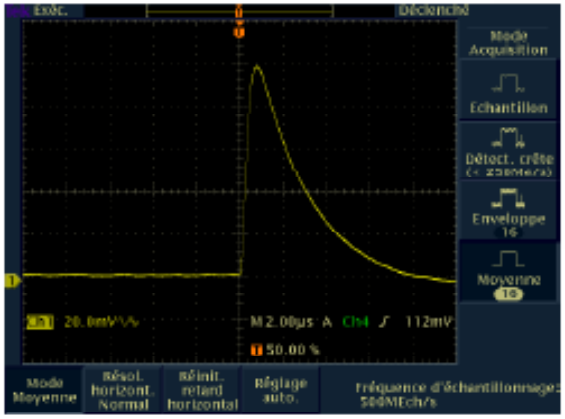
Preamp-shaper results

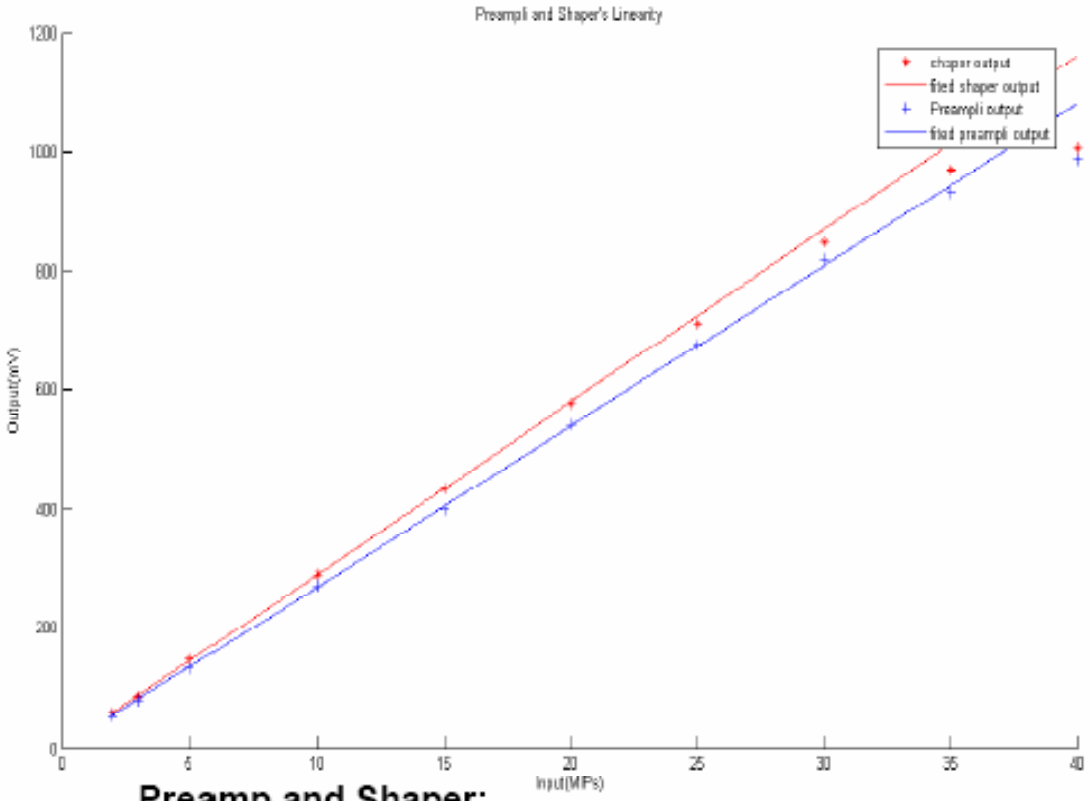
Measured gain - linearities

Preamp output



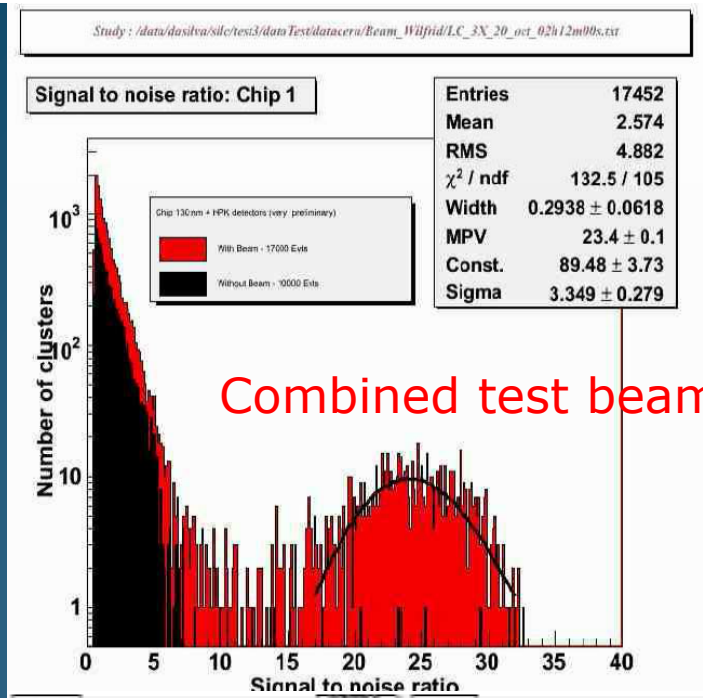
Shaper output

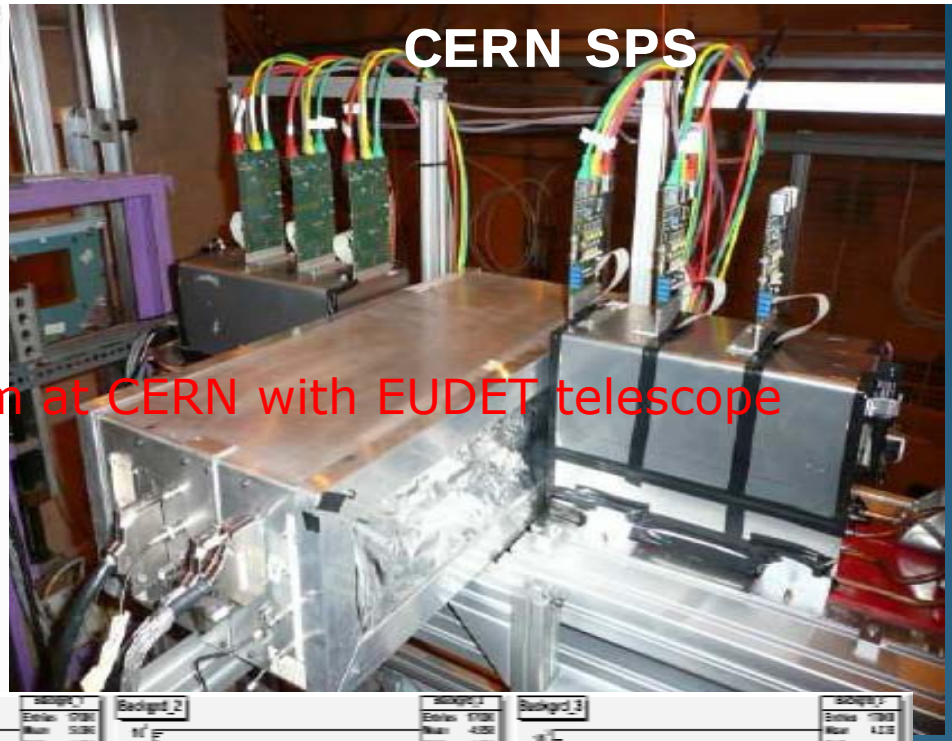




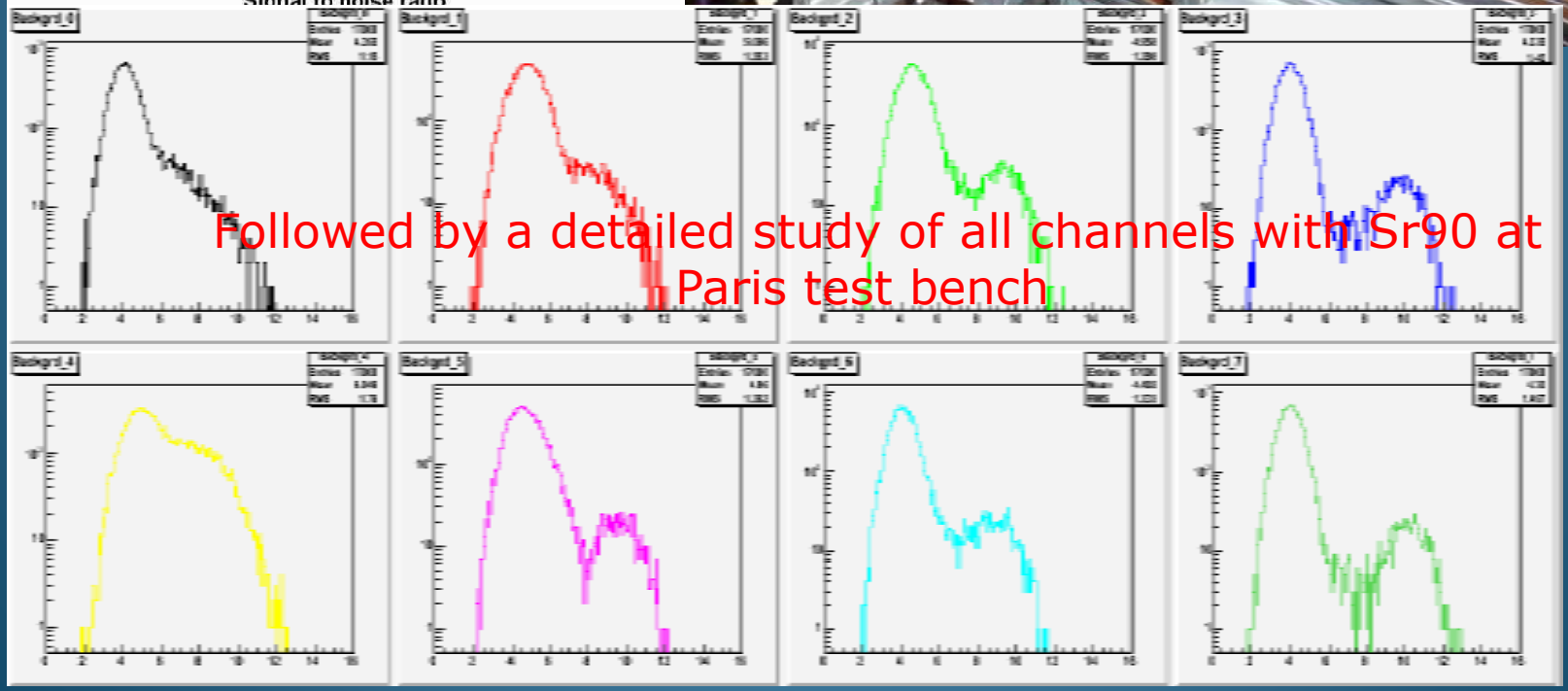
Preamp and Shaper:

Gain = 29mV/MIP
Dynamic range = 20MIPs 1%
30 MIPs 5%
Peaking time = 0.8-2.5µs / 0.5-3µs expected





Combined test beam at CERN with EUDET telescope



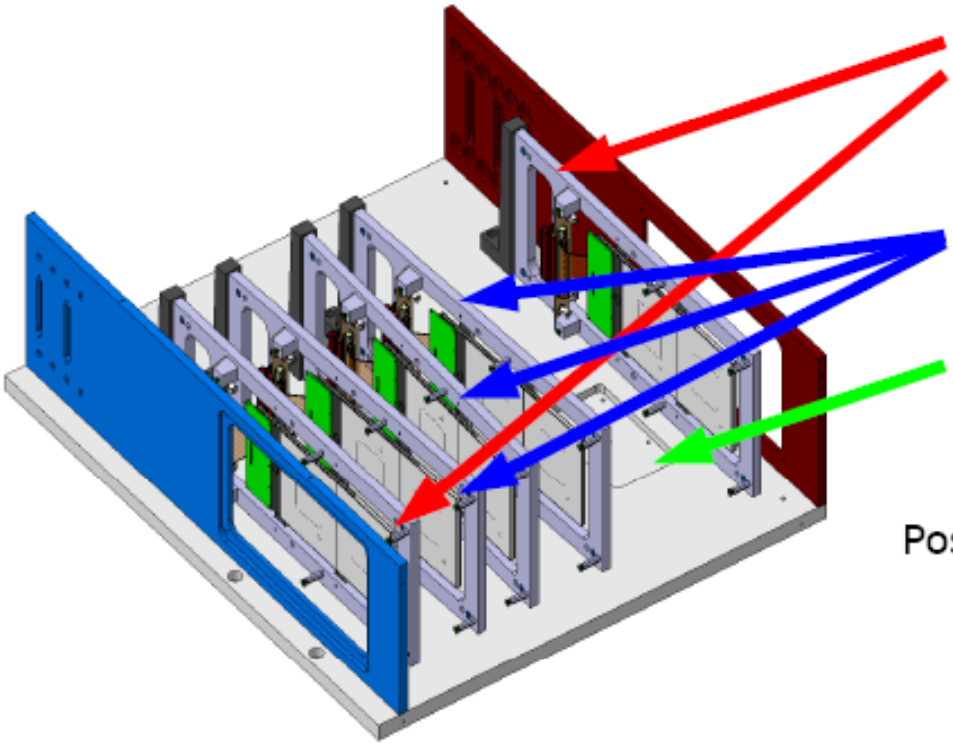
Followed by a detailed study of all channels with Sr90 at Paris test bench

Milestones and Deliverables (present)

Milestone Deliverable	Deadline	Status
Conduction cooling system prototype	36	Ready 40
Large Silicon tracking structure	36	Move to 43
Forward tracker prototype	36	Move to 43
Alignment prototype		Delivered 43
FE chip version 2	36	Delivered 38
Silicon test infrastructure available for users		Delivered 43

Conduction Cooling System Prototype

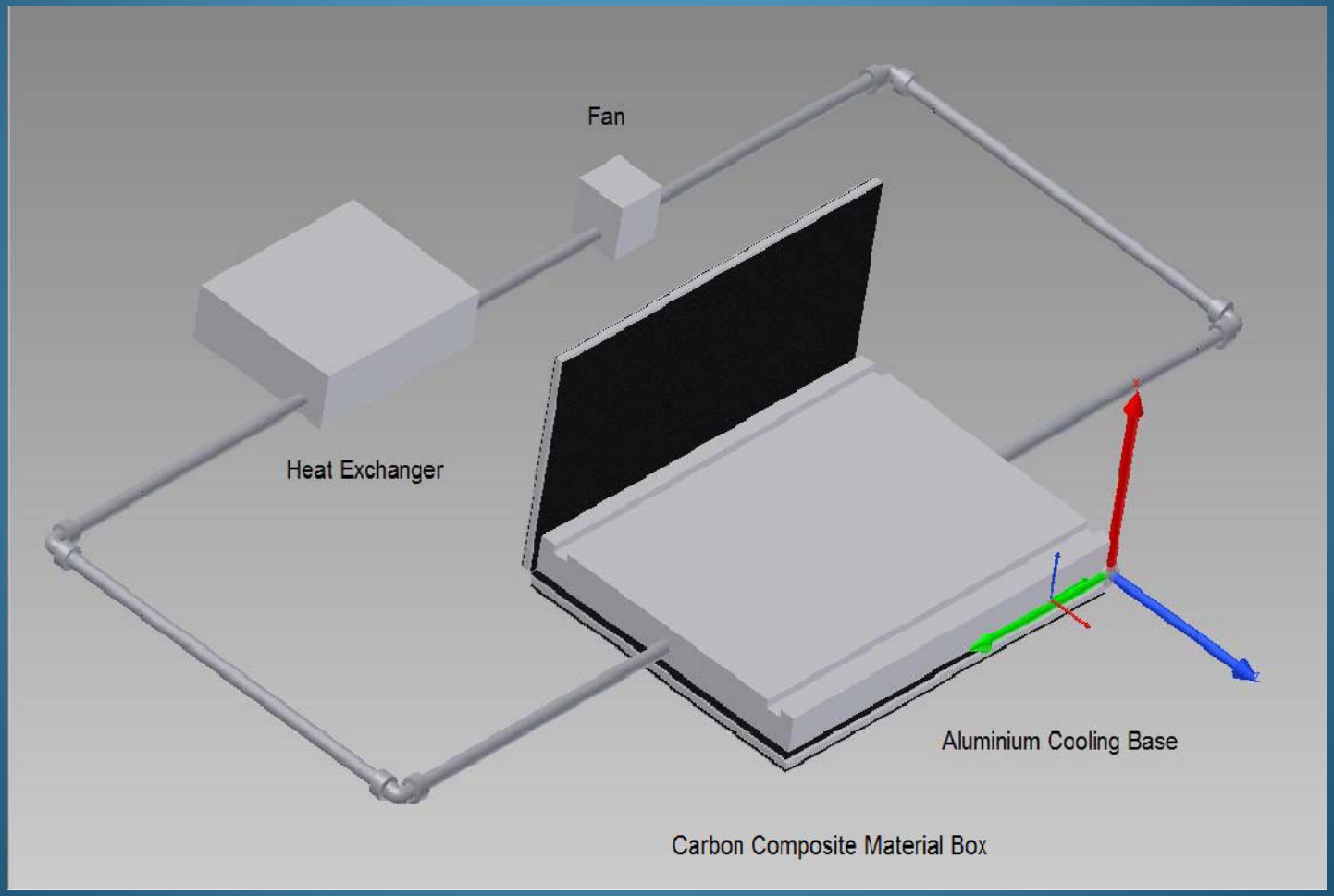
- Designed by LPNHE and OSU
- Description, calculations and test results in Eudet-Memo-2007-52
- Conventional material prototype ready for October 2008 CERN beam test
- EUDET prototype will be built afterwards from composite carbon fibre structures (ready 43)



Conventional material prototype ready by end of next week to be used at the forthcoming test beam at CERN (Nov 1-12)

IFCA, LPNHE, OSU and contribution from the DESY workshop

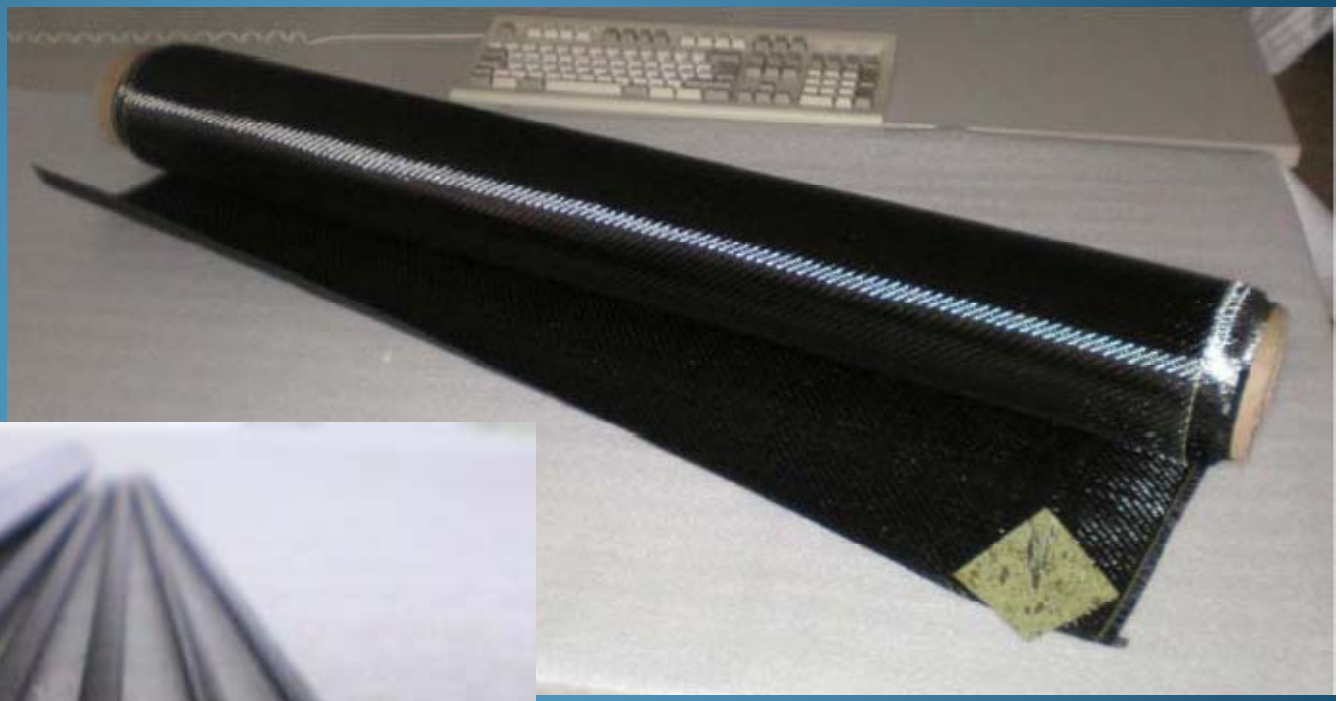
Conduction Cooling System Prototype: Principle *(osu)*

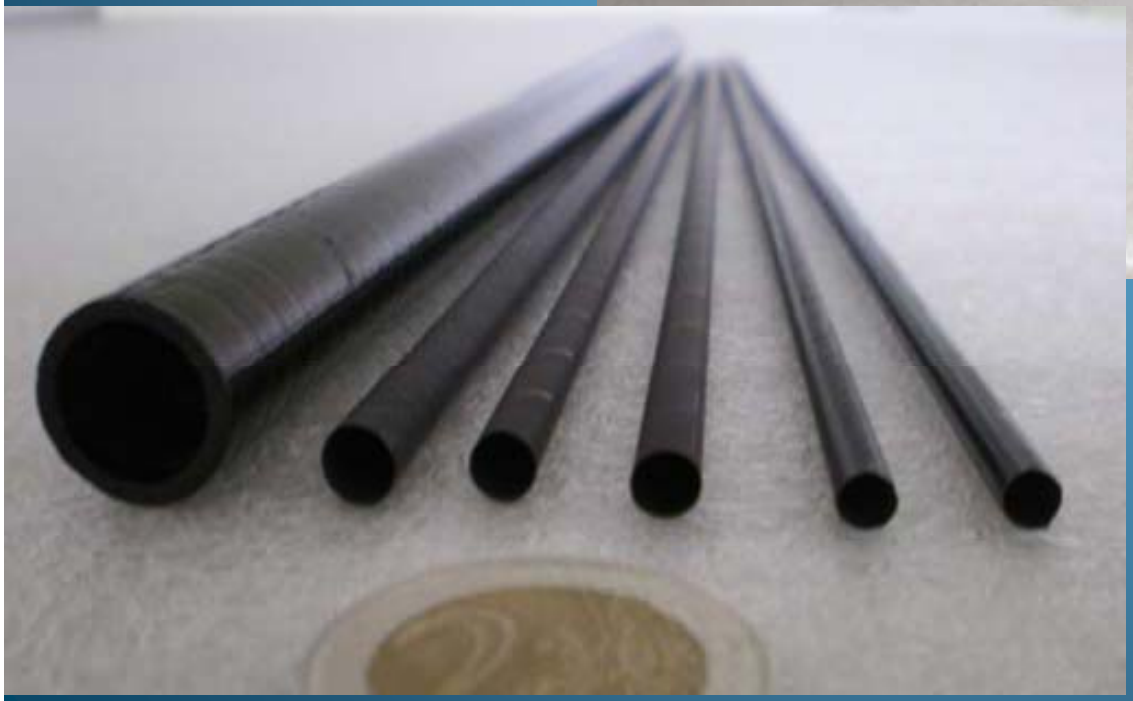


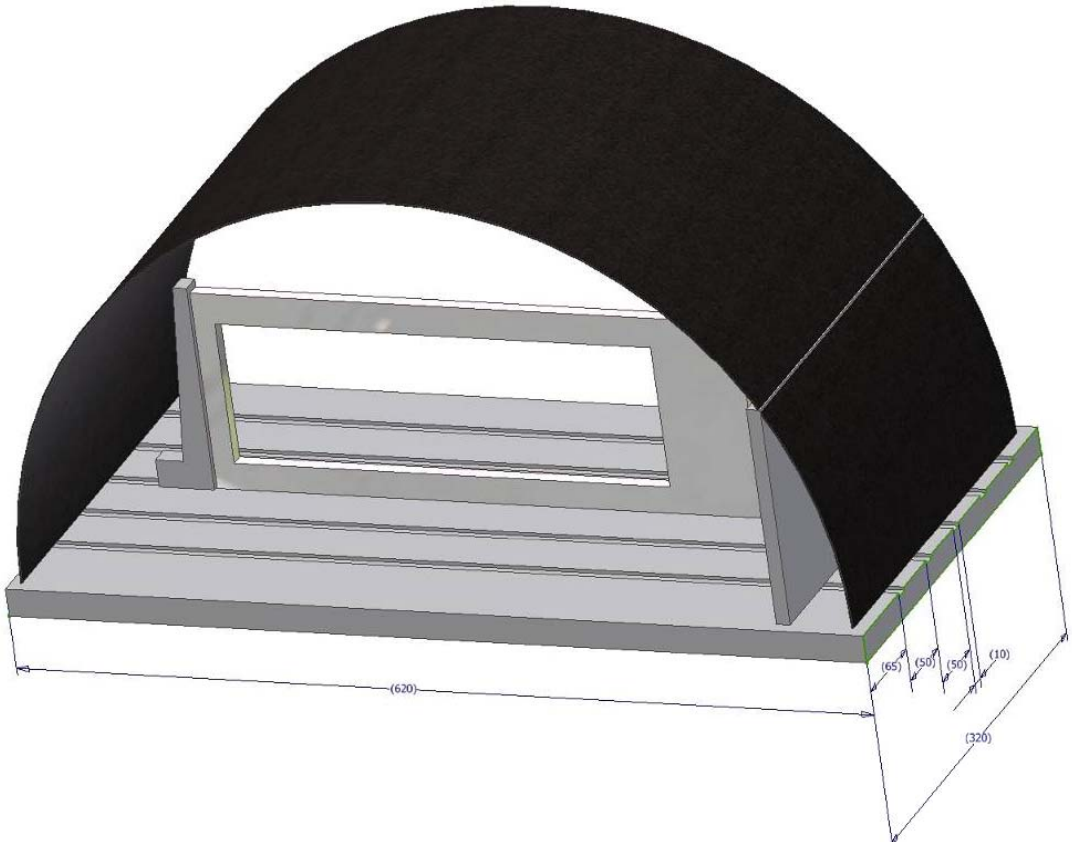
Composite materials

Honeycomb

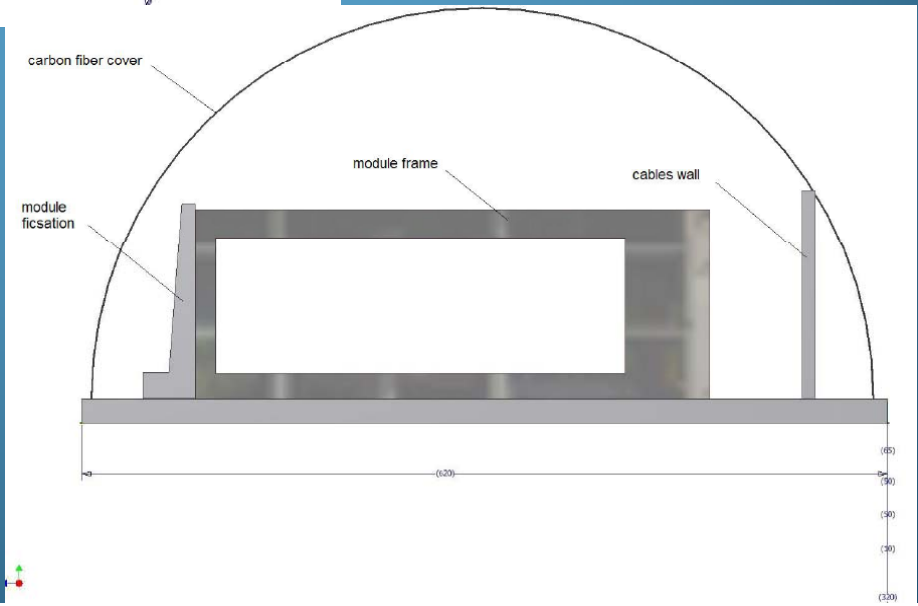
Low material budget







Conduction Cooling System Prototype: Module box ready Week 43 (OSU)

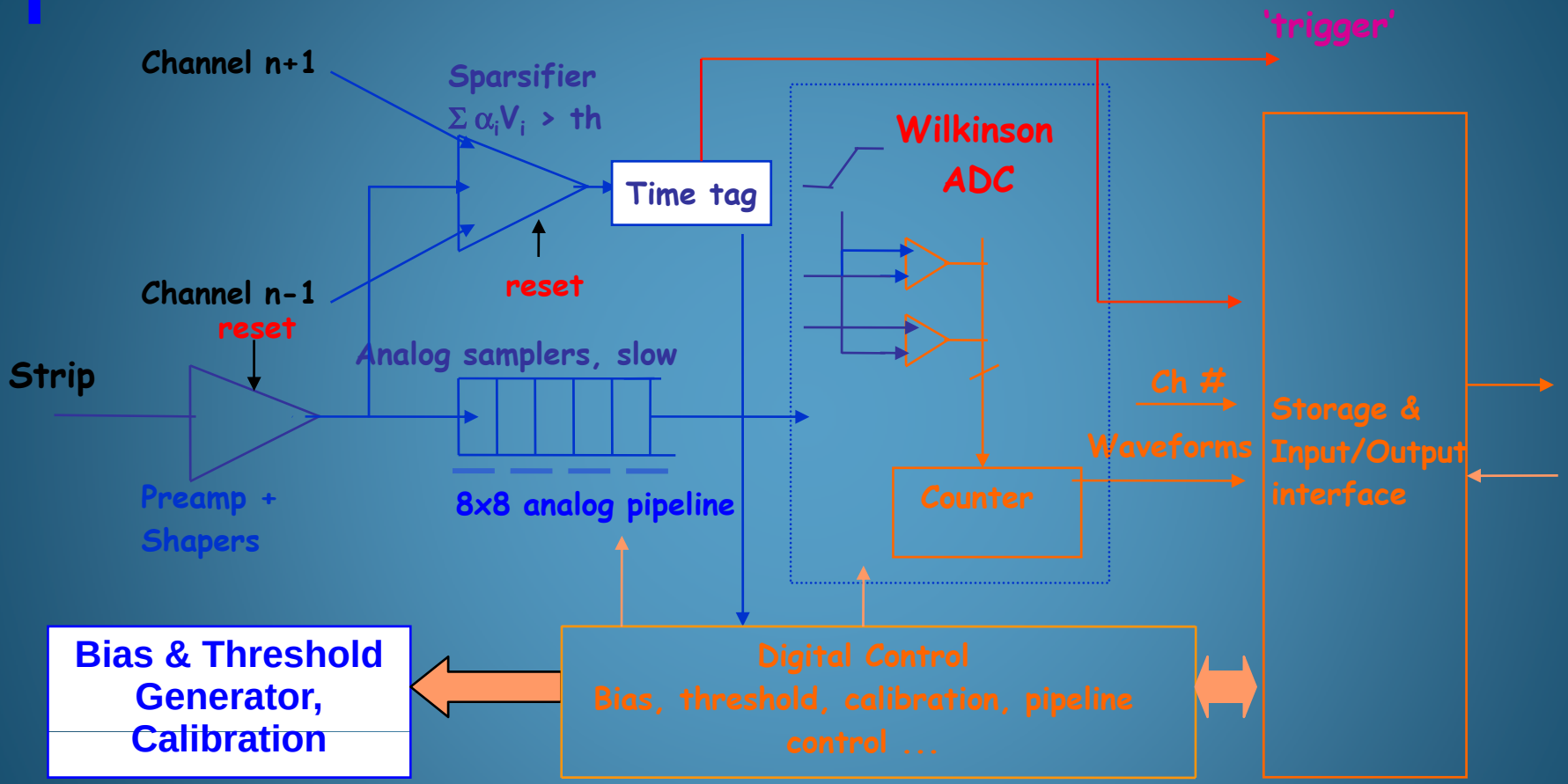


FE Chip version 2 *(LPNHE+U. Barcelona)*

See T.H. Pham's talk at JRA2-SiTRA

- After successful tests of FE version 1 chip (SITR-130_4) 88-channel version was designed in 130 nm and submitted June 24
- Delivered from the foundry September 12
- After thorough testing chip will be assembled into detecting modules

General view of the circuit



Main features of new circuit

88 channels (1 test channel): Preamplifier, shaper, sparsifier, analogue pipeline (8x8 cells), 12 bits ADC

2D memory structure: 8x8/channels

Fully digital control:

- Bias voltage(10 bits) and current (8 bits)
- Power cycling (can be switched on and off)
- Shaping time programmable
- Sampling frequency programmable
- Internal calibration (fully programmable 10 bits DAC)
- Sparsifier's threshold programmable per channel
- Event tag and time tag generation

=> High fault tolerance

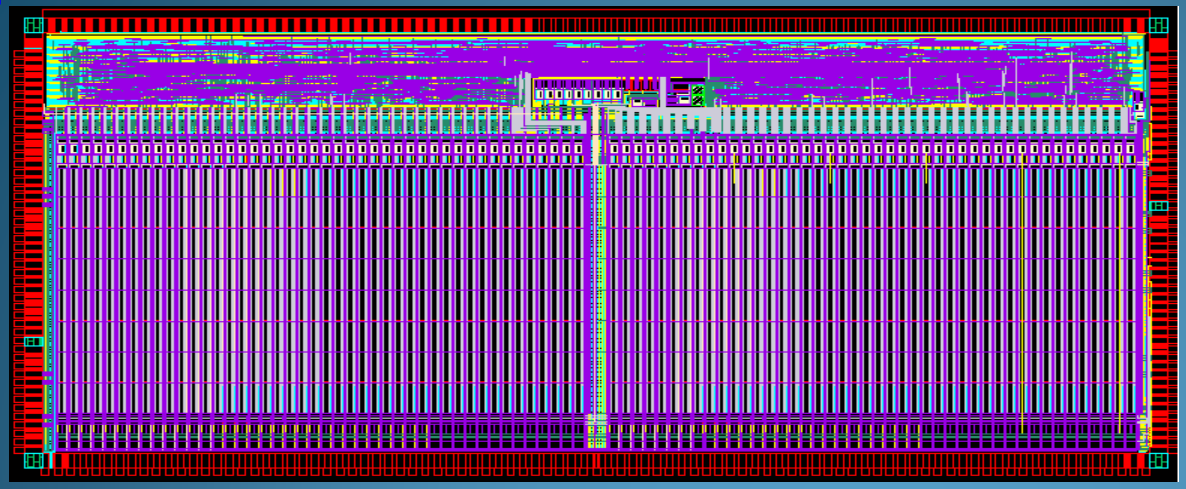
=> High flexibility, robustness

.....

2 Trigger modes: Internal (Sparsification integrated)

External (LVTTL) for beam test

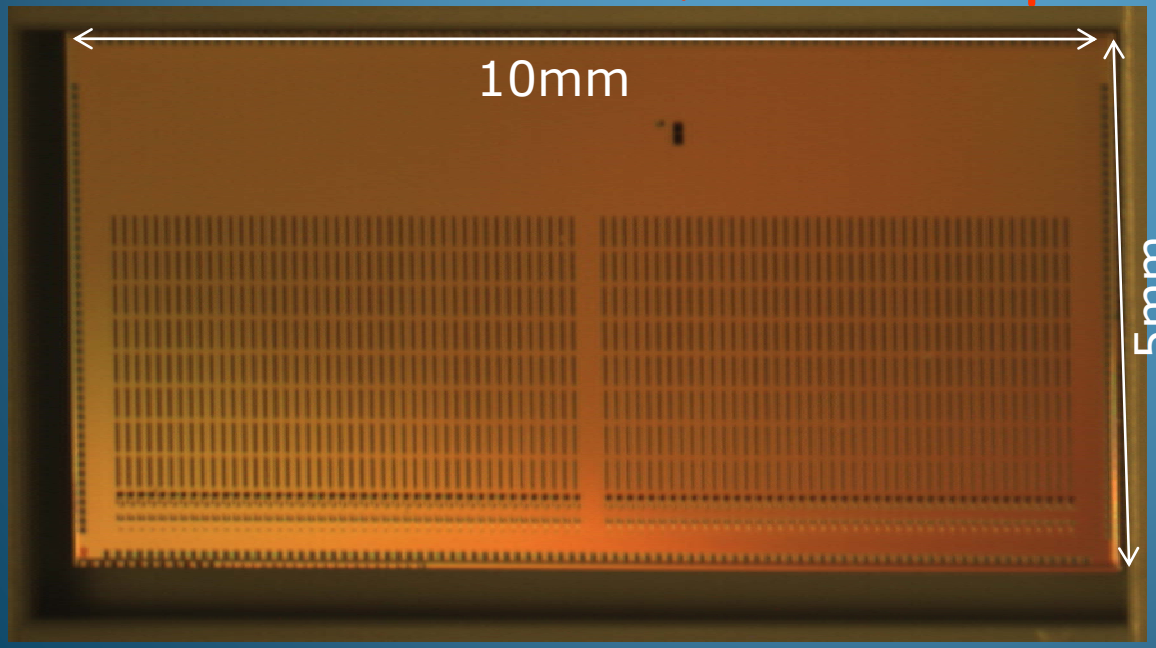
LAYOUT VIEW and PHOTOGRAPH



Size: 5mmx10mm
88 channels (105um pitch)
105umx3.5mm/channel

Analog: 9.5mmx3.5mm
Digital : 9.5mmx700um

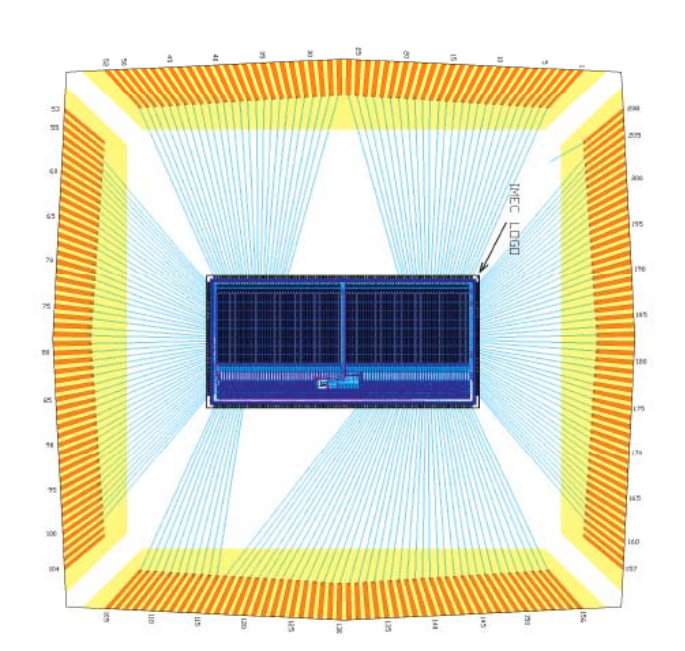
Submitted June 24th '08, received September 12 the naked chips



Photograph of the new chip SiTR_130-88

New readout circuit in 0.13 µm

BONDING DIAGRAM FOR CQFP208 PACKAGE



Package 208 pins
- 50 analog input
- 21 analog test out
- 33 digital pin (22 test pins)
- 107 supply pins

20 packaged chips delivered this week:

For a a detailed test of chip functionality & performances

Test is “easy” because the chip is “fully programmable”

Forward tracker prototype

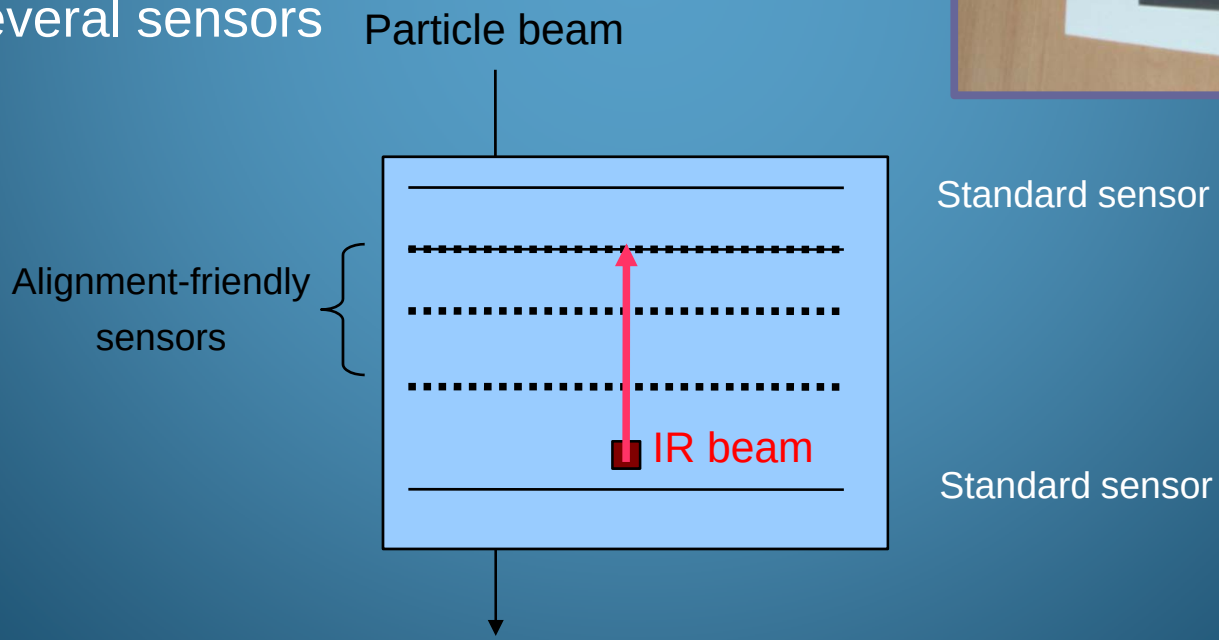
- Detector modules equipped with special alignment sensors
- IR Laser alignment will be performed
- These modules will be tested at October CERN beam test
- this deliverable would benefit from postponing the deadline from M36 to M42

Alignment prototype on beam

See M. Fernandez-Garcia's talk at JRA2-SiTRA

IFCA-SANTANDER + CNM

November 1-11, test beam will study performance of new HPK alignment sensors
These are "standard" sensors with an Al-free window in the backside (ohmic contact)
IR beam pseudo-track can be used to traverse several sensors

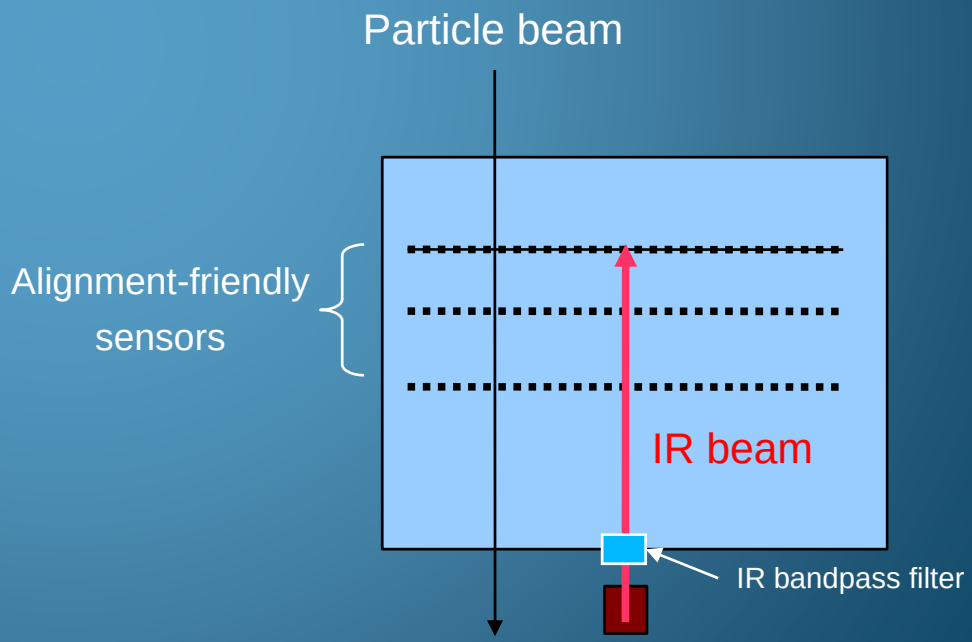


Alignment prototype on beam

See M. Fernandez-Garcia's talk at JRA2-SiTRA

1) Show that the performance of the alignment friendly sensors is the same as the standard ones
2) Compare track reconstructed geometry to IR beam reconstructed geometry
3) Shift only central alignment sensor and compare reconstructed displacement with particle beam and with IR beam

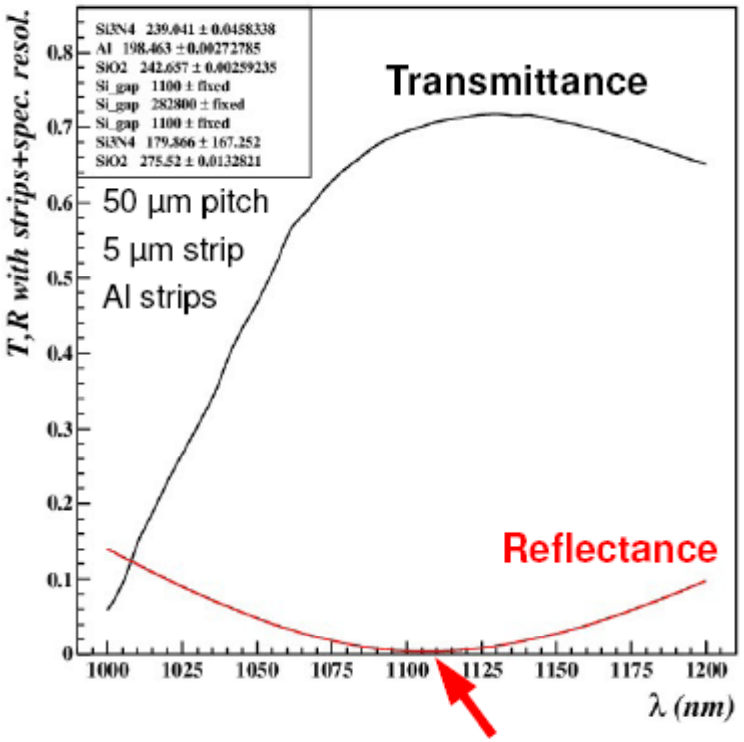
The same setup employed in the test beam can be used as well as an alignment monitor. We just need an IR transparent window in the front side of the cage (it can be a small band pass filter).



Validation of patterned layers simulation

Simulation with strips. Not yet validated. This work is ongoing.

Example of predictions:



Typical AntiReflection Coating signature

Optimized for maximum %T, thin layers
No thickness tolerance studied yet

Maximum %T for a realistic sensor of 70%

Samples of **known** strip detectors without back Al provided by CNM ⇒ validation

We expect to have a transparent design with strips ready by the end of this month

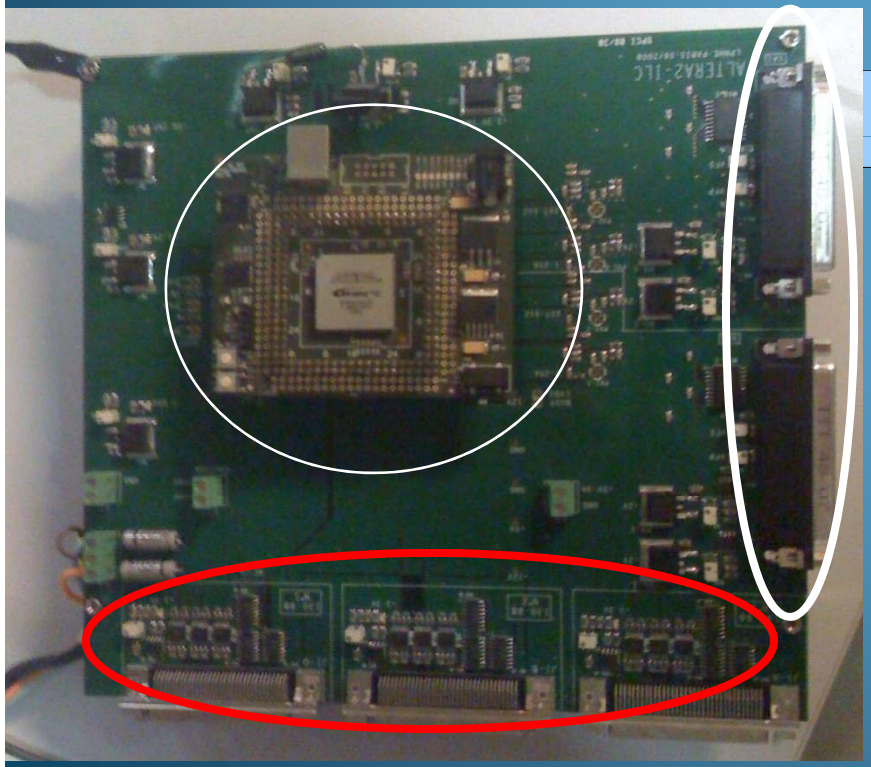
Ready end of 2008

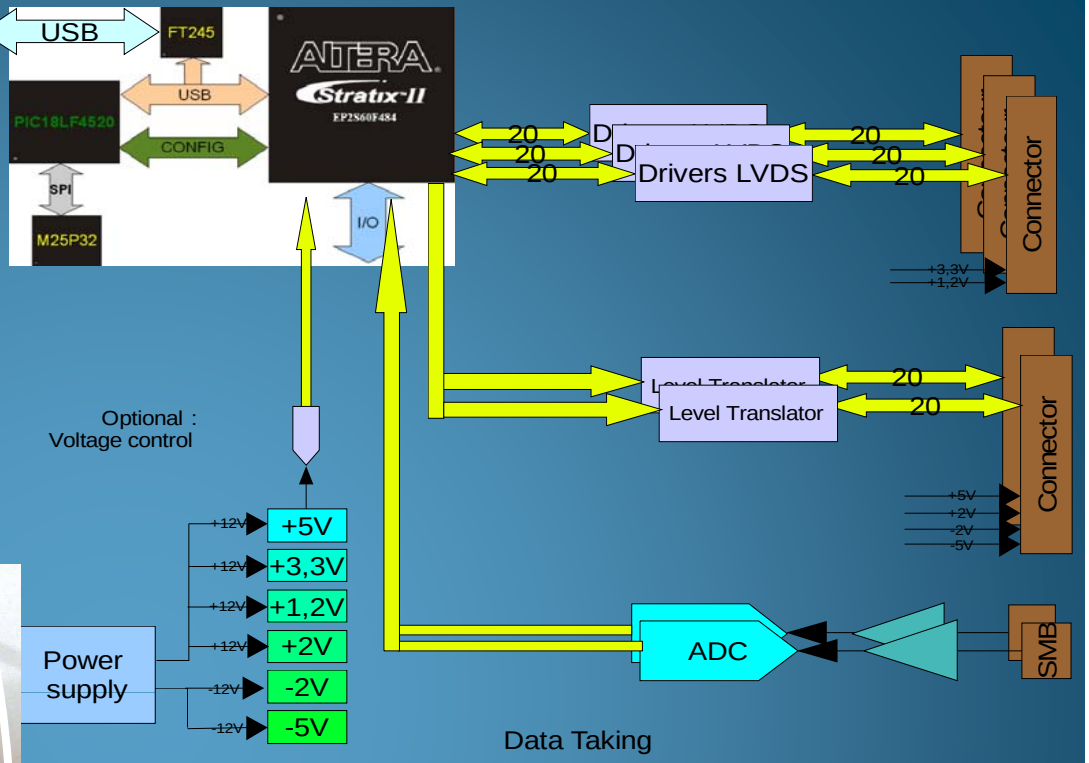
Silicon tracking infrastructure

- Various facilities needed for successful detector testing
  - Cooling
  - Alignment
  - 3D motion
  - Tracking modules
  - FEE
  - DUT DAQ
- Ready by week 43 at CERN
- Overall infrastructure will be available for users (see next)

Barcelona U. + LPNHE

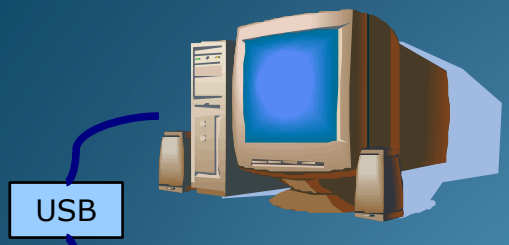
The FPGA board





Synoptic of the new
FPGA board for new Front End

+ associated DAQ software and
interface with the EUDET DAQ



Up to 40m
USB Extender

USB

USB Hub

Up to 3 FPGA

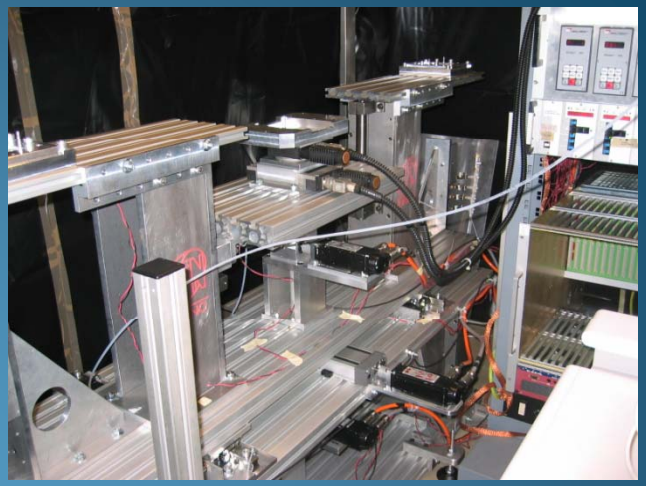
USB
FPGA & drivers

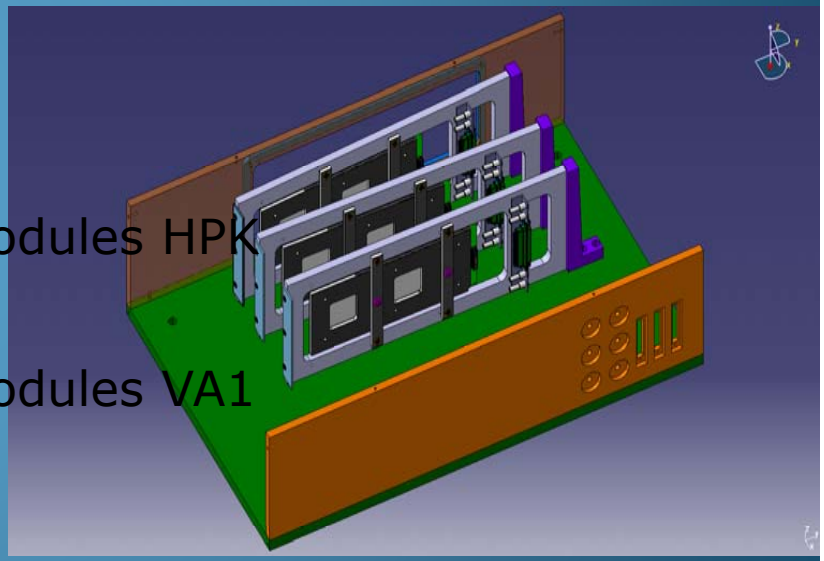
To 3 modules HPK

To 2 modules VA1

USB
FPGA & drivers

USB
FPGA & drivers





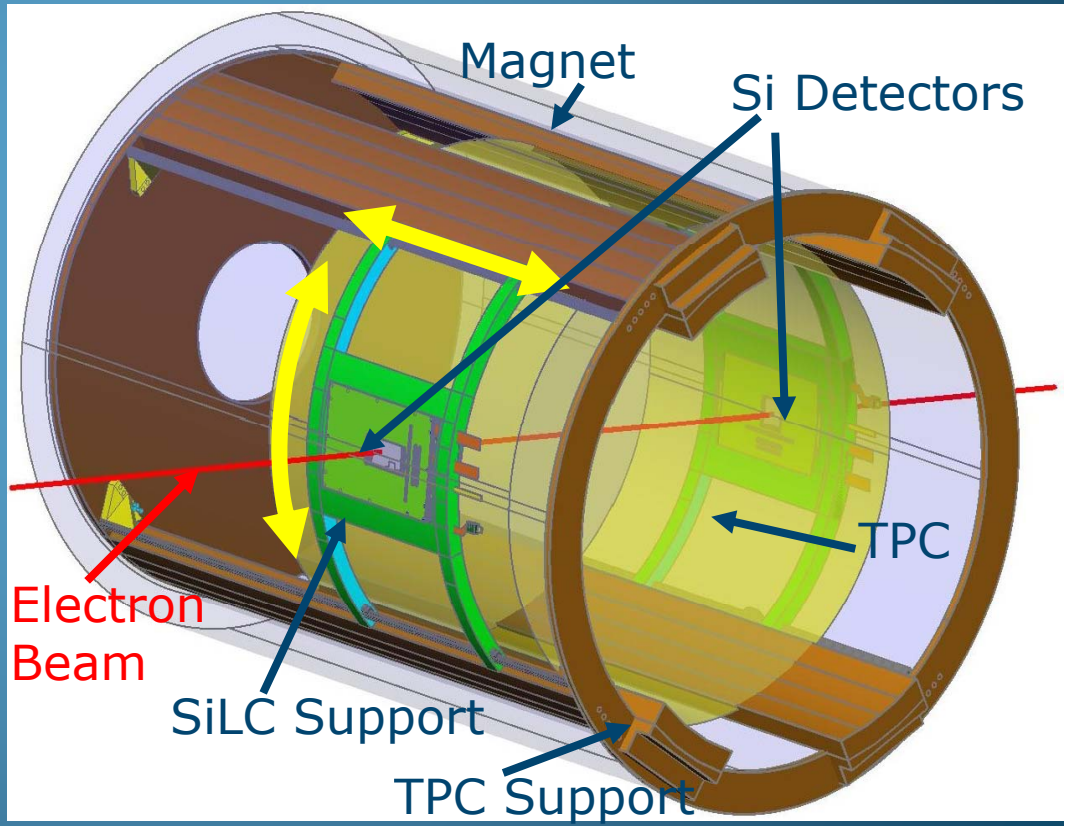
A full test beam Silicon tracking infrastructure

See A. Charpy's talk at JRA2-SiTRA

LP-TPC: Silicon Envelope

(HEPHY, IEKP Karlsruhe, LPNHE)

- **four silicon modules** will be installed:
  - two in front and two behind the TPC, with respect to the e^--beam
    - two independent support structures are needed
  - on each side:
    - one horizontal module consisting of two daisy-chained sensors
    - and one vertical module consisting of one sensor
- **movable support system** is needed because it must be possible to scan the TPC
  - the TPC and the magnet will move relative to the beam
  - the sensors have to stay inside the beam line



See S. Haensel's talk at JRA2-SiTRA

EUDET Memos+Reports

Year	Memos	Reports
2006		1
2007	9	1
2008	7	1

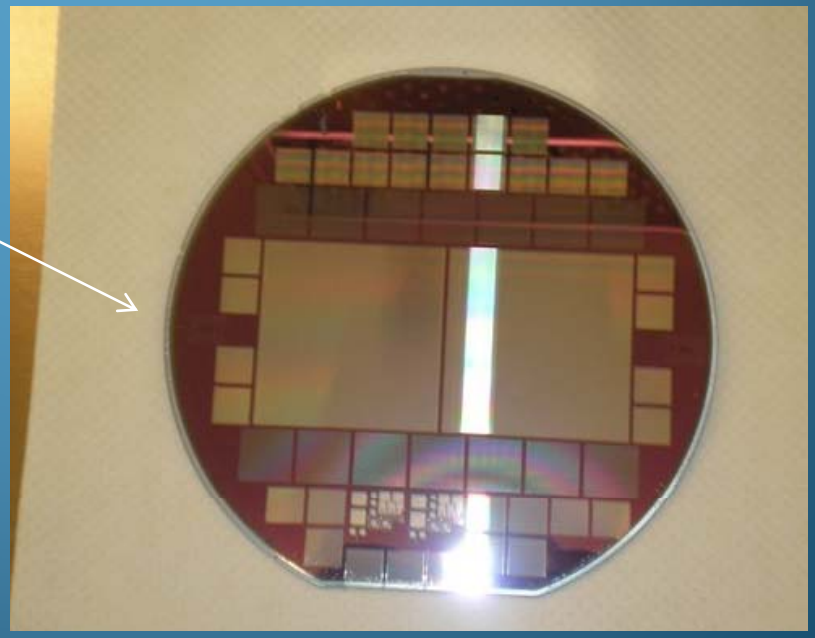
Other SITRA/SiLC activities

(not included in EUDET but necessary for successful EUDET accomplishment)

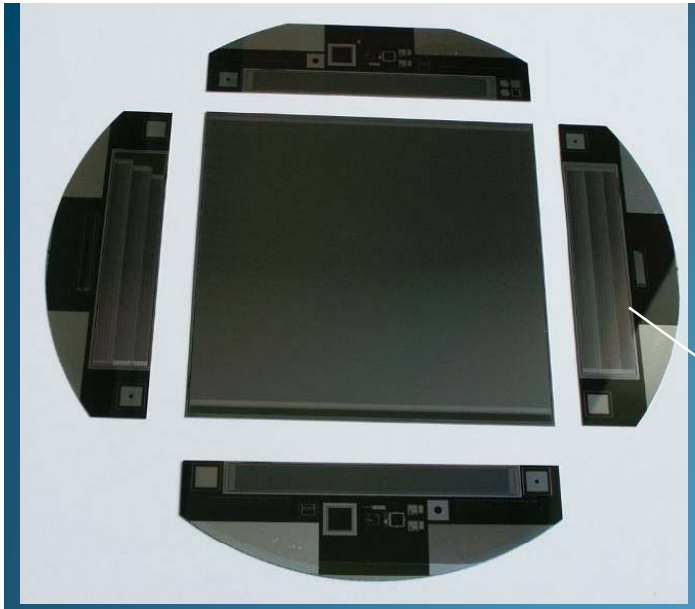
- Si sensor development, production and testing
- Module construction (engineering, tooling)
- DAQ (FPGA, off-detector, TLU/EUDET integration)
- Lab and beam tests
- Simulations

Si-sensors

- Dedicated SiLC strip sensors designed by HEPHY and manufactured by HPK
- Test structures already tested in the beam test (June 2008, CERN)
- Full-sized sensors with alignment treatment will be tested at CERN in October
- VTT 3D structures

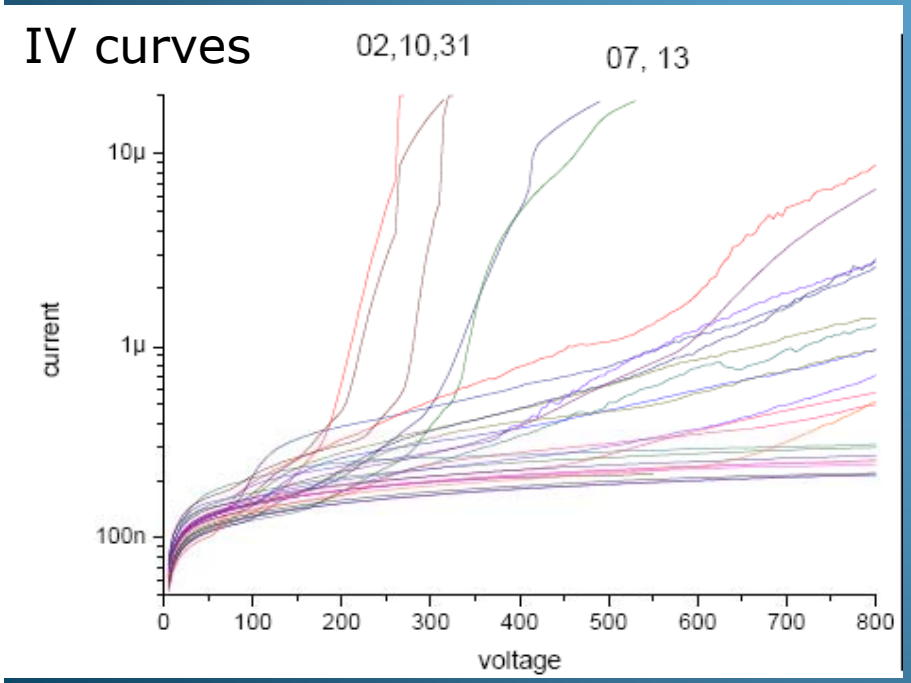


HPK strip sensors



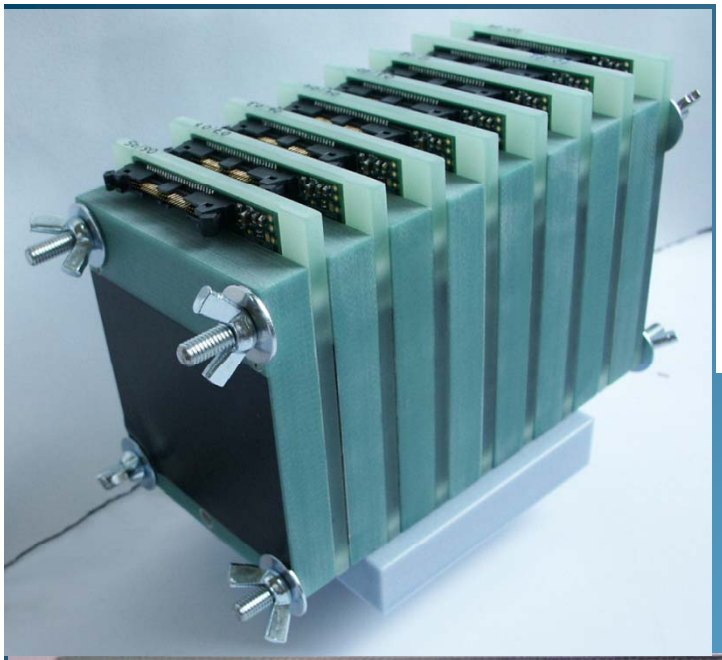
See P. Kvasnicka's talk at JRA2-SiTRA
Th. Bergauer's talk at JRA1

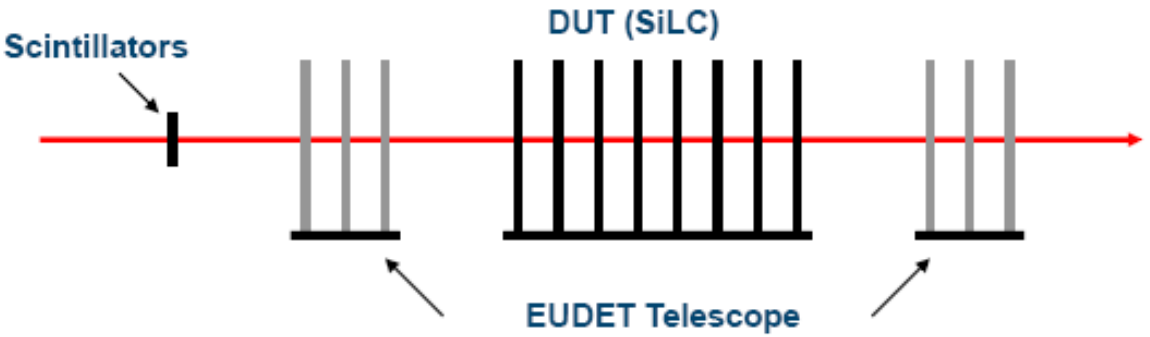
IV curves



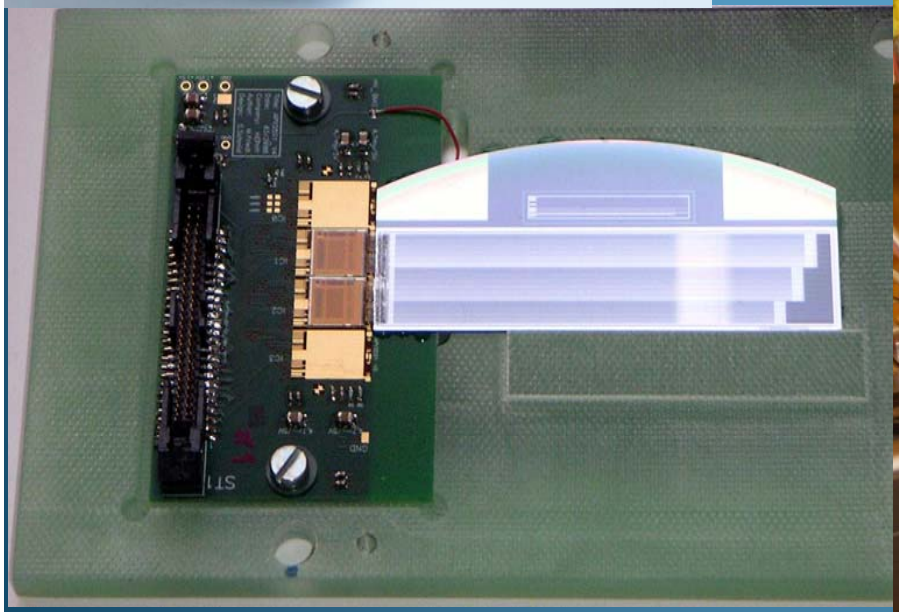
TESTAC:

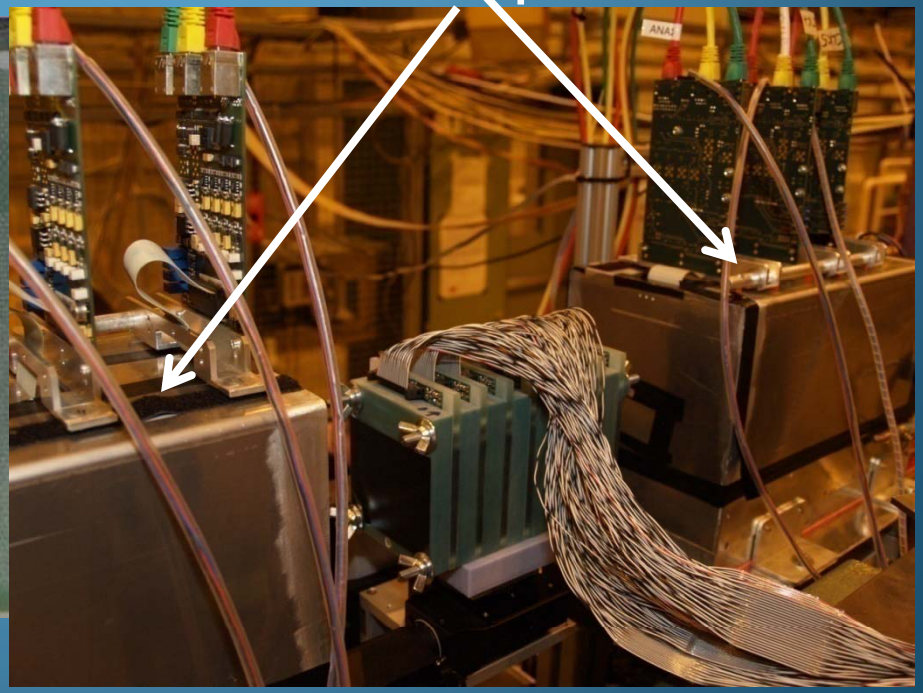
strip width [µm]	intermediate strips
5	no
10	no
12.5	no
15	no
20	no
25	no
5	single
7.5	single
10	single
12.5	single
15	single
17.5	single
5	double
7.5	double
10	double
12.5	double





DUT of HPK test structures
Combined beam test with EUDET telescope at CERN

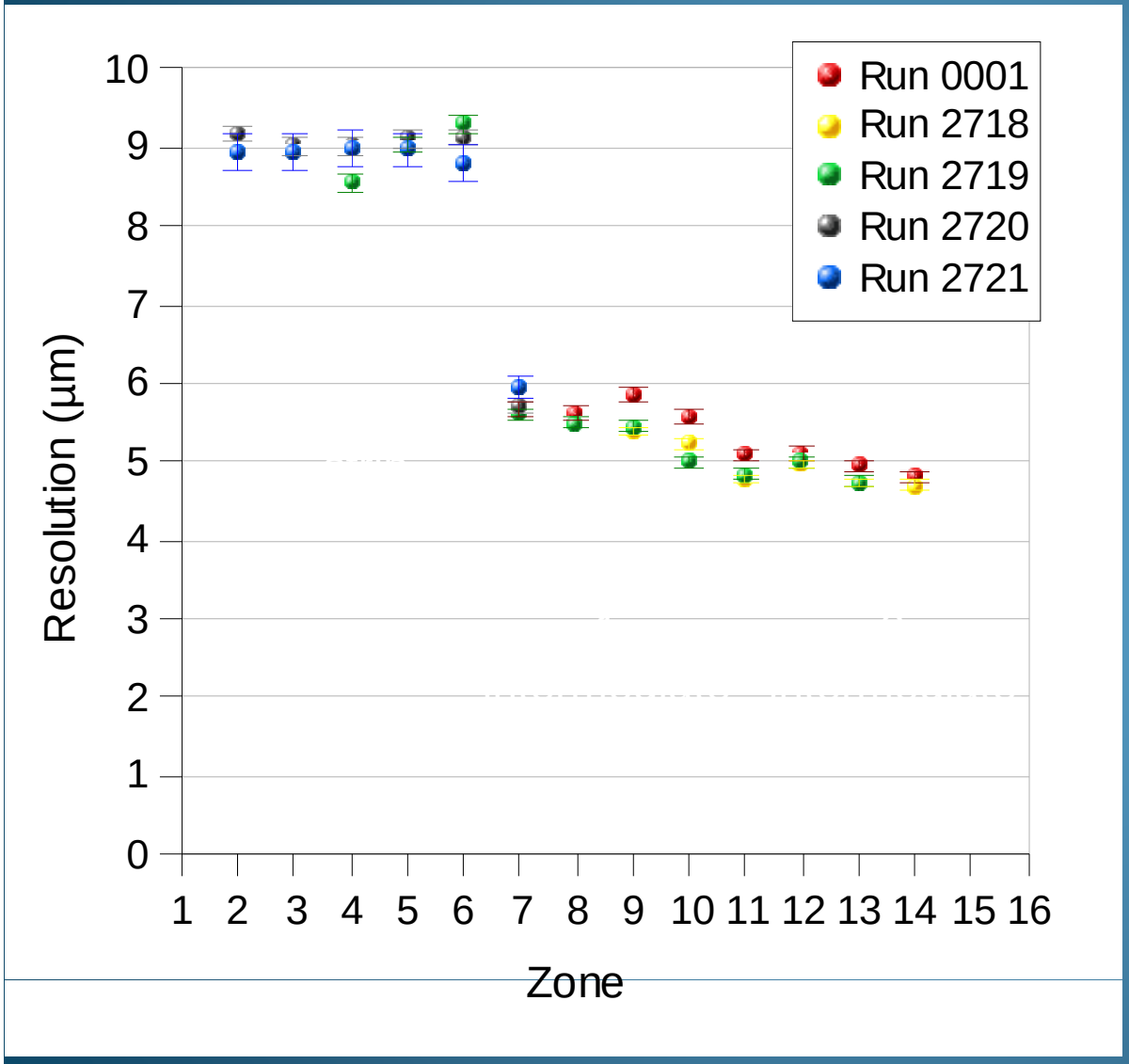




Goal: Resolution studies on Si strip sensors with fine pitch

See Th. Bergauer's talk at JRA1

Spatial resolution vs. strip geometry



50 µm r/o pitch strip

Interesting result:
9µm resolution if no intermediate strip

5 or 6µm resolution if 1 or 2 intermediate strip

Beam tests

- 2008 (CERN):
  - June: Hamamatsu test structures combined JRA1
  - End Oct: HPK alignment prototype + new DUT DAQ infrastructure available for this test and the ones in 09-10
- 2008 (DESY):

  Installation of a SET prototype for the LPTPC t.b.
- 2009
  - April: DESY, FE chip+HPK sensors (combined t.b. with EUDET telescope)
  - DESY: Pursuing LPTPC combined test beam and including chips version 2.
  - Later: CERN (HE beam)
  - Later: FNAL (combined)

Conclusions

- Past deliverables: all completed
- 4 M36 deliverables:
  - 2 mostly complete
  - Other 2: SITRA working with full speed towards completion, ready M43.
  - Alignment prototype ready M43.
  - Full Silicon tracking infrastructure test beam available for users M43.