JRA2-SiTPC Task Summary

Towards a Digital TPC for the LC

Paul Colas

DIGITAL TPC : The Ultimate Resolution

Idea: drift individual electrons under very low diffusion conditions (B=4T, Ar CF_4 Isobutane: σ = 20 μ /sqrt(cm)). Consistent with cluster size at 1m.

Then detect single electrons with a high efficiency and get their position and arrival time precisely with microscopic pads.

Get also dE/dx from cluster counting, and get rid of δ-rays. This is equivalent to, but more precise than, usual truncated mean.

This is made possible by the TimePix chip designed by JRA2-SiTPC.

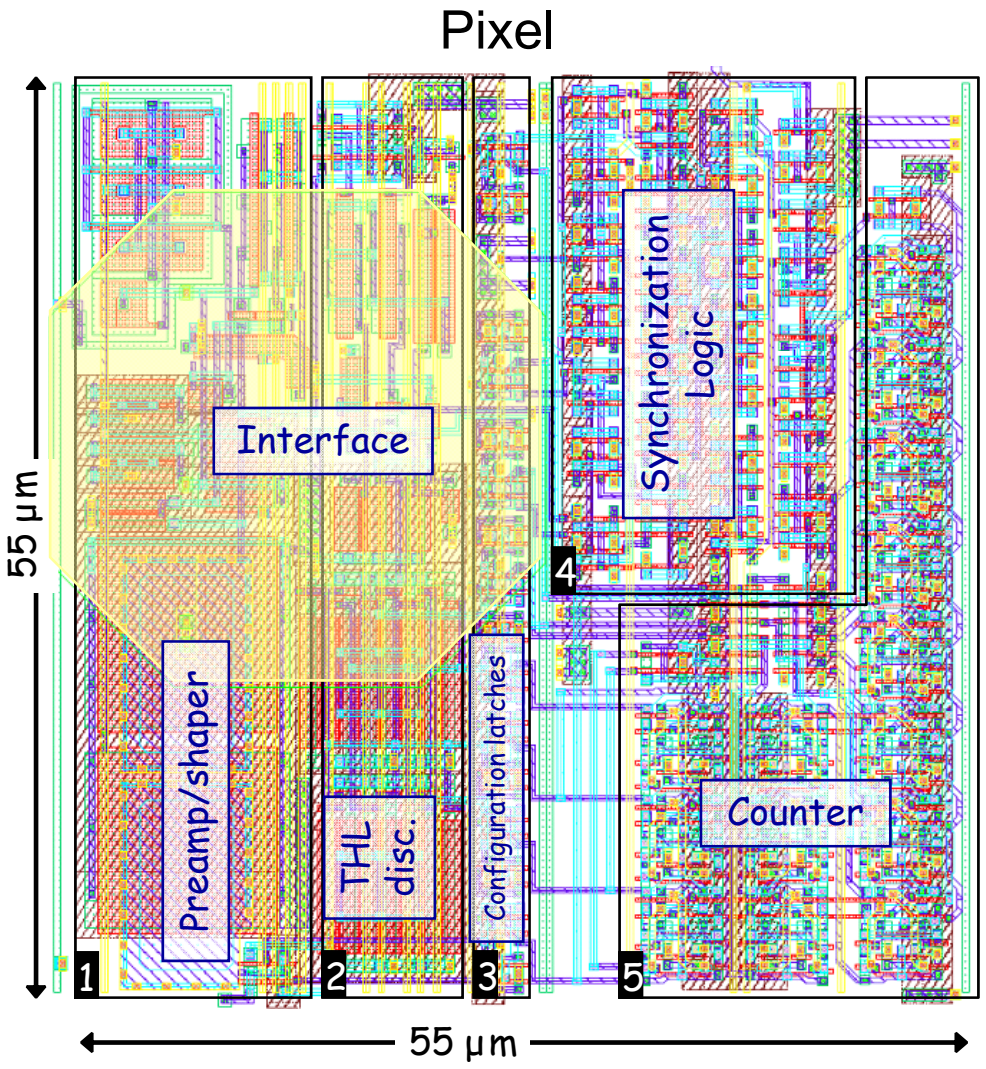
TimePix chip

Idea : take a medical imaging chip (Medipix 2), add a clock to each pixel, replace ‘grey levels’ by ‘clock ticks’

(Michael Campbell, Xavi Lloppart, CERN)

This was the first deliverable, end 2006

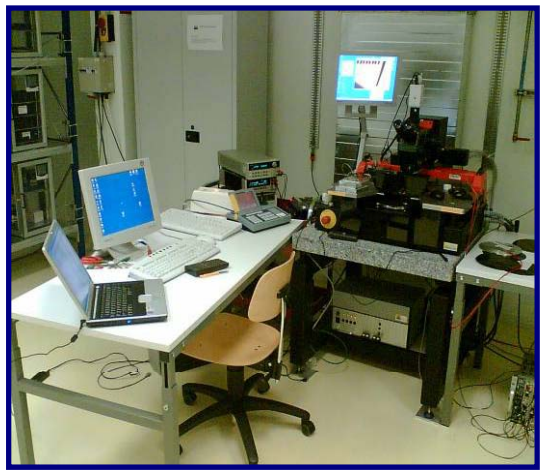
65000 pixels, 14-bit counter, 100 MHz tunable clock frequency -> more voxels than the ALEPH TPC, but tiny!

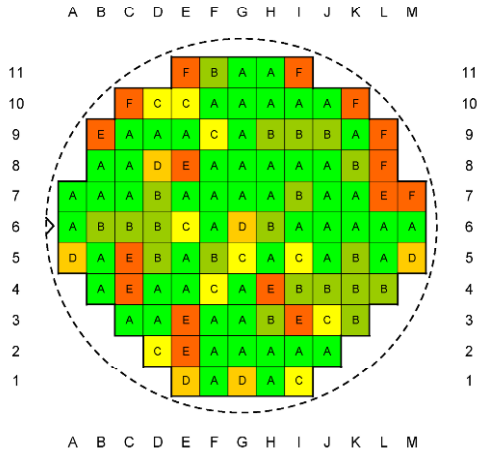


Wafer production and test:

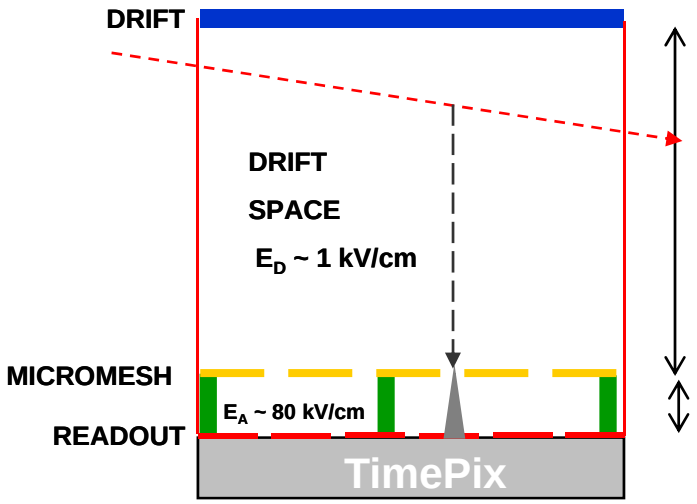
Extra 12 from 1st batch

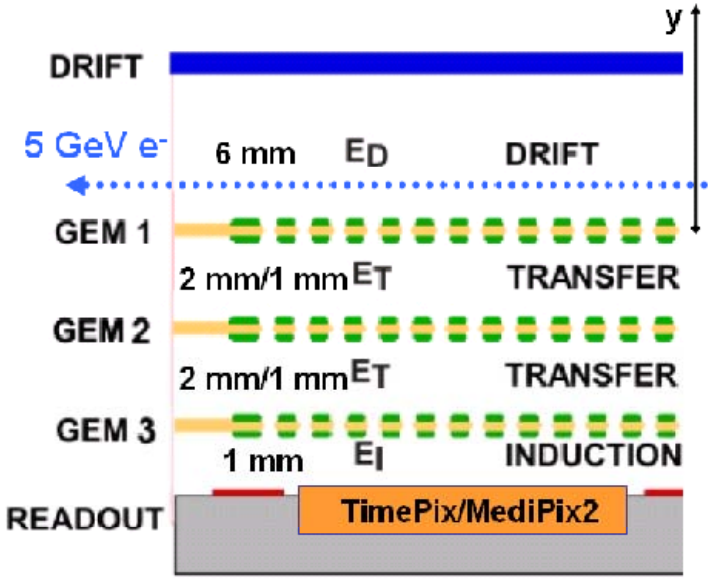
Second production : 38 wafers (105 chips, yield about 80%)

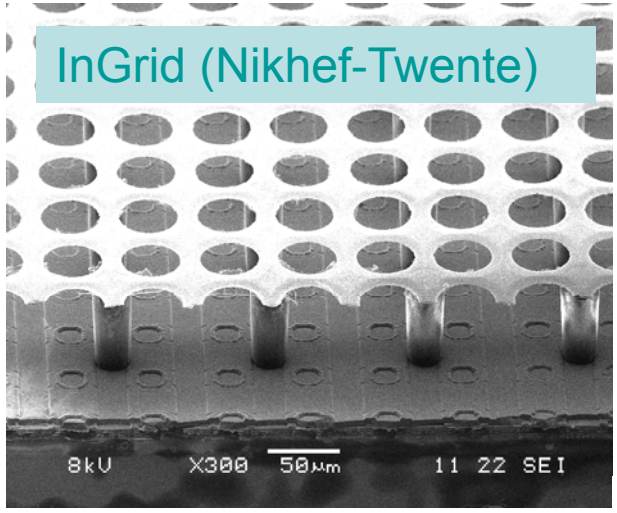


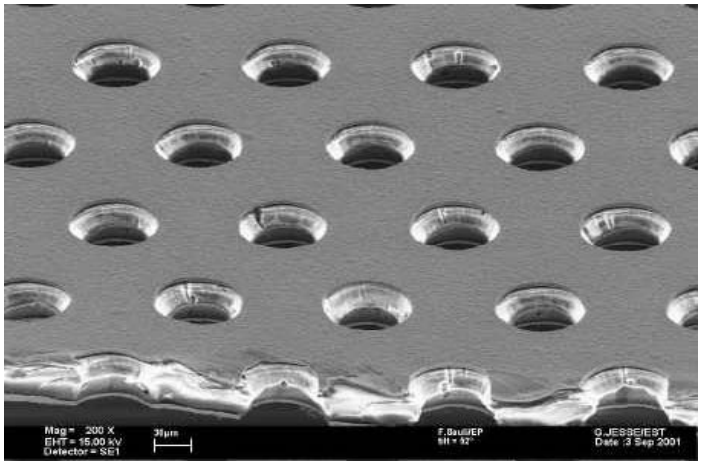


Micromegas and GEM









BONN
Hubert Blank, Christoph Brezina, Klaus Desch, Jochen Kaminski, **Martin Killenberg**, Thorsten Krautscheid, Walter Ockenfels, Martin Ummenhofer, Peter Wienemann, Simone Zimmermann

FREIBURG
Andreas Bamberger, **Uwe Renz**, Andreas Zwerger

NIKHEF+TWENTE
Victor M. BlancoCarballo, Yevgen Bilevych, Maximilien Chefdeville, Martin Fransen, Fred Hartjes, Lucie de Nooij, Joop Rovekamp, Jurriaan Schmitz, Jan Timmermans, Harry van der Graaf, Jan Vischers

SACLAY
David Attié, Paul Colas, Xavier Coppolani, Eric Delagnes, Arnaud Giganon, Ioannis Giomataris

The 4 institutes gave a report (speaker in red)

TimePix was operational end of 2006

First (stable) mips were observed in October 2007 both in GEMs and Micromegas (thanks to SiProt for the latter)

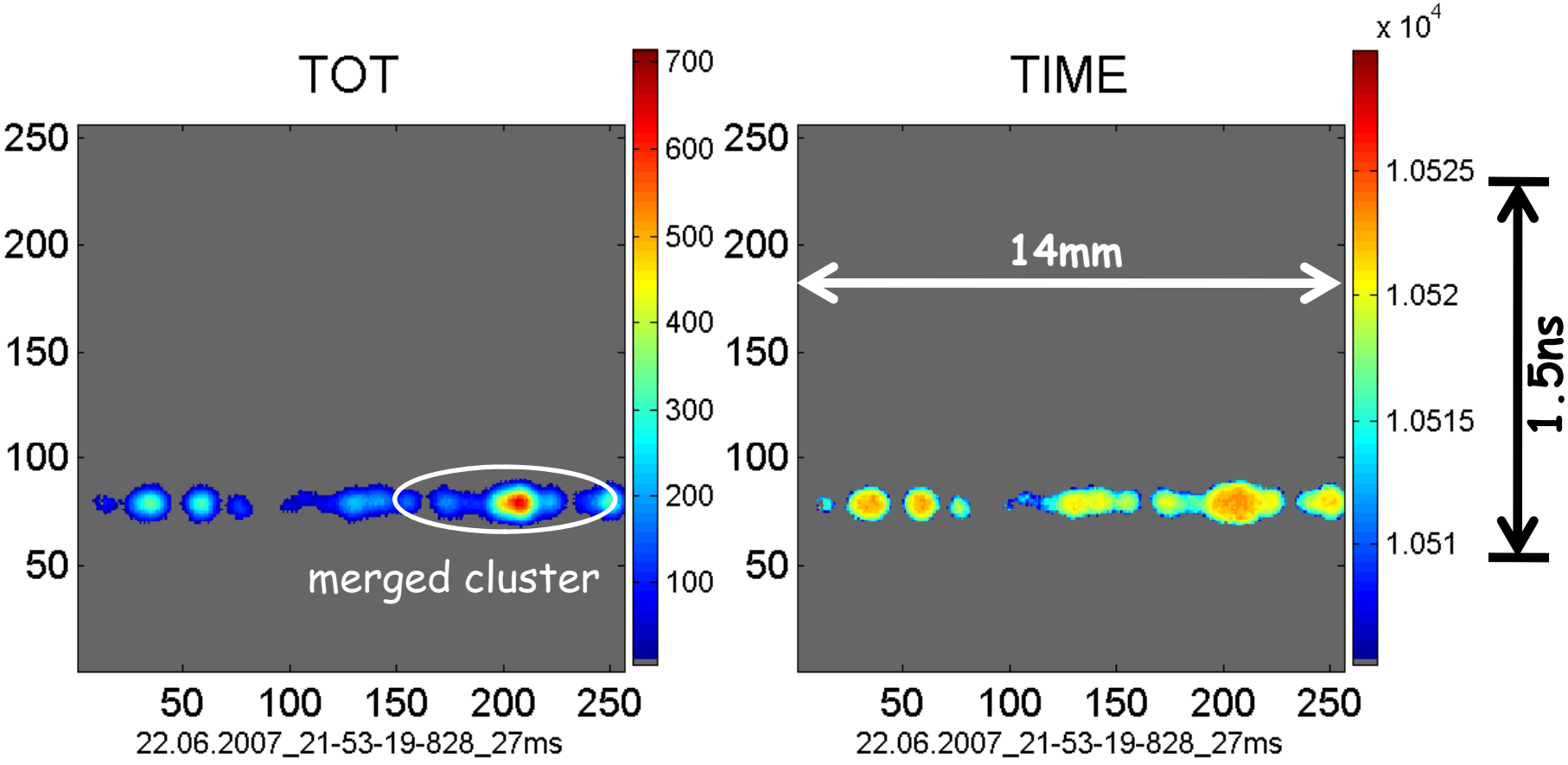
Endplate infrastructure (8-chip panel) was delivered in March

SiTPC infrastructure should be ready for operation end of 2008

Milestones:

Milestone	Date	Task	
Preamplifier prototype board ready	12	A	
			Deliverable
Field cage available	18	A	
Convection cooling system prototype ready	18	C	
DAQ prototype available	24	A	
			Deliverable
Motorized 3D table ready	24	C	
FE chip version 1	24	C	
Central tracker prototype	24	C	
			Deliverable
Conduction cooling system prototype ready	36	C	
FE chip version 2	36	C	
Forward tracker prototype	36	C	
Silicon tracking infrastructure available	36	C	
Prototype compact readout system ready	48	A	
Final report	48	A,B,C	

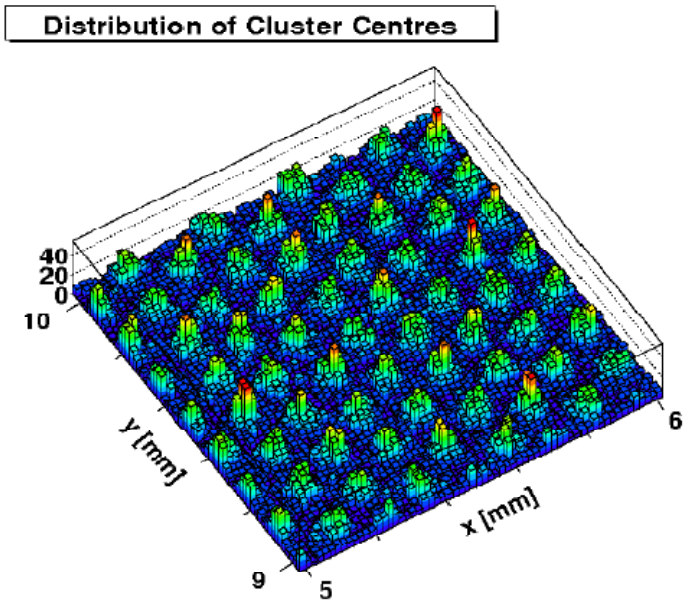
There is a lot to do with single chips

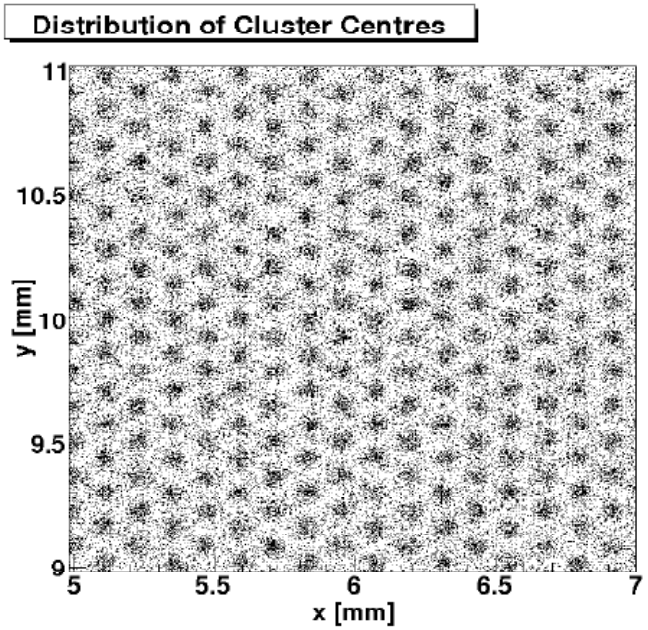


See tracks and resolve merged clusters

GEM structure measured in Bonn

- Dedicated high statistics run with ^{90}Sr source untriggered, no z information available
- Long drift distance ≈25 cm
- GEM spacing: 1 mm transfer gaps and induction gap

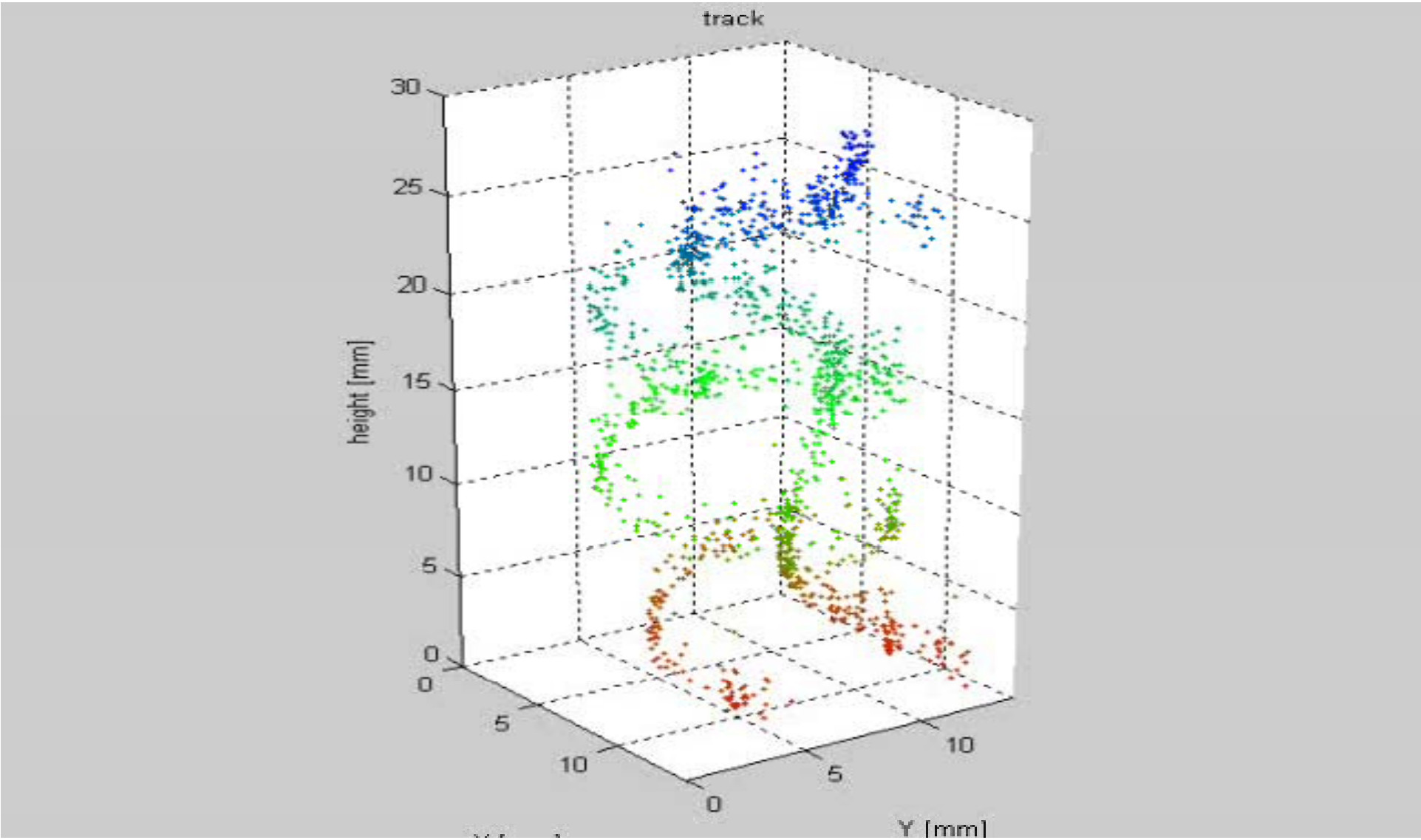




We can see every single GEM hole!

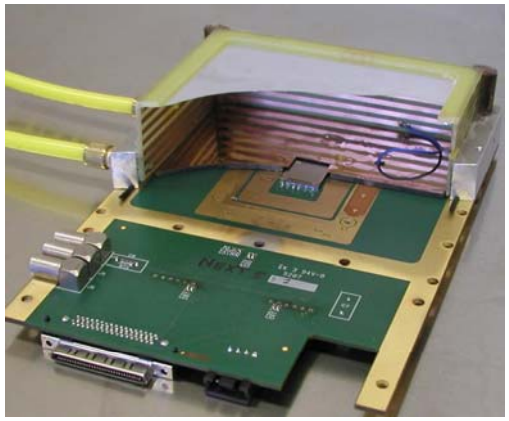
universitätbonn

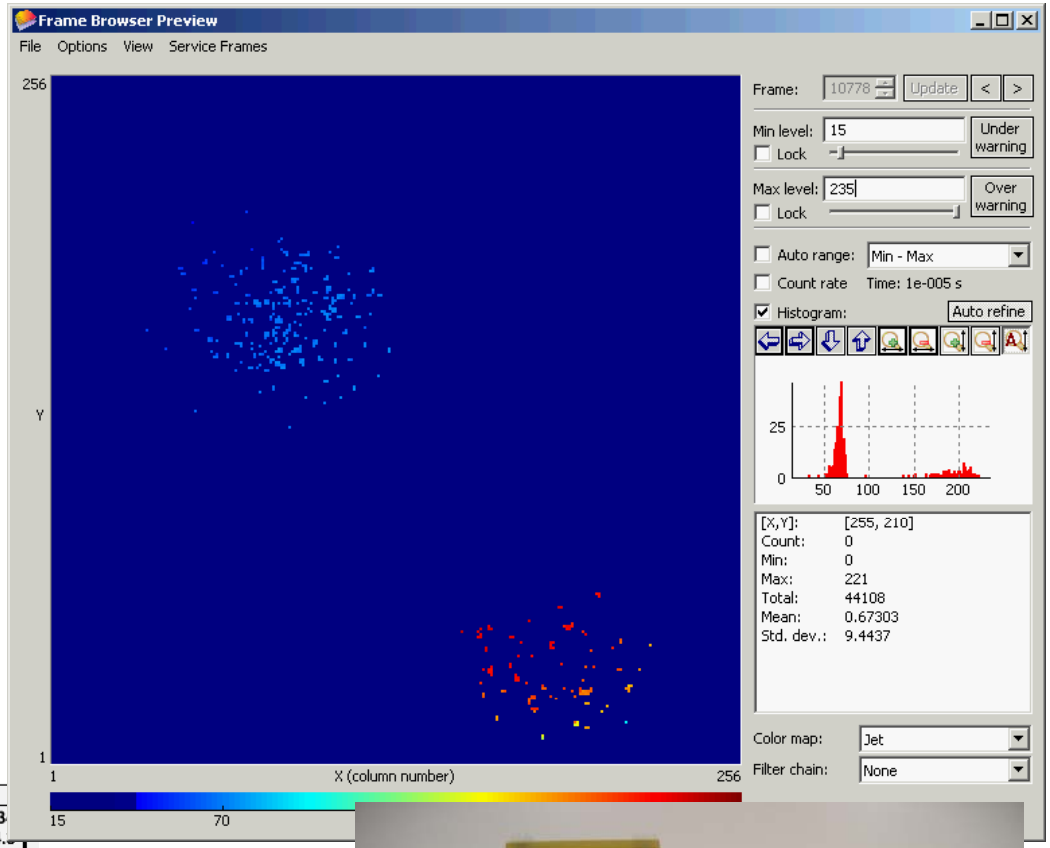
See beautiful 3D tracks in a magnetic field

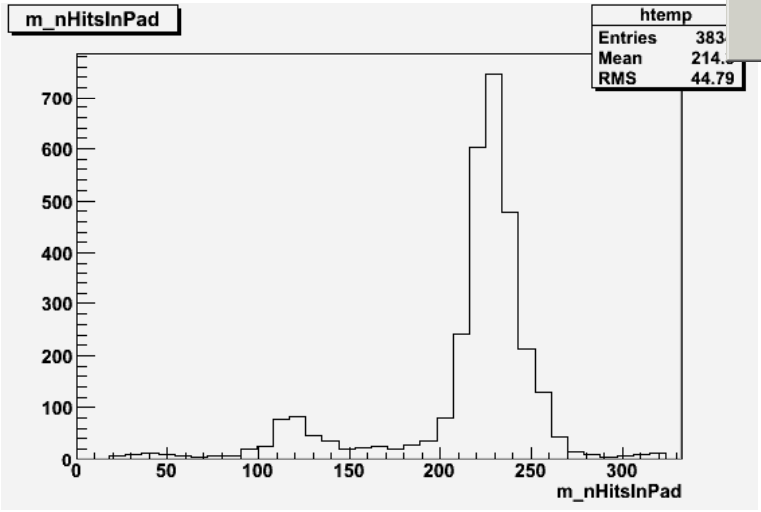


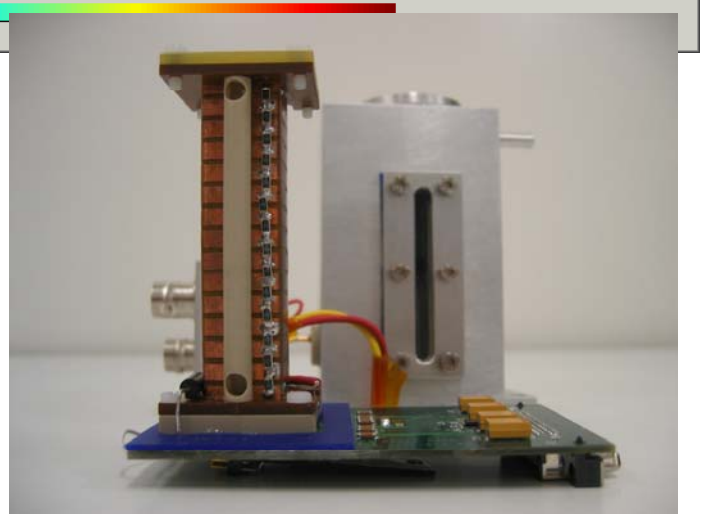
See electrons from an X-ray conversion one by one and count them, study their fluctuations

(Nikhef-Saclay)

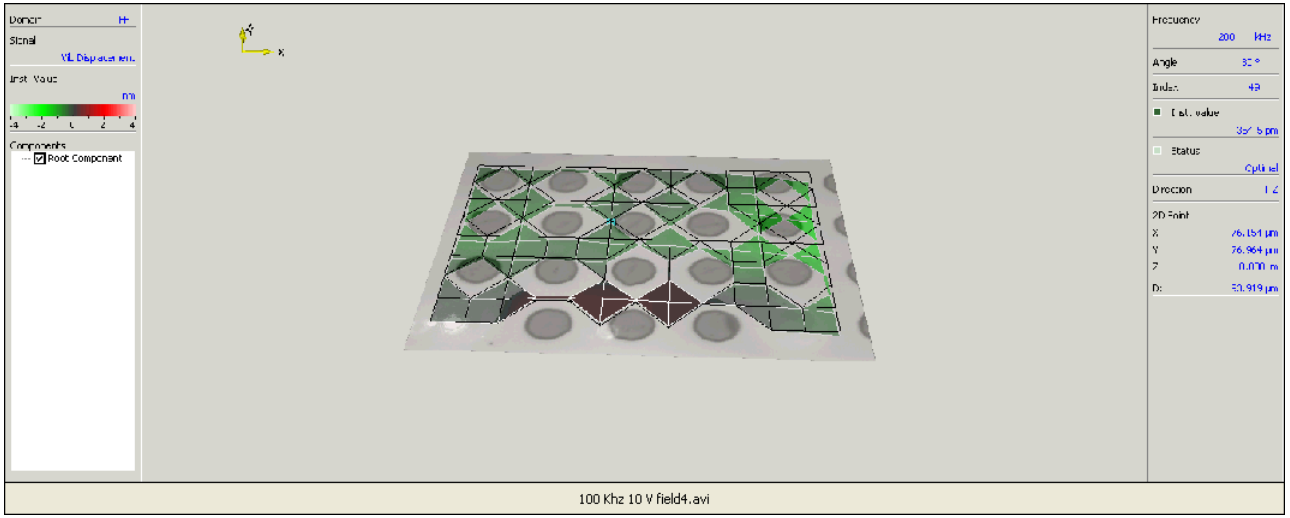








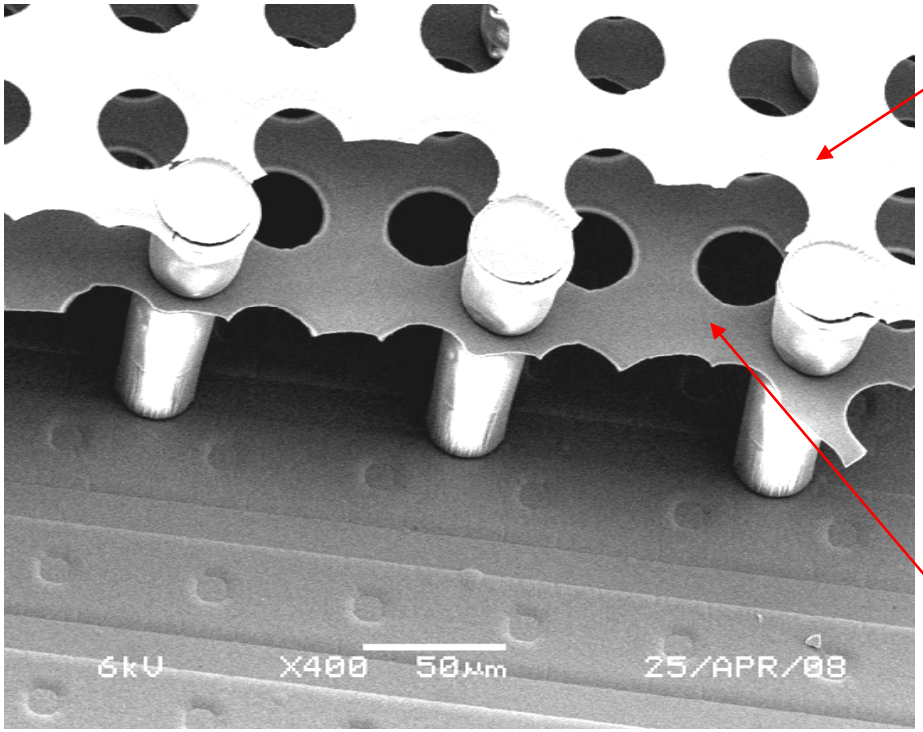
Study mesh vibrations and robustness



Twingrid operated for first time

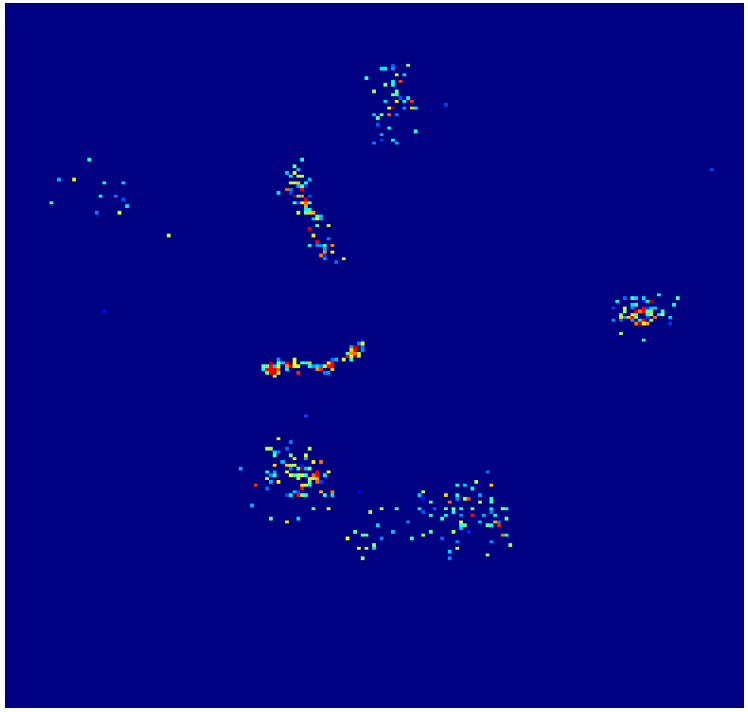
- Double structure on a chip seems feasible
- No protection layer
- Chip survived ~5hours, protection layer needs to be added on next devices

Nikhef-Twente



450V

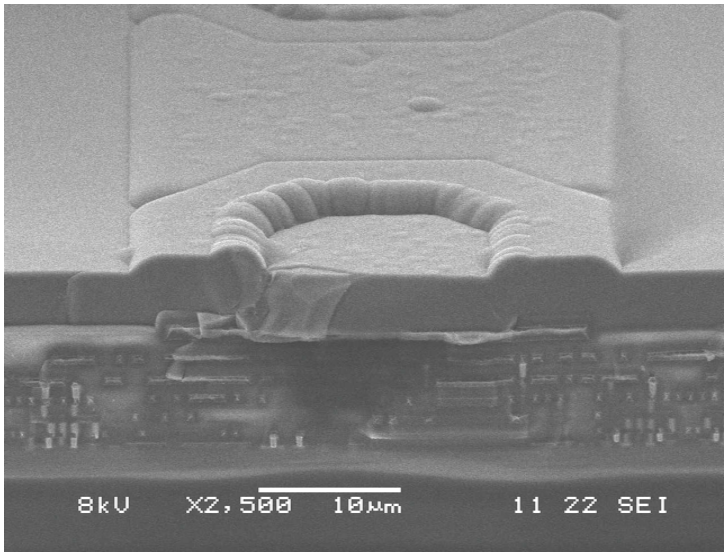
100V



SiRN:New anti-spark material

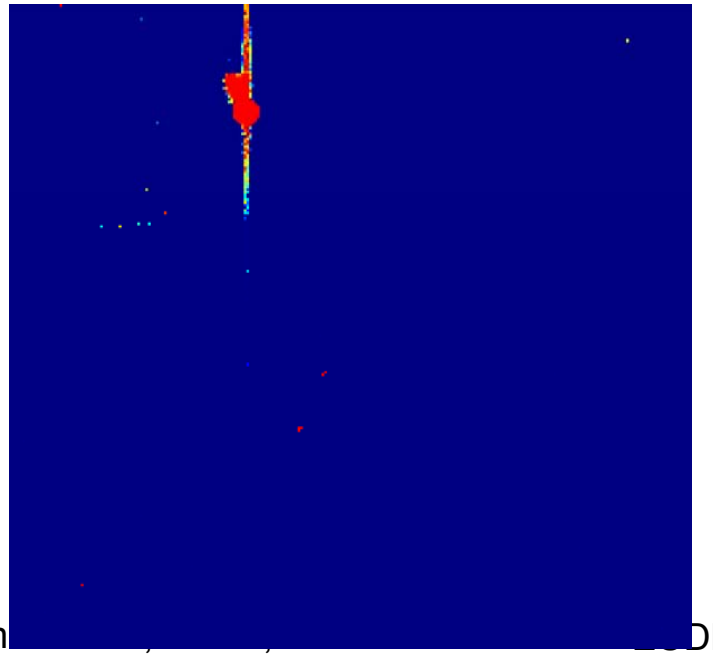
- Si_3N_4 typical anti-scratch layer on CMOS
- Si-RichN, excess of Si makes it high resistive
- Deposited by PECVD at 300 °C or lower
- Any lab can do it !!

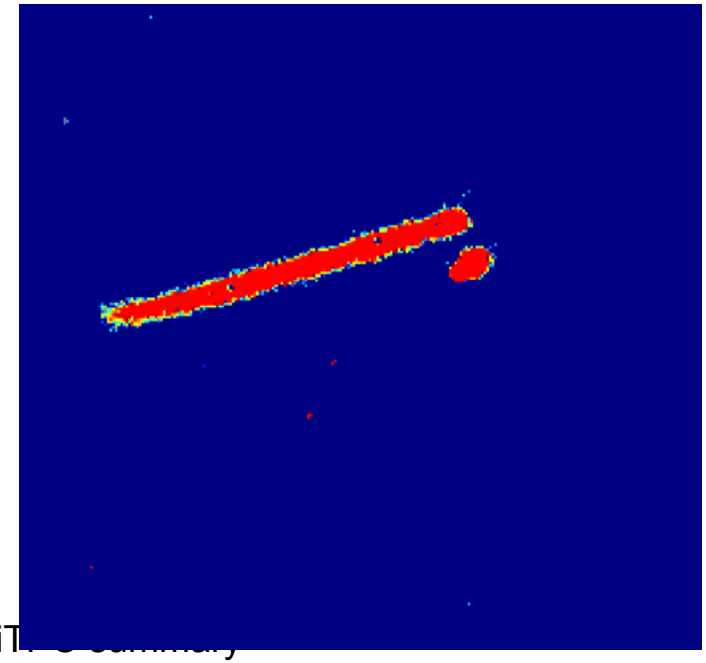
Nikhef-Twente



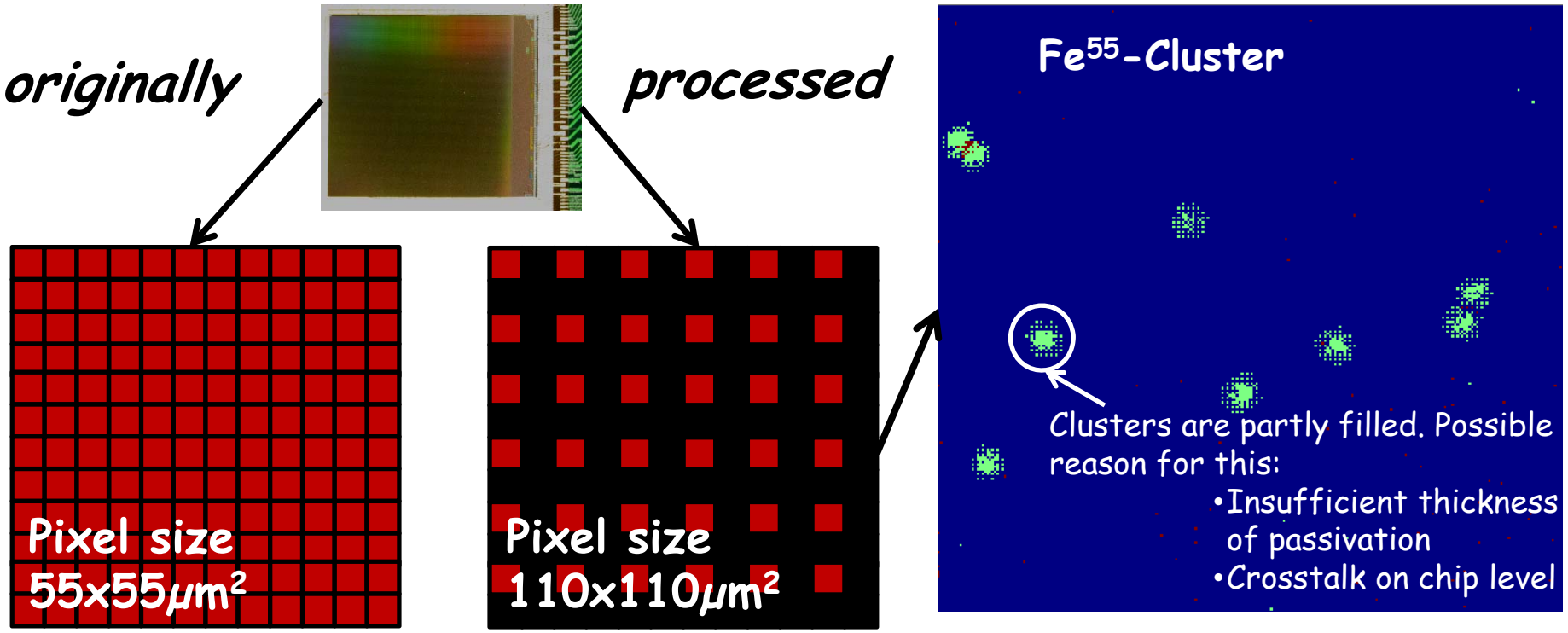
And it can withstand sparks

- Timepix covered with 7,2 μm SiRN
- Micromegas on top
- Ar/Iso 80/20, 520V on the grid and the chip does not want to die





Chip Post-Processing



Pixel active

Pixel passivated

- Work on technologies for post processing chips
- Optimization of readout granularity

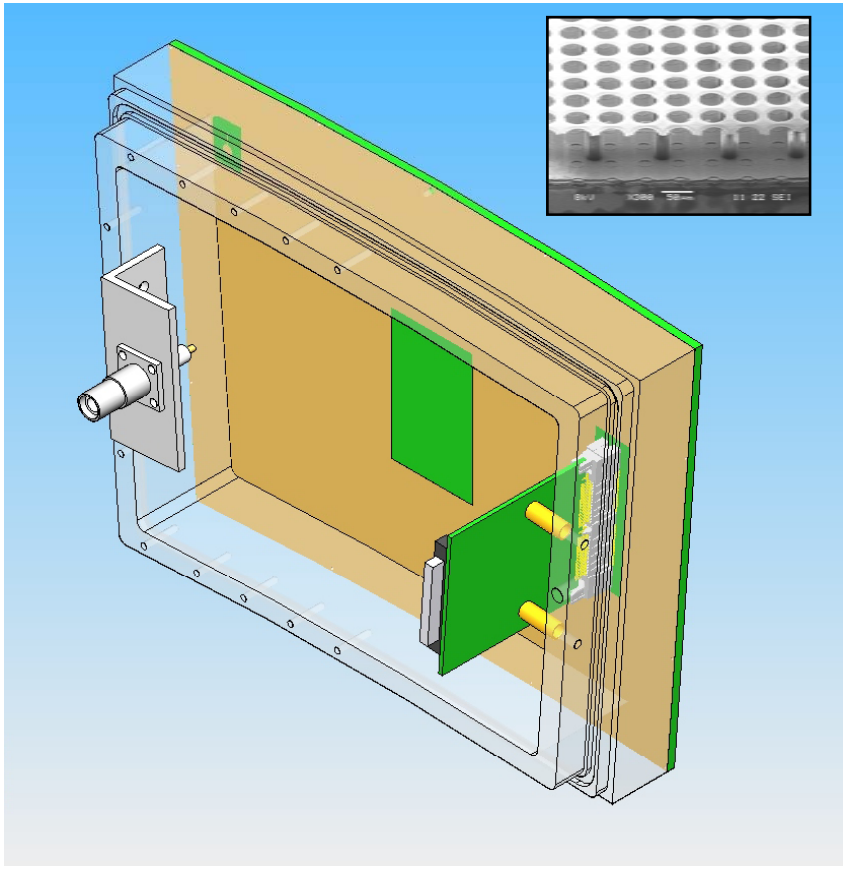
Deliverable for this year: endplate infrastructure (scheduled end of 2007, delivered March 2007

Large Prototype Endplate: voluntary contribution from Cornell

Next deliverable: SiTPC endplate

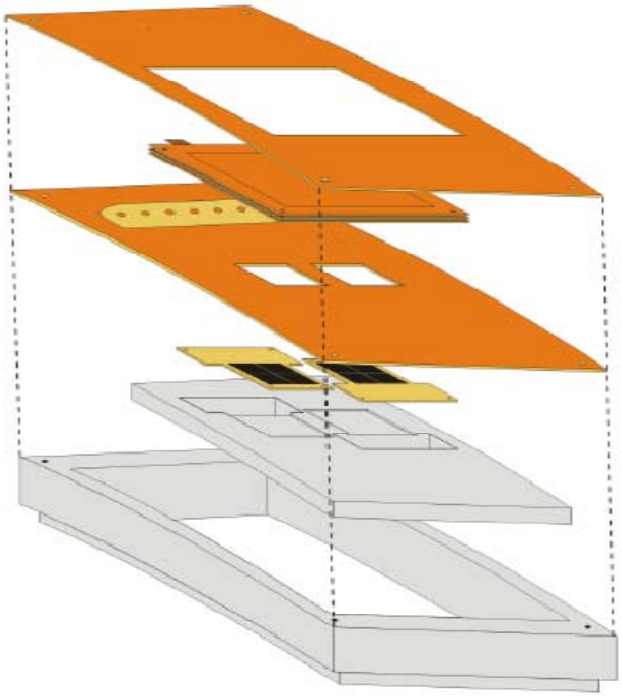
Micromegas (InGrid)

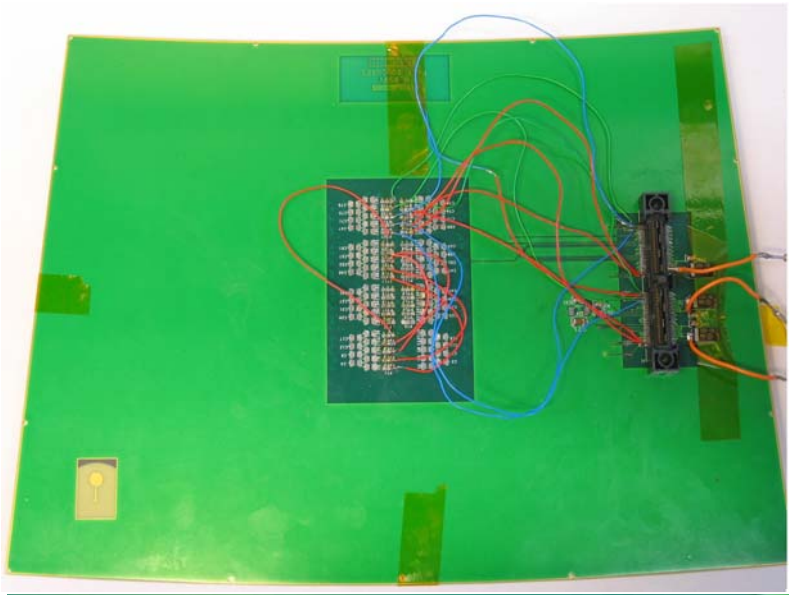
Saclay and Nikhef-Twente

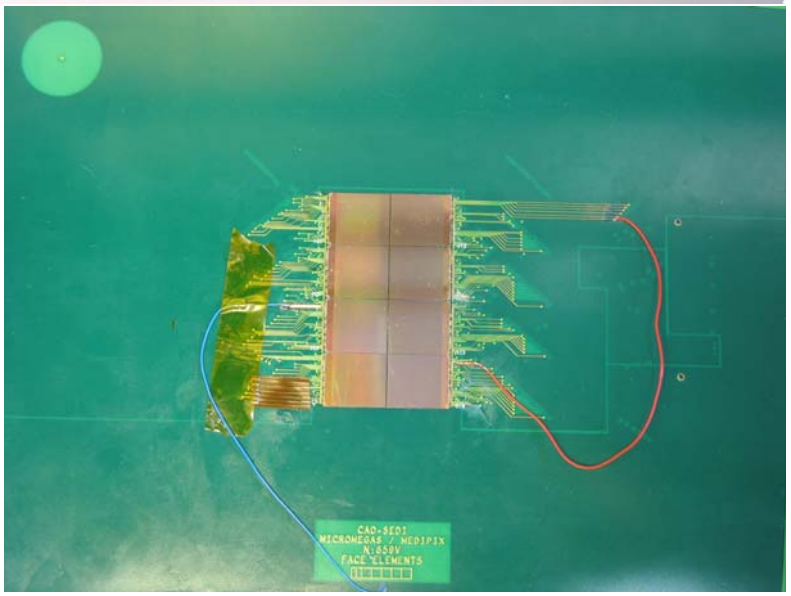


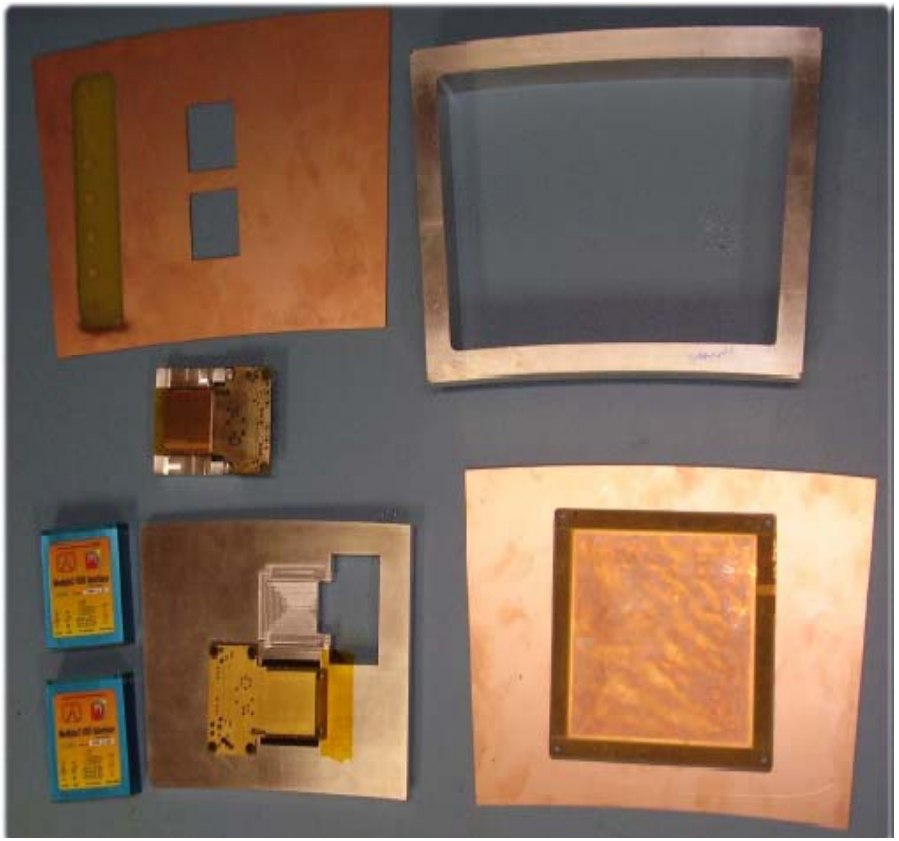
GEM

Bonn and Freiburg







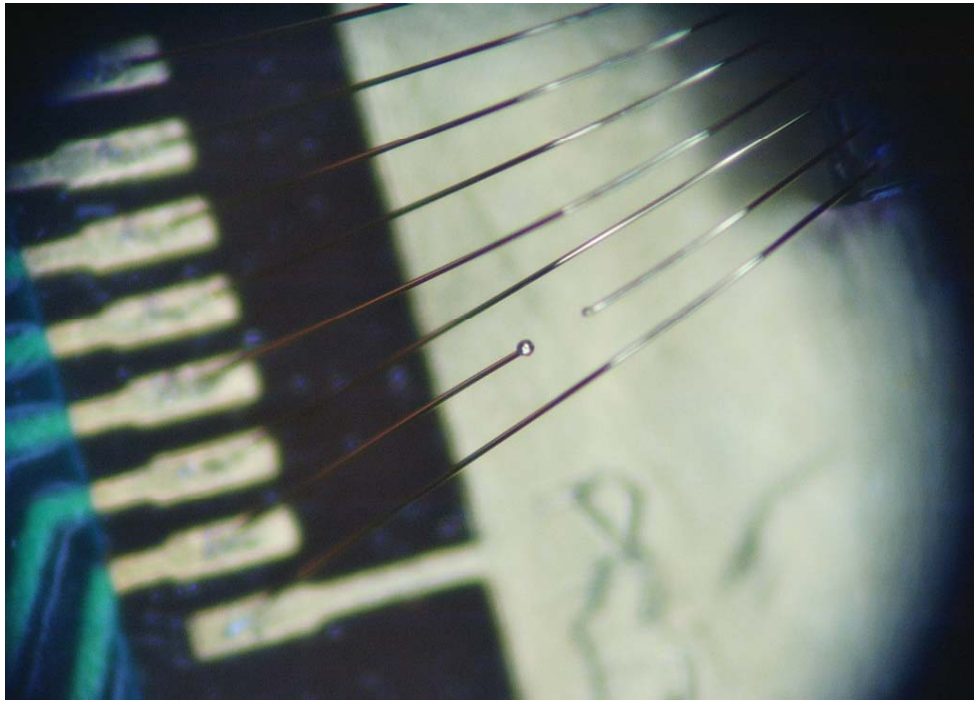


But there are difficulties:

Power consumption 1.2 A -> requires an additional supply

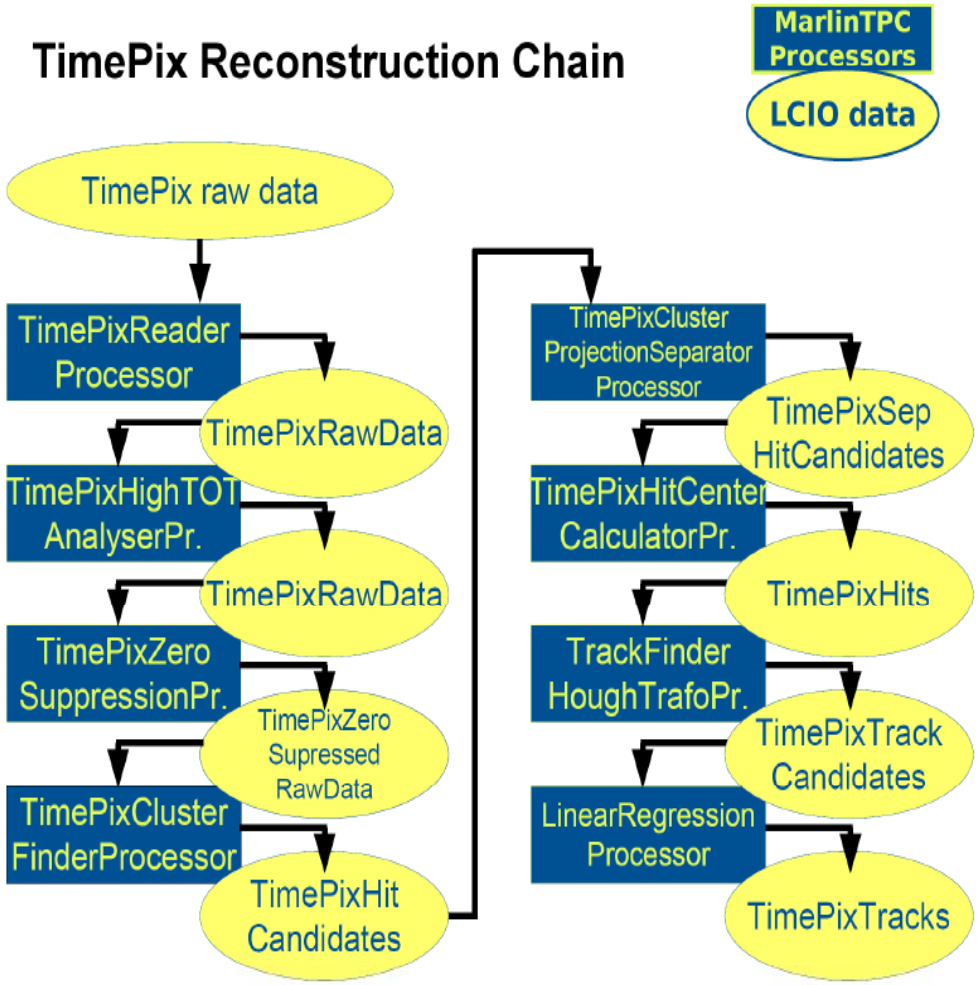
Serial readout : need to be able to go through a dead chip

Incidents to be understood : melted wires, broken chips?



SOFTWARE DEVELOPMENT

- Development of Pixelman (plug-in's)
- TimePix in the Marlin analysis framework
- Evolve to multi-chip capabilities



CONCLUSION

- A lot is being done with single chips: post-processing, new structures, basic studies…
- But the real game is to go for more and more chips: already with 4 or 8 chips, many difficulties are encountered, but will be solved hopefully in the coming months.
- For a real full scale, new concepts are necessary (self-triggering, on-chip processing, inter-chip communication, 3D technology). This is not in the EUDET contract, maybe FP7, 8…?