Status Report TPC Task

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DESY

EUDET Annual Meeting 2008
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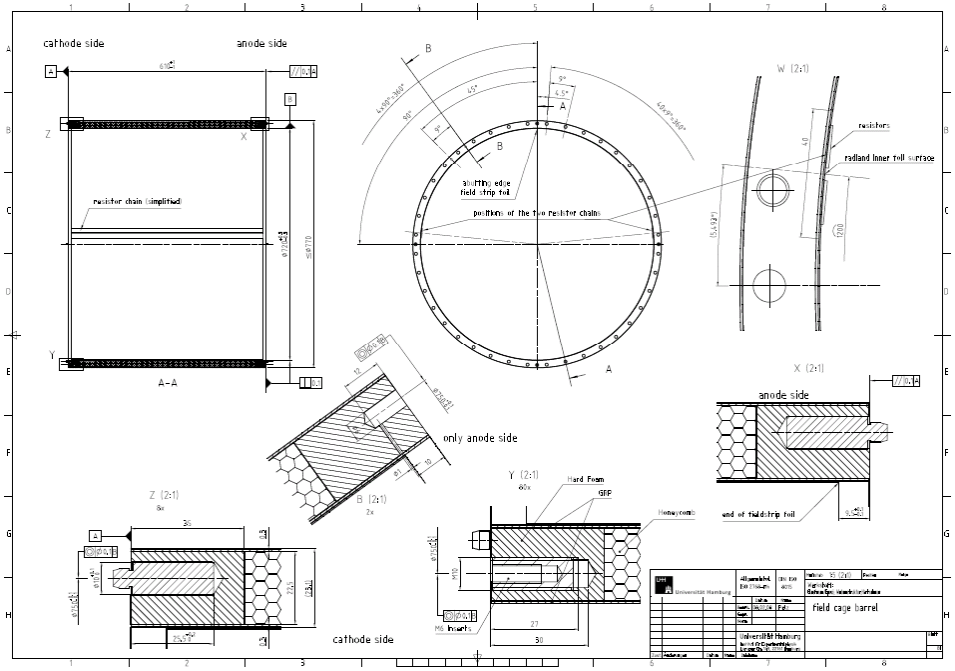
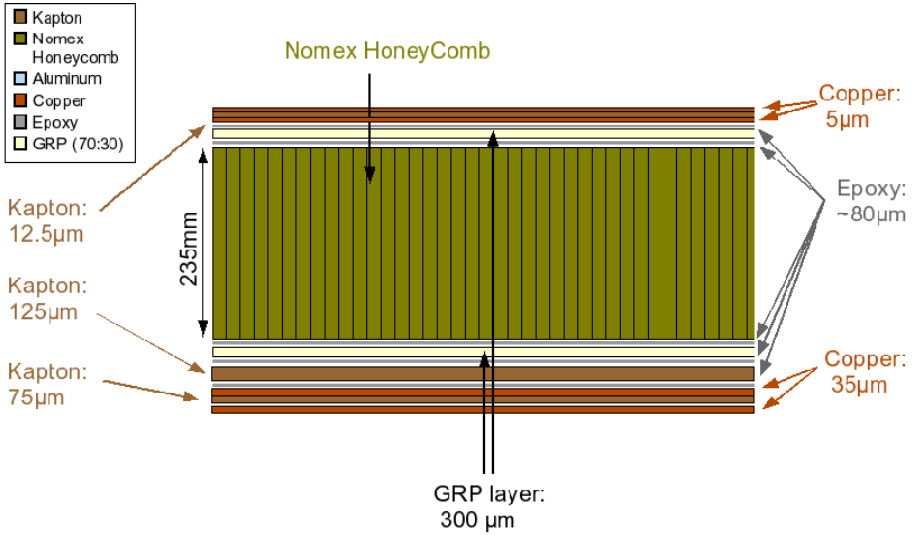
TPC Task

Comprises:

- Large Prototype TPC LP
  - Field Cage
  - DAQ & Monitoring, Gas/HV
  - Mechanics
- MicroMegas Module
- ALTRO Electronics
- TDC Electronics

LP Field Cage





Inner Diameter 720 mm, Outer diameter 770 mm
Wall thickness 25 mm
Length 610 mm

LP Field Cage

Survey results: specs seem to be within the tolerances

Parallelism Cathode/Anode: $\delta = 0.110 \pm 0.003\,\mathrm{mm}$

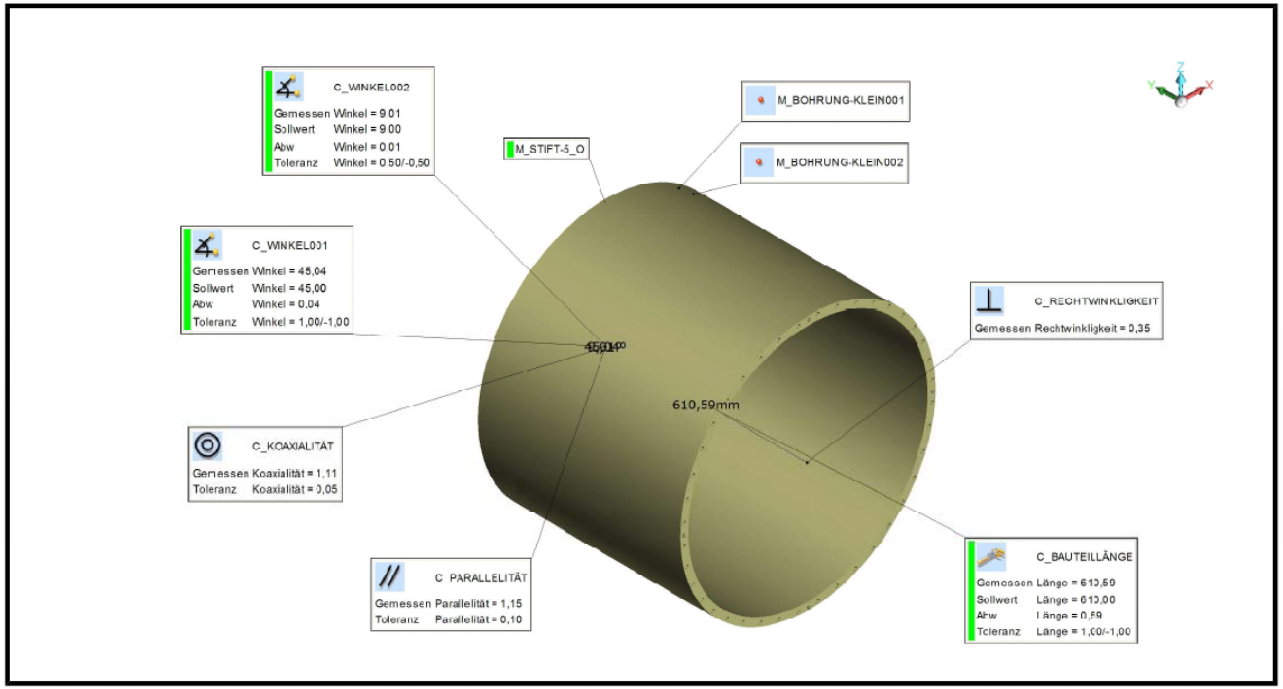
Peter Schade, DESY

Fieldstrip pitch:

$p = 2.78 \pm 0.10$ mm

Nominal:

$p = 2.80$ mm



LP Field Cage

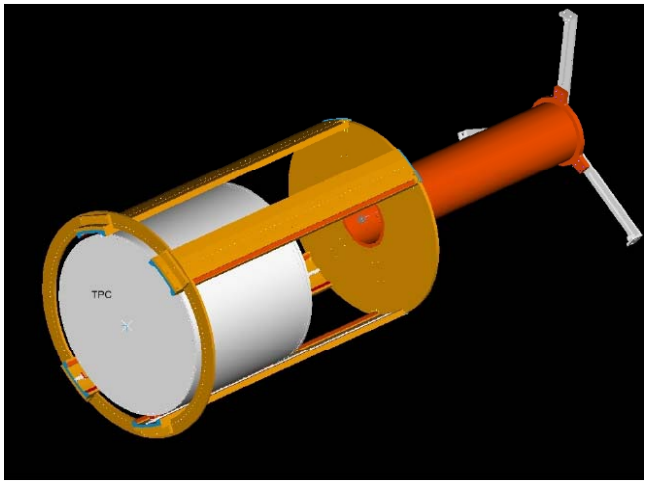
- Mount a few more resistors and HV connectors/contacts to outside
- Check all electrical connections of the field cage/strips, HV test
- Pressure test, leak test and gas purity test
- Endplate to be attached to the field cage

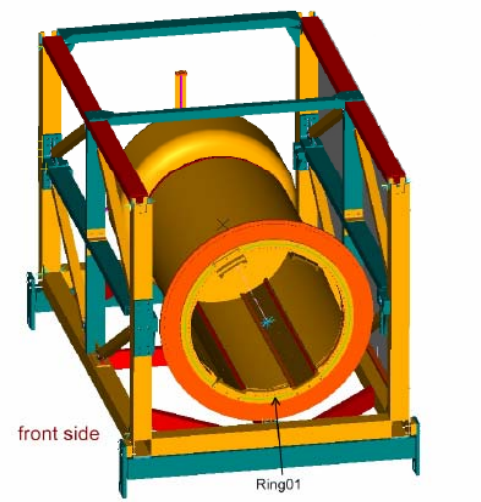
LP DAQ & Monitoring, Gas & HV

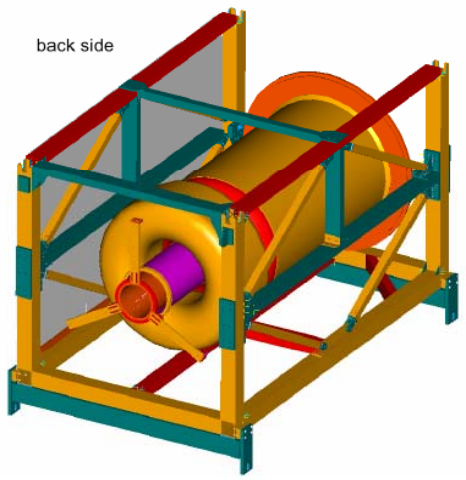
- Trigger Logic Unit (TLU) provided by University of Brussels
- Monitoring via DOOCS:

  Distributed Object Oriented Control System
- Basic gas system
- HV → Configuring, Controlling, Monitoring
  - CAEN (GEMs/MicroMegas/Termination plate)
  - FUG (Cathode)

LP Mechanics

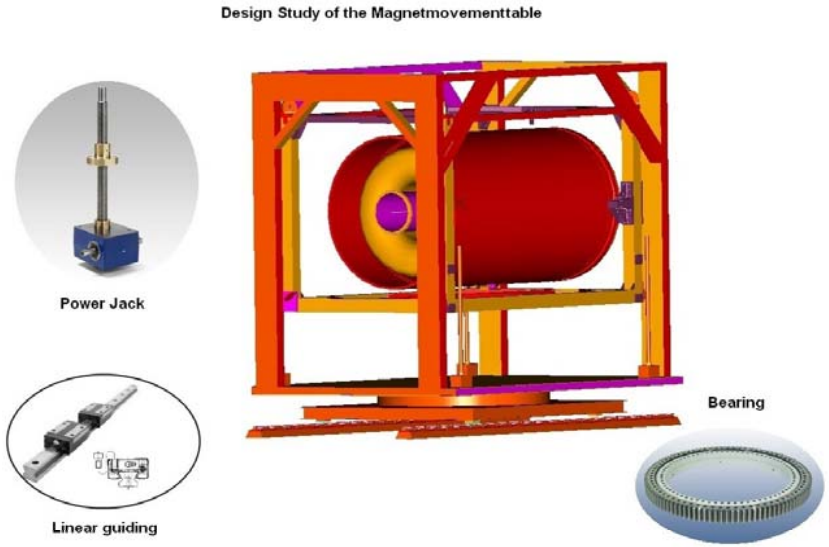






Support structures:

- TPC
- PCMAG



F. Hegner, V. Prahl, R. Volkenborn, DESY

LP Plans

Main components are available:

- TPC needs to be assembled
- Assembled TPC needs to be commissioned
- DAQ components are available
- Slow Control / HV / Gas system available
- Magnet / T24/1 available; final handover of PCMAG with KEK cryogenic experts this week
- TPC support structure: parts are already installed at PCMAG, rest is expected to arrive in mid/end October

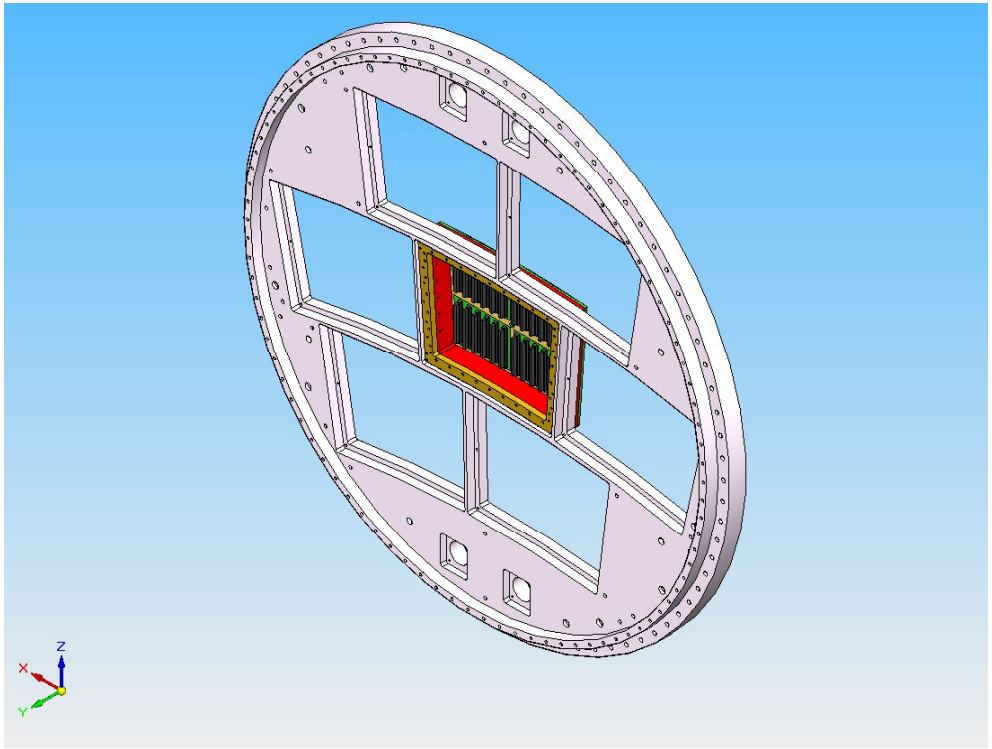
MicroMegas Modules

Panels: in 2008-2009: 1 panel at a time in the centre of the detector. Others are dummy. Also plans for trying a multichip InGrid+TimePix panel (see D. Attié's talk this morning)

PCBs have been produced

4 with the Saclay routing in 6 layers (delivered early June)

4 with the CERN routing with 4 layers (August)



P. Colas, Saclay

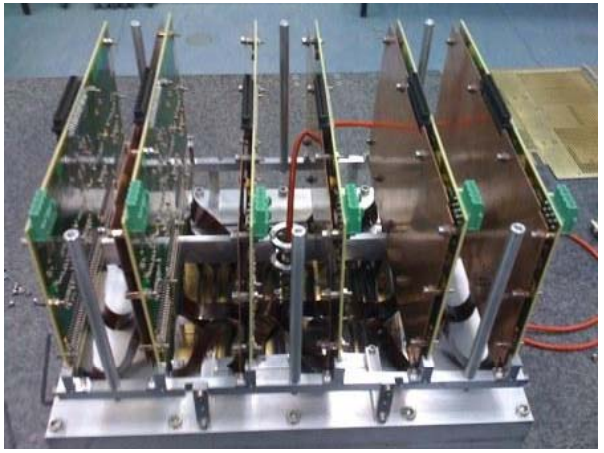
A first 'bulk Micromegas' panel (without resistive foil) and a second, with a resistive carbon-loaded kapton, have been produced at CERN,

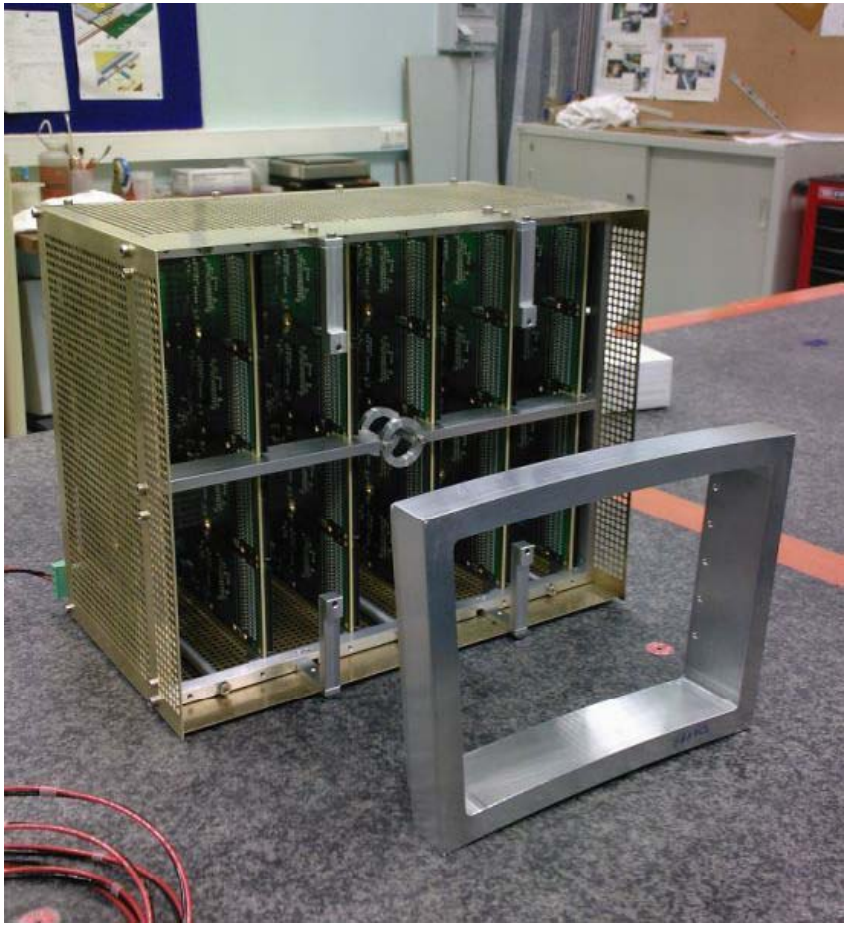
(Rui de Oliveira)

MicroMegas Modules

Shielding, Faraday cage, flat cables, gasbox…

P. Colas, Saclay





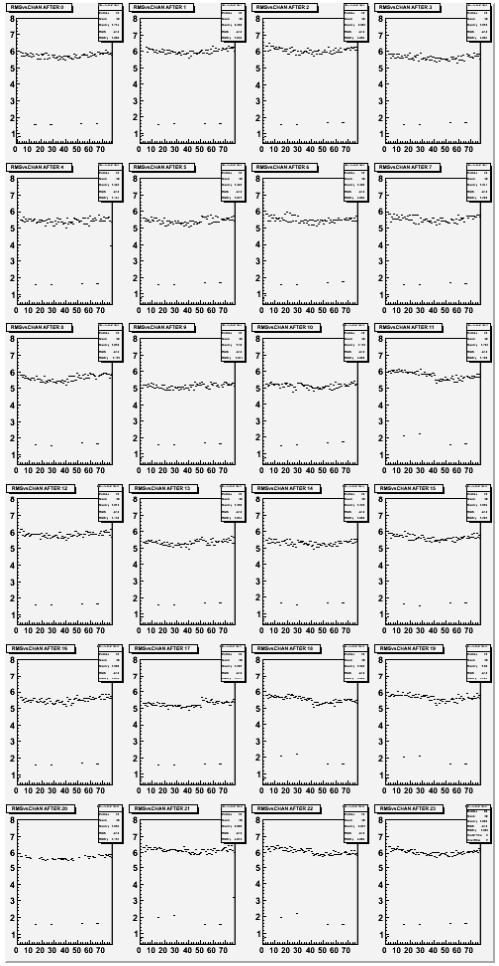
MicroMegas Modules

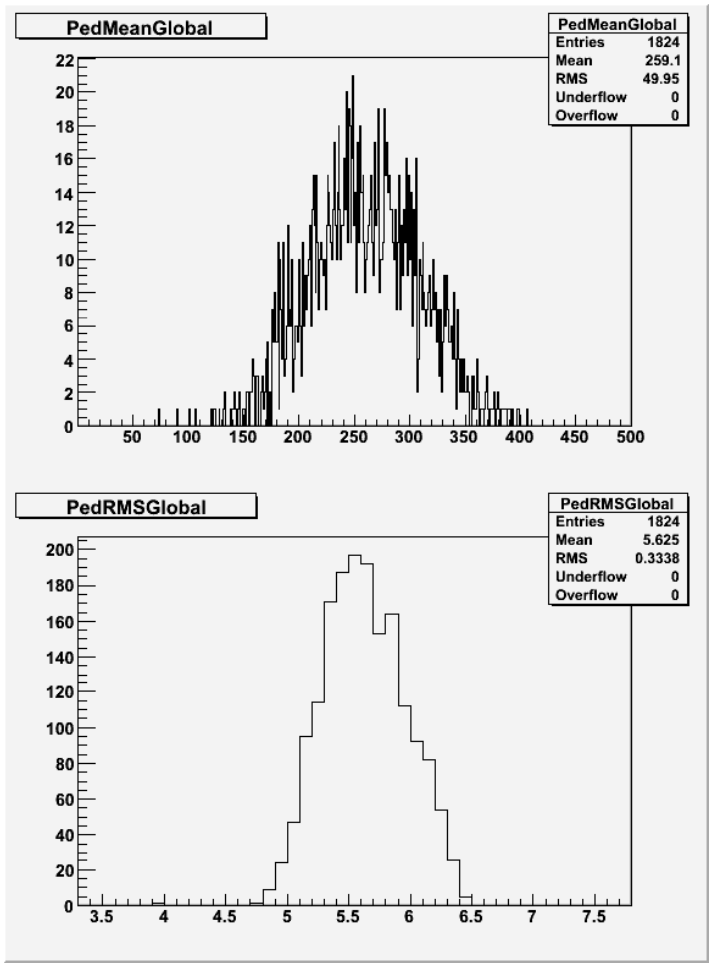
Tests in gas were performed in Saclay

(one faulty pad had to be disconnected)

Pedestals with all channels connected to the detector with flat cables

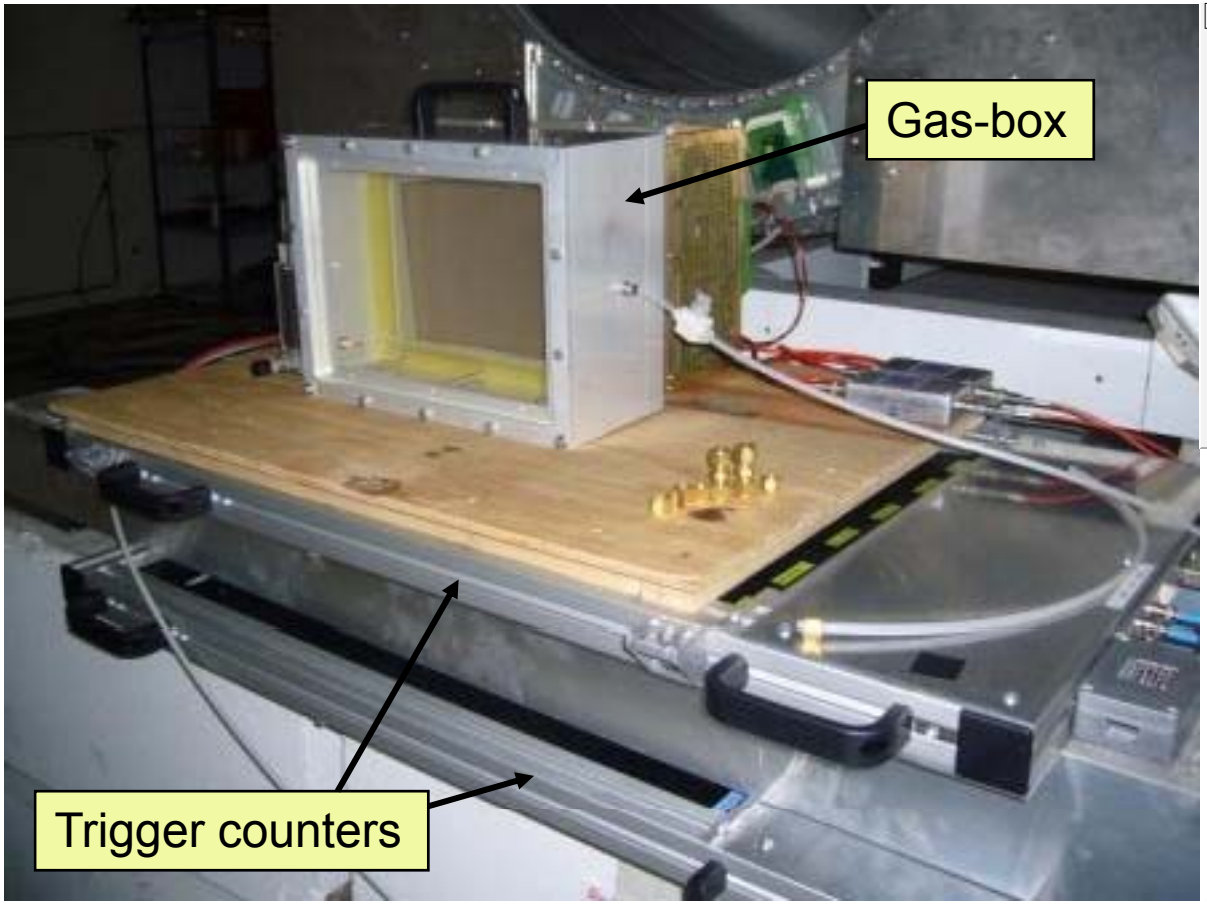
<σ> = 5.6 ADC /4096

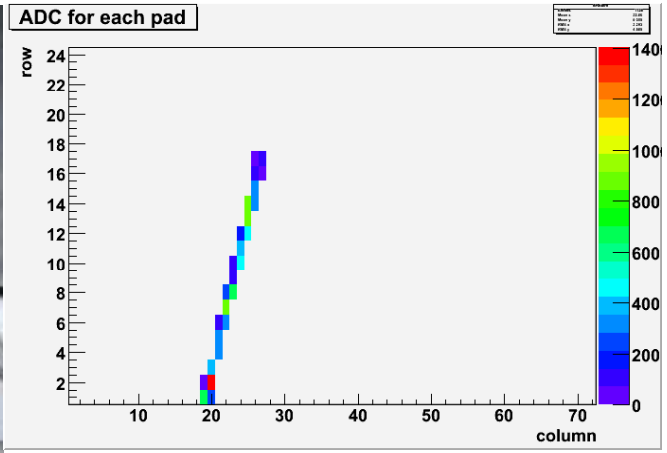


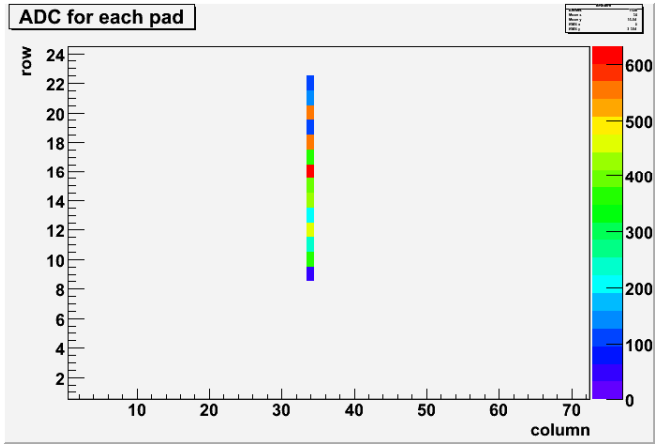


P. Colas, Saclay

MicroMegas Modules







P. Colas, Saclay

MicroMegas Modules

Schedule

Take beam data in the magnet in the period of weeks 44-45-46 (+1?) depending on the field cage status. Then other periods with various PCBs in 2009.

Start R&D for electronics on a mezzanine PCB. Should be ready for early 2010.

- R&D to optimize protection compactness

- Development to test AFTER chips at the wafer level

- new card design

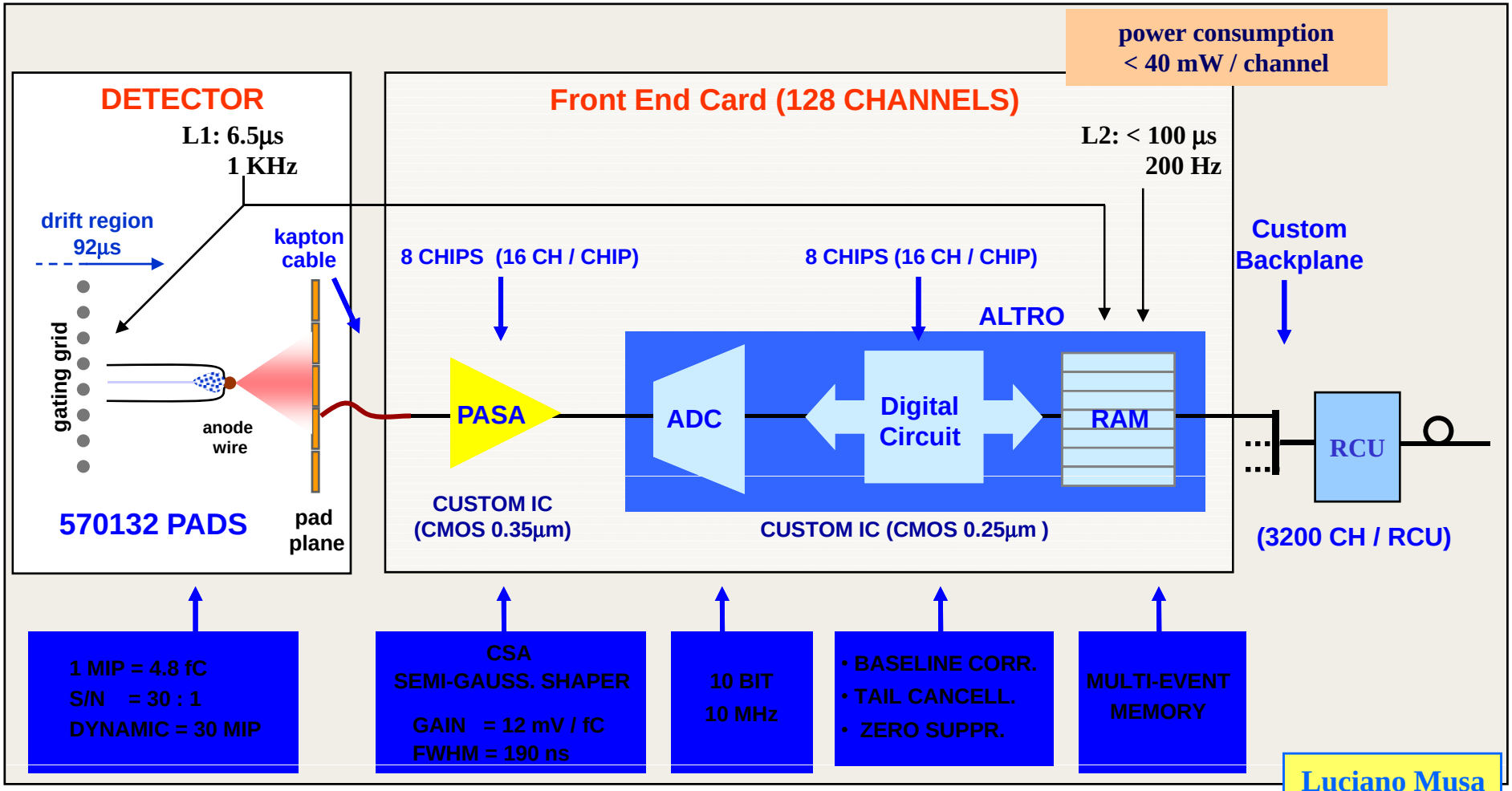
Make 7 fully equipped modules (250 Watts)

Start cooling and integration studies

Resistive coating techniques are being tested

ALTRO Electronics: S-ALTRO

Based on the existing PASA + Altro electronics designed for the Alice TPC



ALTRO Electronics: S-ALTRO

- Application : Designed for the readout of the ILC TPC.
- Fundamental signal requirements : Signal charge, channel number and a time stamp.
- Architecture : Based on existing PASA + Altro electronics for the ALICE TPC.
- Integration : Integrate PASA + Altro functions into a single chip.
- Polarity : Both positive and negative signal response
- Scaling : To fit with 4mm^2 pad size, dimensioning of SRAMs to ILC requirements.
- Technology: IBM 0.13um CMOS.

ALTRO Electronics: S-ALTRO

So far :
Individual blocks have been studied as unique modules.

Power issues :
Power pulsing of PASA and ADC a strong concern.
System effects of power pulsing not clear, it could adversely affect noise performance.

Chip work remaining :
Review of specifications
Study practical suitability of blocks for the S-Altro design.
(technology file conversion LM/DM, floorplan, power routing etc.)

Study to dimension SRAMs.
Floor-plan / package study

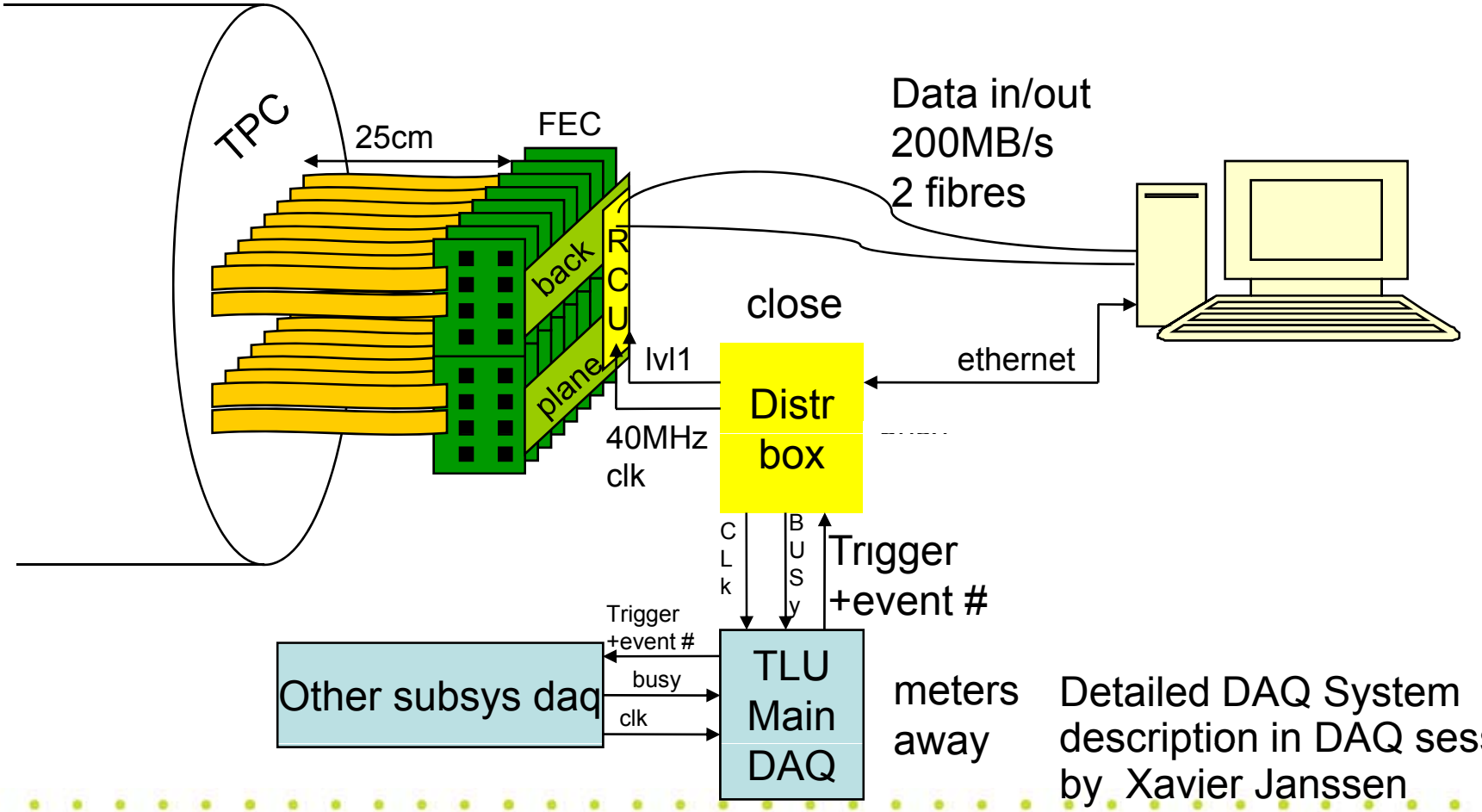
Design modules for the following :
Testability (BIST, probe pads)
Control logic
Internal test pulse generation
Programmable interface + registers

Chip assembly :
Full custom layout work
Synthesis of digital blocks
Simulation with corners
Global power routing
Clock trees
DRC etc.

ALTRO GEM Electronics

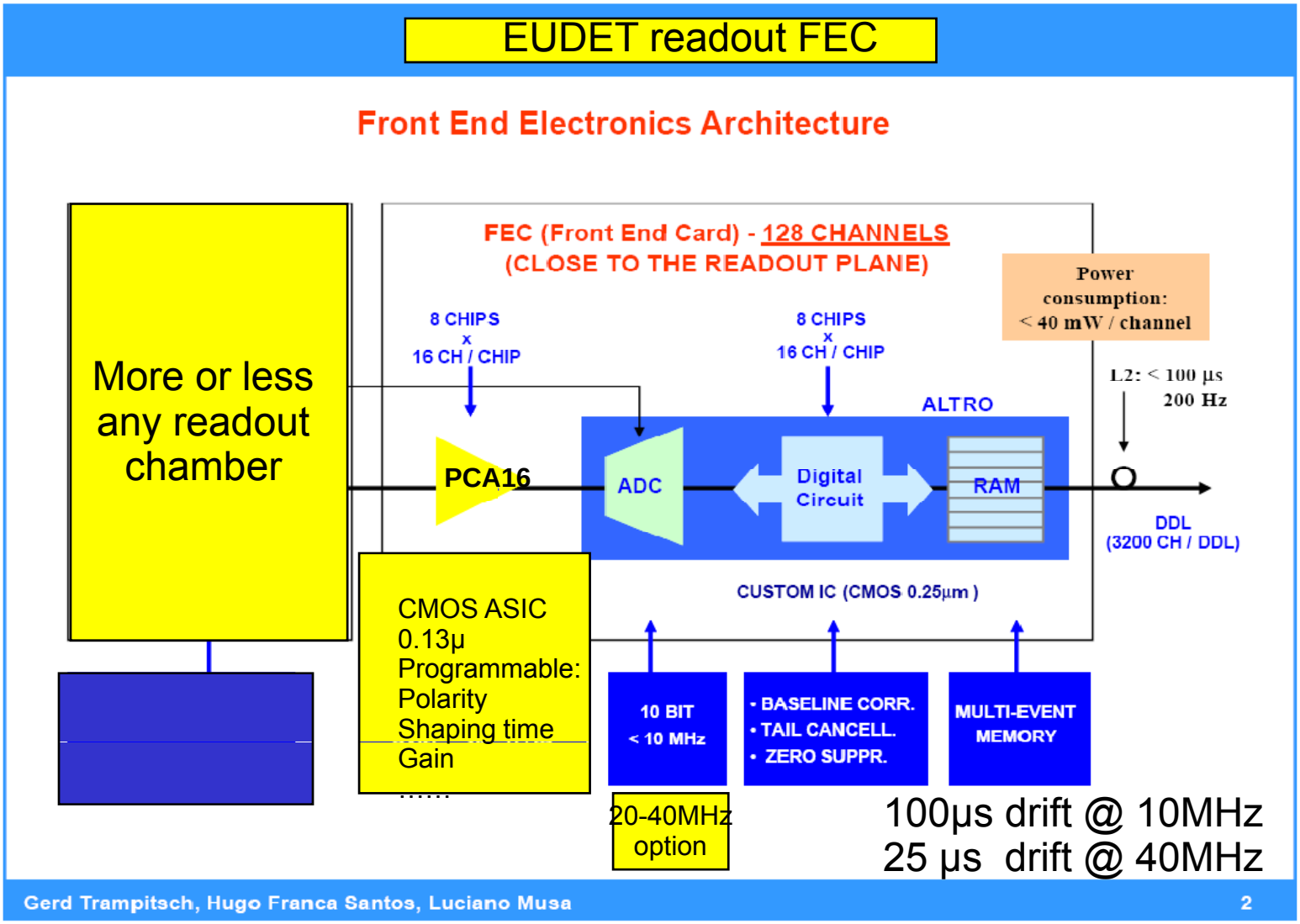
If we run together with other subsystems

2048ch,16 FEC



Detailed DAQ System description in DAQ session by Xavier Janssen

ALTRO GEM Electronics



ALTRO GEM Electronics

ALTRO digitizer+drift storage

-Differential input from PCA 16
-16 channels per chip
-10 bit resolution, 1mV per ADC channel
-1k samples per event

-10MHz sampling in ALICE (100microsecs drift)
-20MHz (50microsecs drift)
-Ca 125 chips with enhanced sampling freq. 40MHz
-Pedestal subtraction, common to all samples
-Advanced zero suppression - good data is sequence (selectable) of non-zero samples.
-Pulse data, + pre and postsamples
-4 event buffering. (multievent buffering not used here)
-several other ALICE features for MWPC pulses are disabled

ALTRO GEM Electronics

The main modifications relative to ALICE FEC

Remote control of PCA16 via board controller

-Optional control by switches removed in final design

-Modified grounding around ALTRO, reduced coherent noise significantly

-Modified reference voltages to ALTRO in order to accomodate all settings of PCA16. So the standard calibration is 1.2mV/ADC channel. If experience tells us that some settings may not be used, this may be changed back to 1mV/channel by changing 2 resistors per FEC).

-skipped water cooling

-Added one external voltage+regulator for PCA16, 1.5V. Saved ca 20% pwr.

ALTRO GEM Electronics

CHIP Availability

EUDET

-PCA16, 160 tested and available in Lund for 2048ch system

-ALTRO 25MHz, 160 tested and available in Lund for 2048ch system

-ALTRO 40MHz for high resolution sweet spot, ca 100 operational at CERN (needs desoldering from boards).

LC-TPC project

-PCA16, 772 chips arrived last week (ca 90FEC). Testing ca 2 weeks.

-25MHz ALTRO, tested, 400 in Lund, ca 300 to get from CERN

ALTRO GEM Electronics

- **5 FEC assembled last week+2 existing, 1120 channels, (EUDET 1000ch system). Evaluate nxt week**

- Oct 17: order 100 FEC Circuit boards. 3 w delivery; tests of PCA16

- Nov 10: assemble 11 (27) FEC 2w delivery

- Nov 24: 2048 ch EUDET system ready

(option to discuss 32 FEC max RCU system 4096 ch instead of 2048)

- **Get 40MHz option operational**

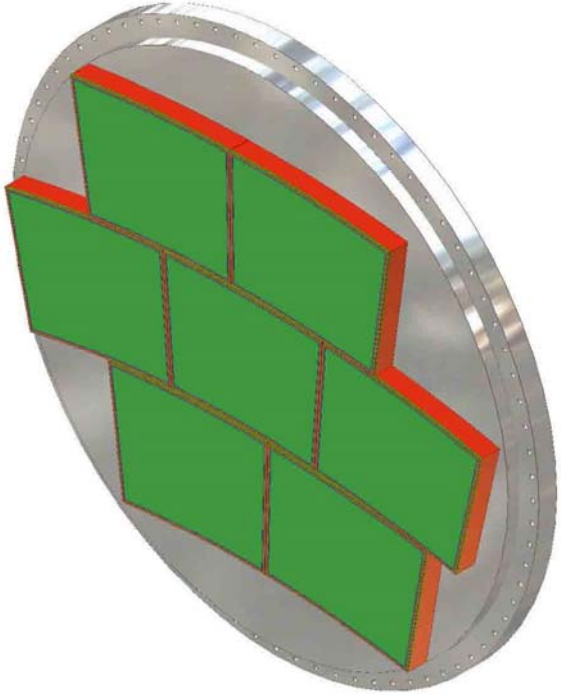
After experience with full crate system, finalize cooling

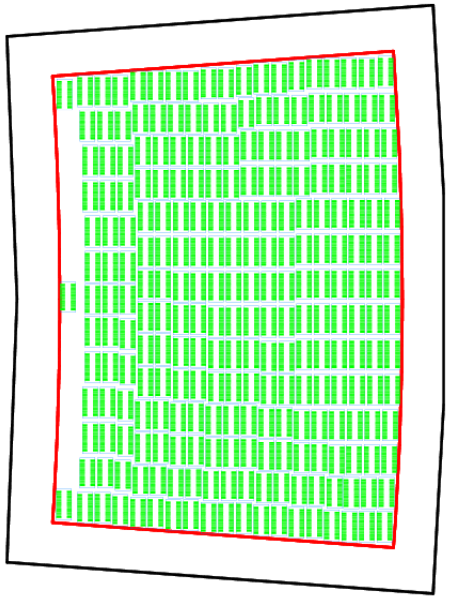
- **At any time when needed, assemble remaining FECs, depends on chip yield but ca 100 FECs in total can be expected. Takes 2w after order.**
- **4 parallell systems, RCU and out, ordered with delivery during october.**

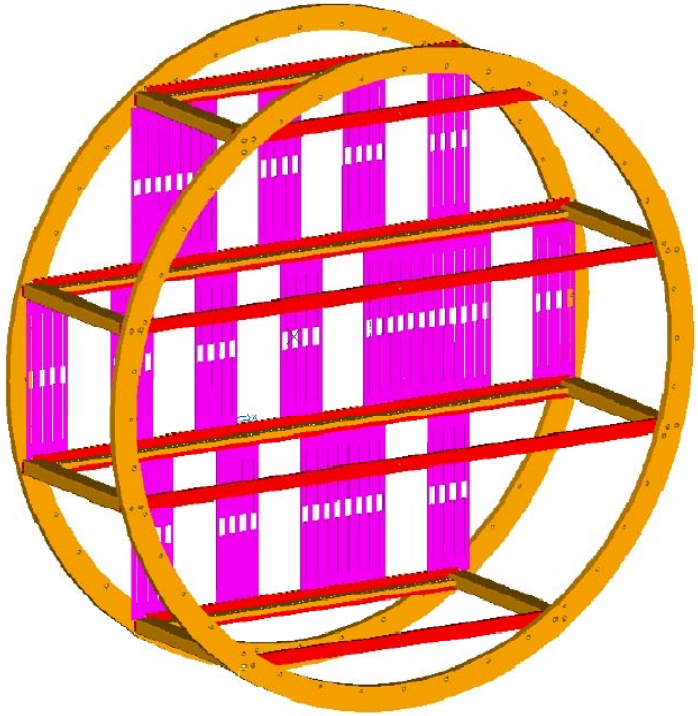
  plus one development system in Lund and one in Brussels.
- **Mechanics & cooling**

ALTRO GEM Electronics

Mechanics in progress

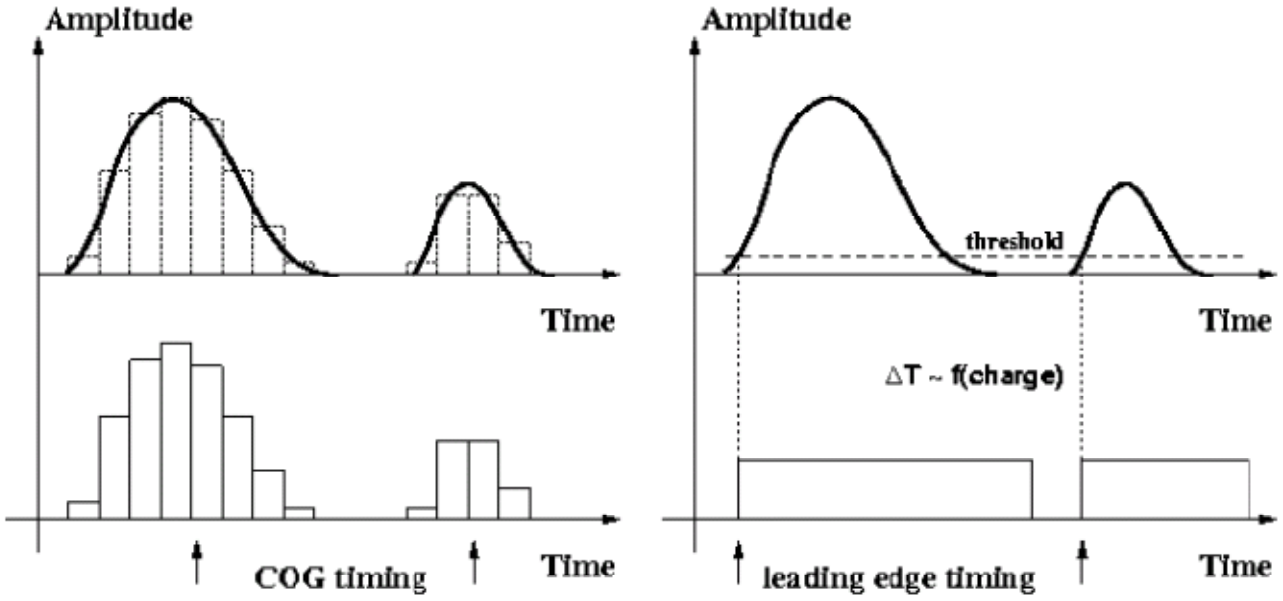






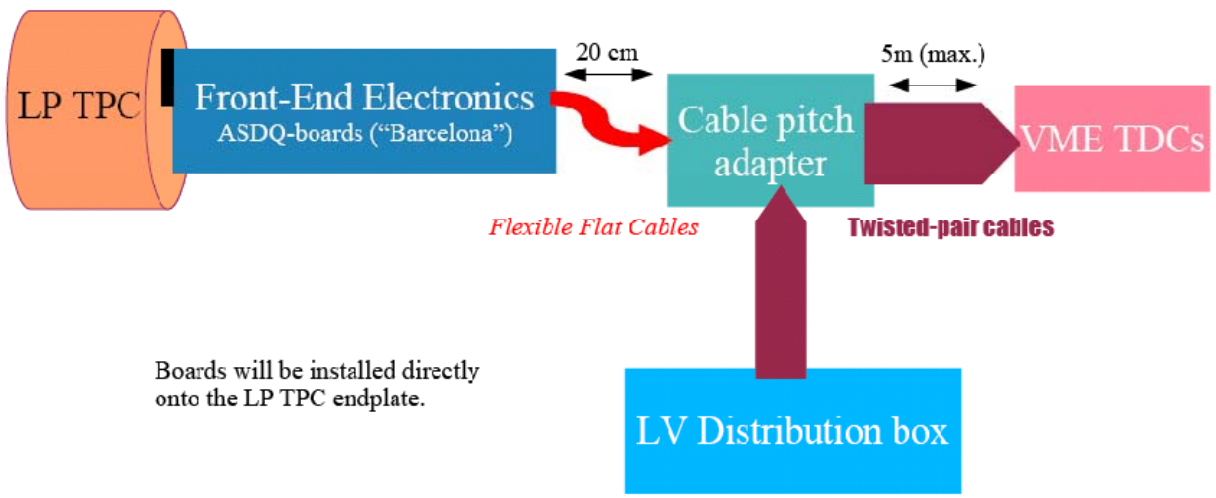
TDC Electronics

TPC signal processing with Time-to-Digit Converter



- The time of arrival is derived using the leading edge discriminator.
- The charge of the input signal is encoded into the width of output digital pulse.

TDC Electronics



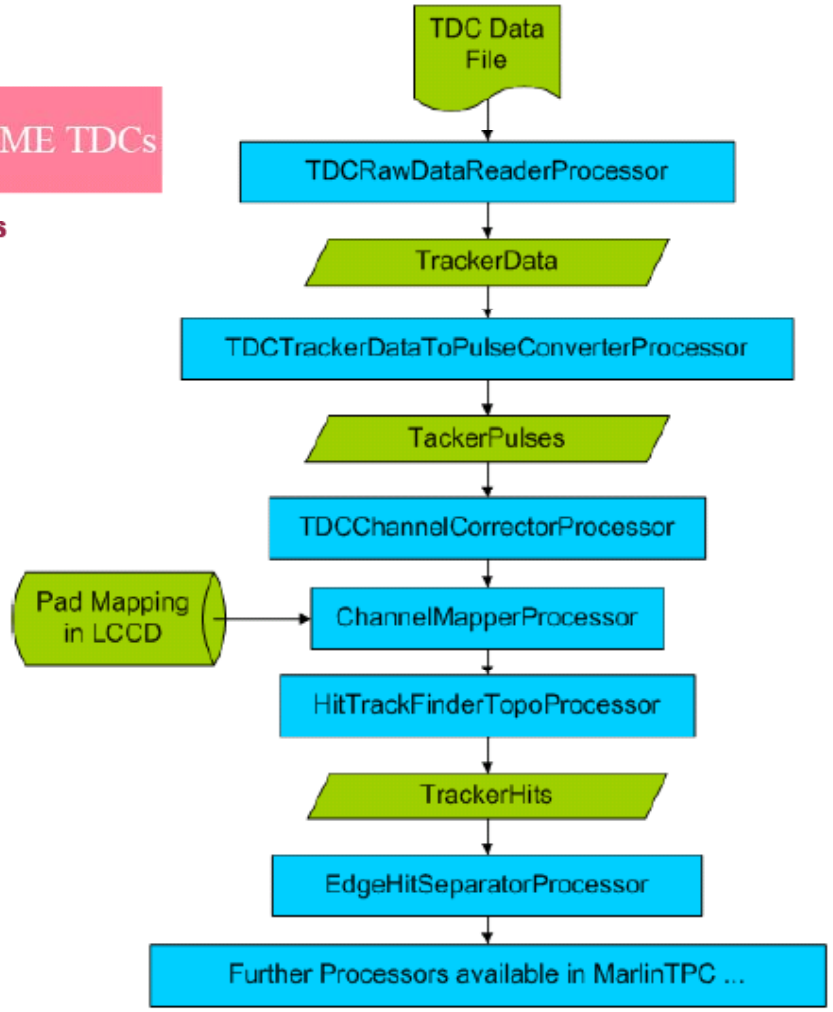
Boards will be installed directly onto the LP TPC endplate.

32 channels in 30 mm * 106 mm
Top-to-bottom thickness: 4.4 mm
Weight: ~15g

First tests successful

2 boards assembled for first tests
28 will be assembled later

20 boards will be used (640 channels)



TDC Electronics

Main components of the readout electronics are there.
Low voltage distribution is still missing.

Next steps:
- Test with small TPC chamber
- Integration with EUDAQ
- Twisted pair cable ?
- Cooling and support structure preparation

Options:
- Compact VME crate (with remote power supply)
- Power cycling ?

Summary & Outlook

- LP infrastructure expected to be available in week 43 (by end of October)
- MicroMegas module with AFTER electronics to be assembled with TPC in week 44
- Commissioning of LP with MicroMegas and DESY electron beam starting from week 45
- ALTRO EUDET system available in week 47

ALTRO Electronics: S-ALTRO

Prototype 1

- Prototype Layout
  - **12 Channels**
    - 7 Standard
    - 5 Test
  - **3 mm² Silicon Area**
- Test Channels
  - **Fast Channel**
  - **Triple Gain Channel**
  - **Different Preamplifier Architectures**
    - Folded Cascode
    - Rail to Rail Preamplifier
    - Regulated Cascode
- Input Charge Range
  - **200 fC Standard Channel**
  - **60 fC Triple Gain Channel**

Programmable Charge Amplifier (PCA 16)

Goals :

- 1.5 V Supply, power consumption < 8 mW / channel
- 16 channel charge amplifier + anti-aliasing filter
- Single ended preamplifier
- Fully differential output amplifier
- Both signal polarities
- Power down mode (wake-up time = 1 ms)
- Programmable peaking time (30 ns – 120 ns) – 3rd order semi Gaussian pulse shape
- Programmable gain in 4 steps (12 – 27 mV/fC)
- Pre-amp_out mode
- Tunable time constant of the preamplifier
- Pitch 190.26um, Channel length 1026um,
- Chip dimensions = 1.5mm x 4mm

ALTRO Electronics: S-ALTRO

ADC Specs

Input stage	Differential
No. of bits	10
Conversion rate	< 40Ms/s
Power consumption	< 10mW at 10Ms/s
Power up/down mode	Yes with wake up time < 1ms
Layout area	< 1mm^2

ADC Status

High-speed, high-resolution analogue-to-digital converter

- Resolution: 10 bits
- Speed: up to 40 MSPS
- Power: 32 mW @ 40 MSPS
- Area: 0.78 mm^2 in a 0.13 μm CMOS process

The pipelined architecture offers the best trade-offs for System on Chip.

Pipelined ADC: 8x1.5bit stages + 1x2 bit stage

ALTRO Electronics: S-ALTRO

Pipelined ADC: Spec.s & Schedule

- Supply: 1.5V single
- Input: 1Vpp swing (2V differential)
- Resolution: 10-bit
- Sampling rate: 40 MSPS
- Power consumption: 32mW at 40MSPS per channel
- Channels: 2
- Single channel area: 0.78 mm^2

ADC project schedule

• October	2008 -	Design review
• November	2008 –	Submission in a MOSIS MPW
• February and March	2009 –	Test and characterization at CERN

Furthermore: Studies of DSP, Lower Power Design, Compression