A 130nm CMOS Digitizer Chip for Silicon Strips readout at the ILC

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on behalf of

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Work in the framework of the SiLC (Silicon for the Linear Collider), R&D Collaboration
and the EUDET I3-FP6 European Project

Outline

- *Silicon strips readout*
- *Front-End Electronics*
- *The 4-channel evaluation chip in 130nm CMOS*
- *The 88 channel chip*
- *Conclusion*

Silicon strips detectors at the ILC

Envelope around the central tracking device

Assume:

- A few 10^6 Silicon strips
- 10 - 30 cm long,
- Thickness 200–300 μm
- Strip pitch 50 μm
- AC coupled (DC coupled if necessary)

→ Millions of channels
Integration of k-scale channels readout chip

Silicon strips data

- Pulse height: Cluster centroid to get a few µm position resolution

→ *Detector pulse analog sampling*

- Time: 150-300 ns for BC identification

→ *Shaping time of the order of the microsecond depending upon strip length (capacitance)*

→ 80ns analog pulse sampling and on-chip digitization

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Functionalities to be integrated

- Full readout chain integration in a single chip

  - Preamp-shaper
  - Sparsification — Trigger decision on analog sums
  - Sampling — 8-deep sampling analog pipe-line
  - Analog event buffering: — Occupancy: 8-16 deep event buffer
  - On-chip digitization — 10-bit ADC
  - Buffering and pre-processing:
    Centroids, least square fits, lossless compression and error codes
  - Calibration and calibration management
  - Power switching (ILC duty cycle)

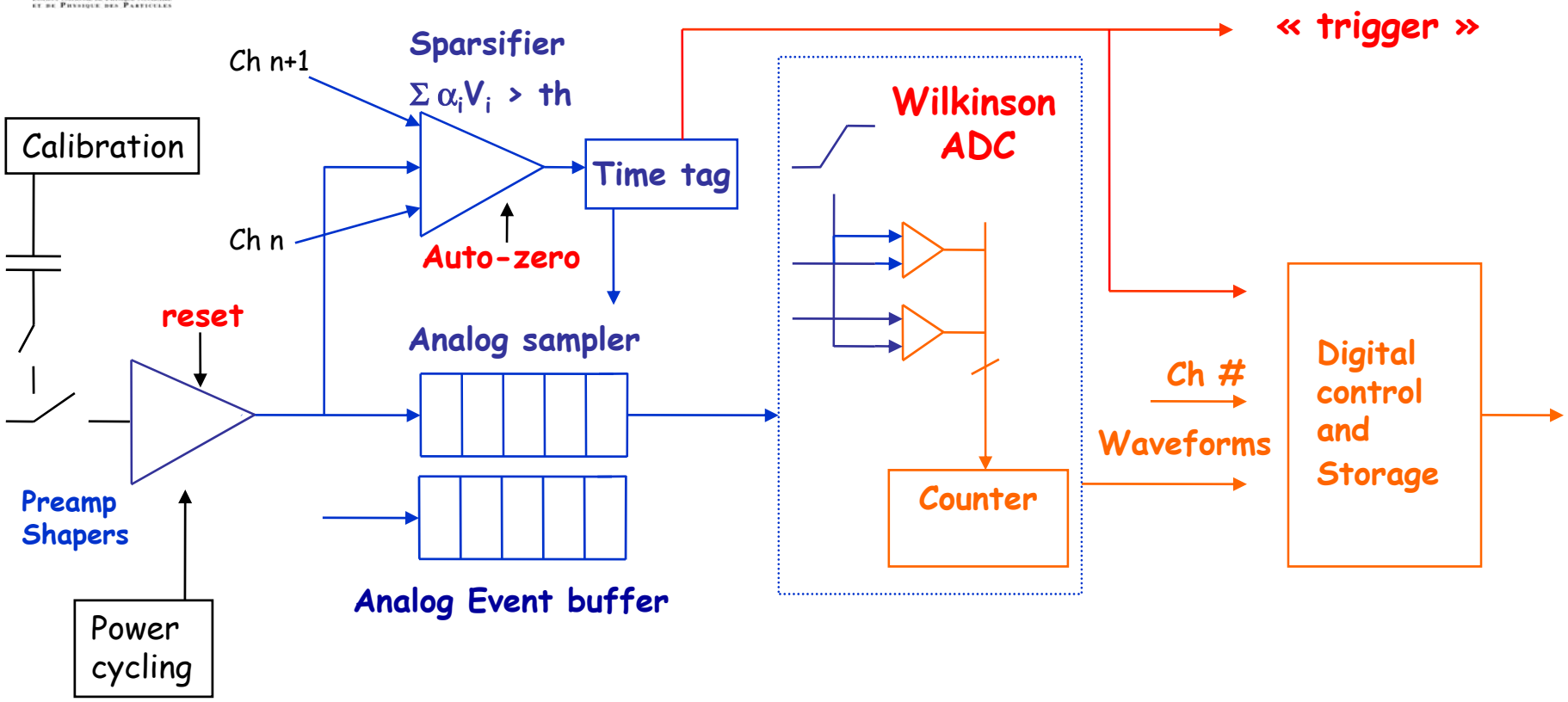
Front-End chip numbers

Goal: Integrate 512-1024 channels in 90nm CMOS:

- **Amplifiers: - 30 mV/MIP over 30 MIP range**
- **Shapers: - ranges: 500ns-3μs**
- **Sparsifier: - Threshold the sum of 3-5 adjacent channels**
- **Samplers: - 8 samples at 80-640ns variable sampling clock period**
  - Event buffer 8-16 deep
- **Noise baseline:**
  Measured with 180nm CMOS:
  375 + 10.5 e-/pF @ 3 μs shaping, 210μW power
  S/N ~ 20
- **ADC: - 10 bits**
- **Buffering, digital pre-processing**
- **Calibration**
- **Power switching can save a factor up to 200**

ILC timing: 1 ms: ~ 3000 trains @ 360ns / BC 199ms in between

Front-end architecture



Charge 1-30 MIP, Time resolution: BC tagging 150-300ns
80ns analog pulse sampling

Technology: Deep Sub-Micron CMOS 130-90nm

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Front-end in 130nm

Motivation for 130nm CMOS:

- Smaller
- Faster
- Less power
- Will be (is) dominant in industry
- (More radiation tolerant)

Drawbacks:

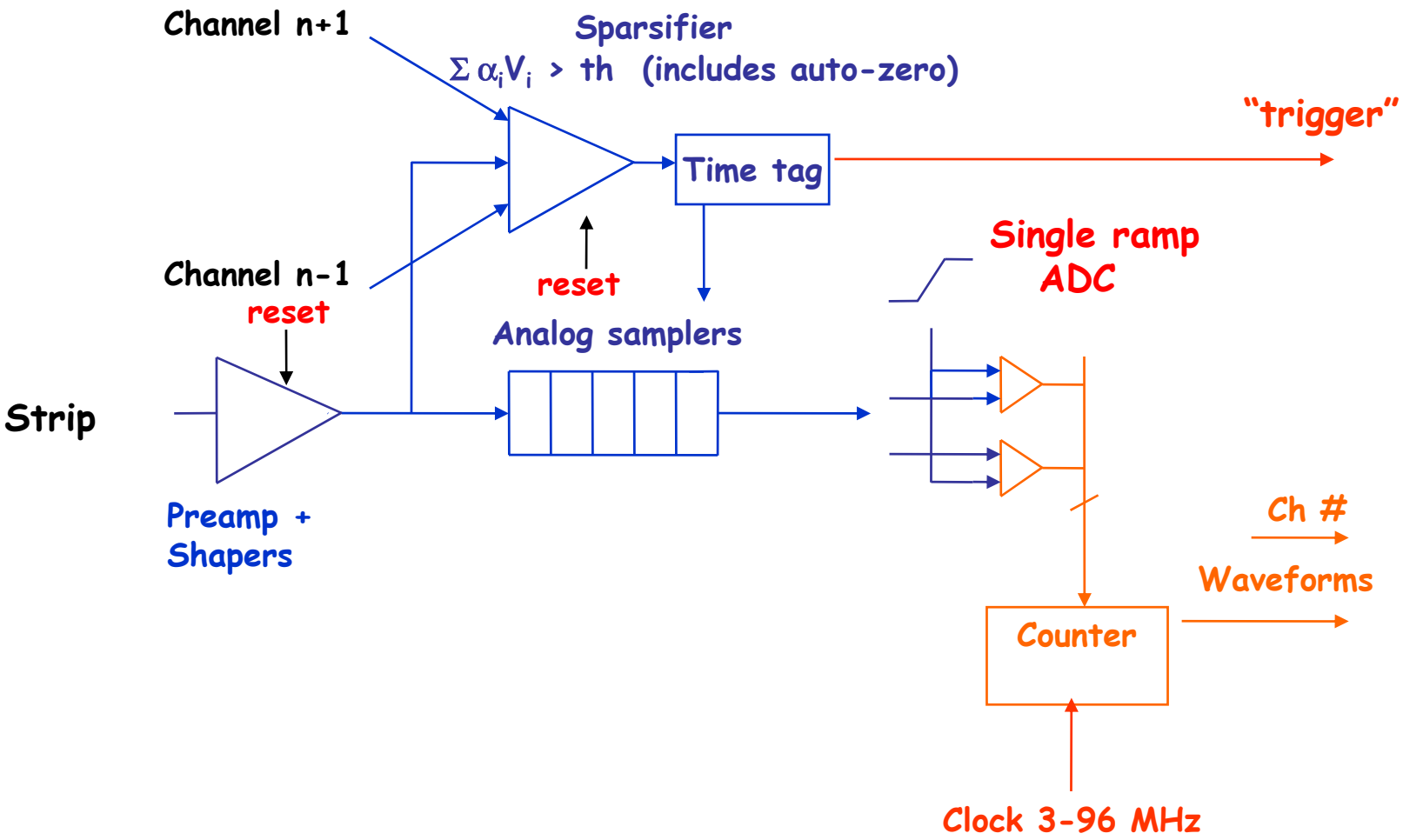
- Reduced voltage swing (Electric field constant)
- Noise slightly increased (1/f)
- Leaks (gate/subthreshold channel)
- Design rules more constraining
- Models more complex, not always up to date

UMC CMOS Technology parameters

	180 nm	130nm
• 3.3V transistors	yes	yes
• Logic supply	1.8V	1.2V
• Metals layers	6 Al	8 Cu
• MIM capacitors	1fF/μm²	1.5 fF/μm²
• Transistors	Three Vt options	Low leakage option

Help from IMEC Europractice (Leuven, Belgium): Paul Malisse, Erwin Deumens

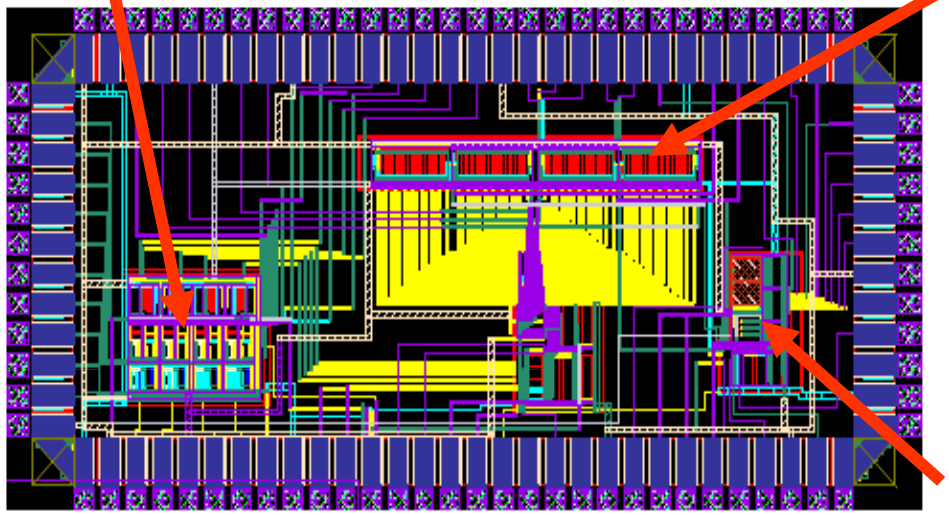
4-channel Chip



4-channel chip layout

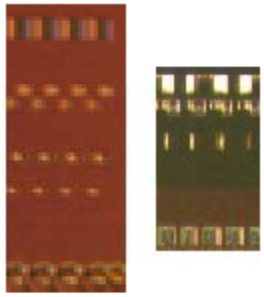
Amplifier, Shaper, Sparsifier 90*350 µm²

Analog sampler 250*100 µm²



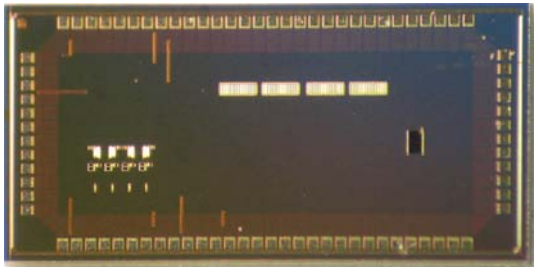
A/D 90*200 µm²

Layout of the 130nm chip including sampling and A/D conversion



180nm 130nm

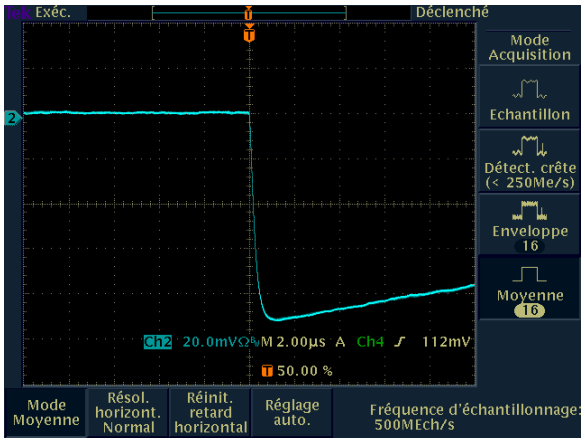
Photo



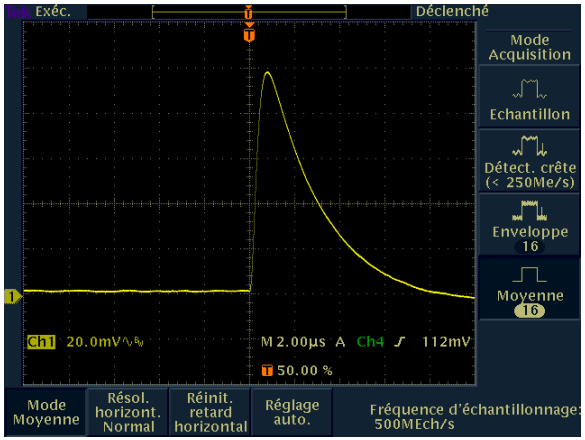
Preamp-shaper results

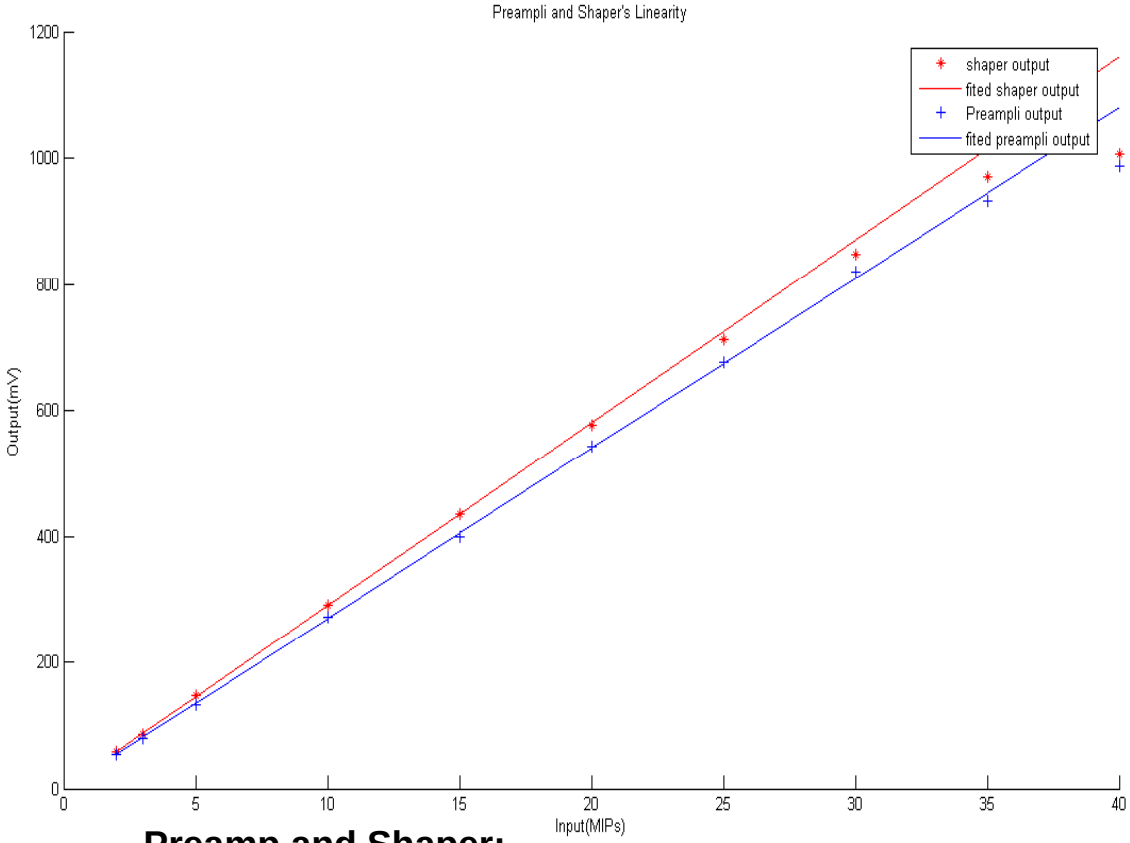
Measured gain - linearities

Preamp output



Shaper output

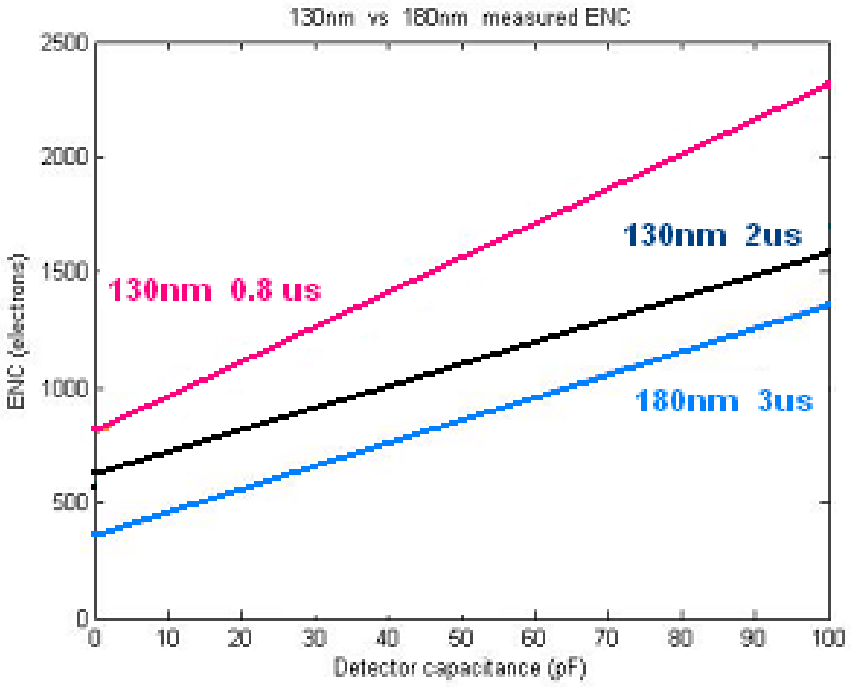




Preamp and Shaper:

Gain = 29mV/MIP
Dynamic range = 20MIPs 1%
30 MIPs 5%
Peaking time = 0.8-2.5µs / 0.5-3µs expected

Noise results

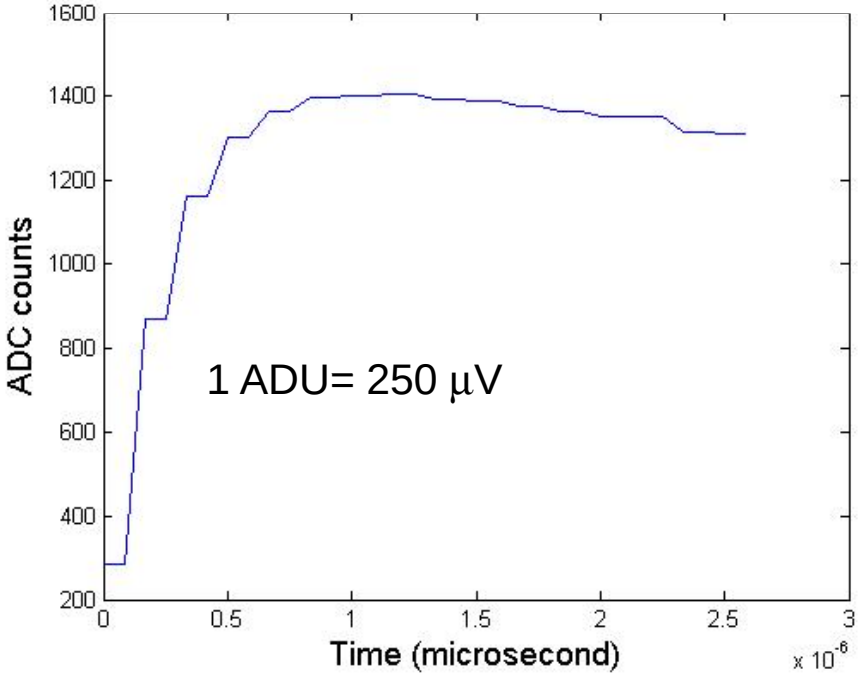


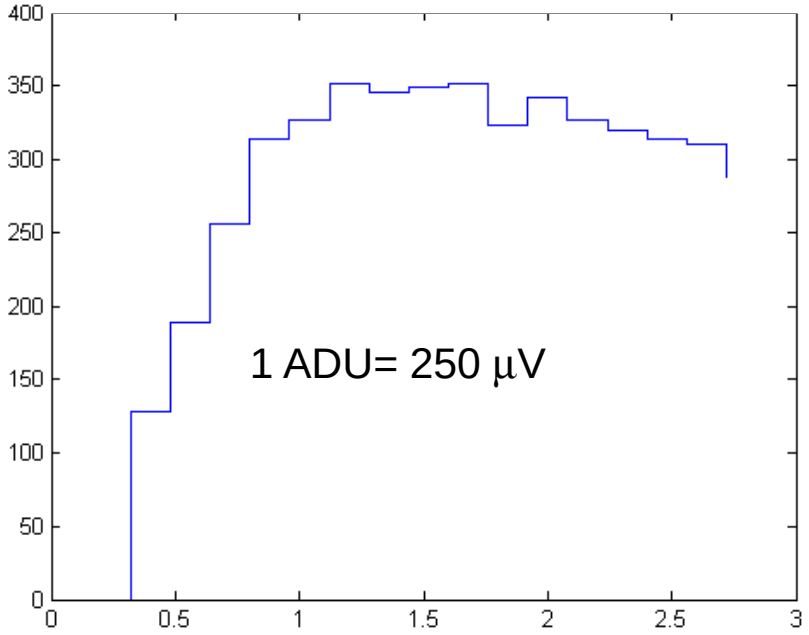
Power (Preamp+ Shaper) = 245 µW

Noise: 130nm @ 0.8 µs : 850 + 14 e-/pF 245 µW (150+95)
130nm @ 2 µs : 625 + 9 e-/pF
180nm @ 3 µs : 375 + 10.5 e-/pF 210 µW (70+140)

Digitized analog pipeline output
Laser response of detector + 130nm chip

Digitized shaper output



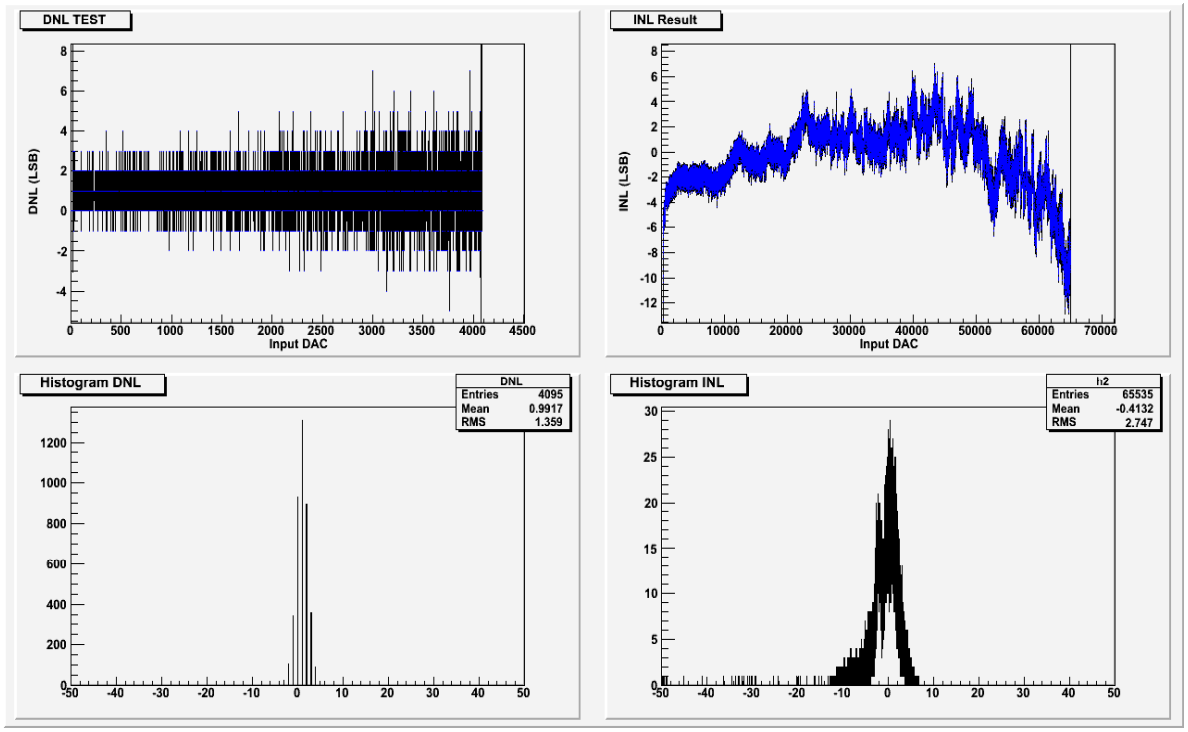


Sampling rate = 12 MHz
Readout rate = 10 KHz

From calibration pulser as input

From Laser diode + Silicon detector

ADC TEST



DAC Input :

Dynamic : 0 – 1V

Offset : ~1V

ADC Output :

From 50 bin to 3780 bin:

+INLmax = 7 LSB

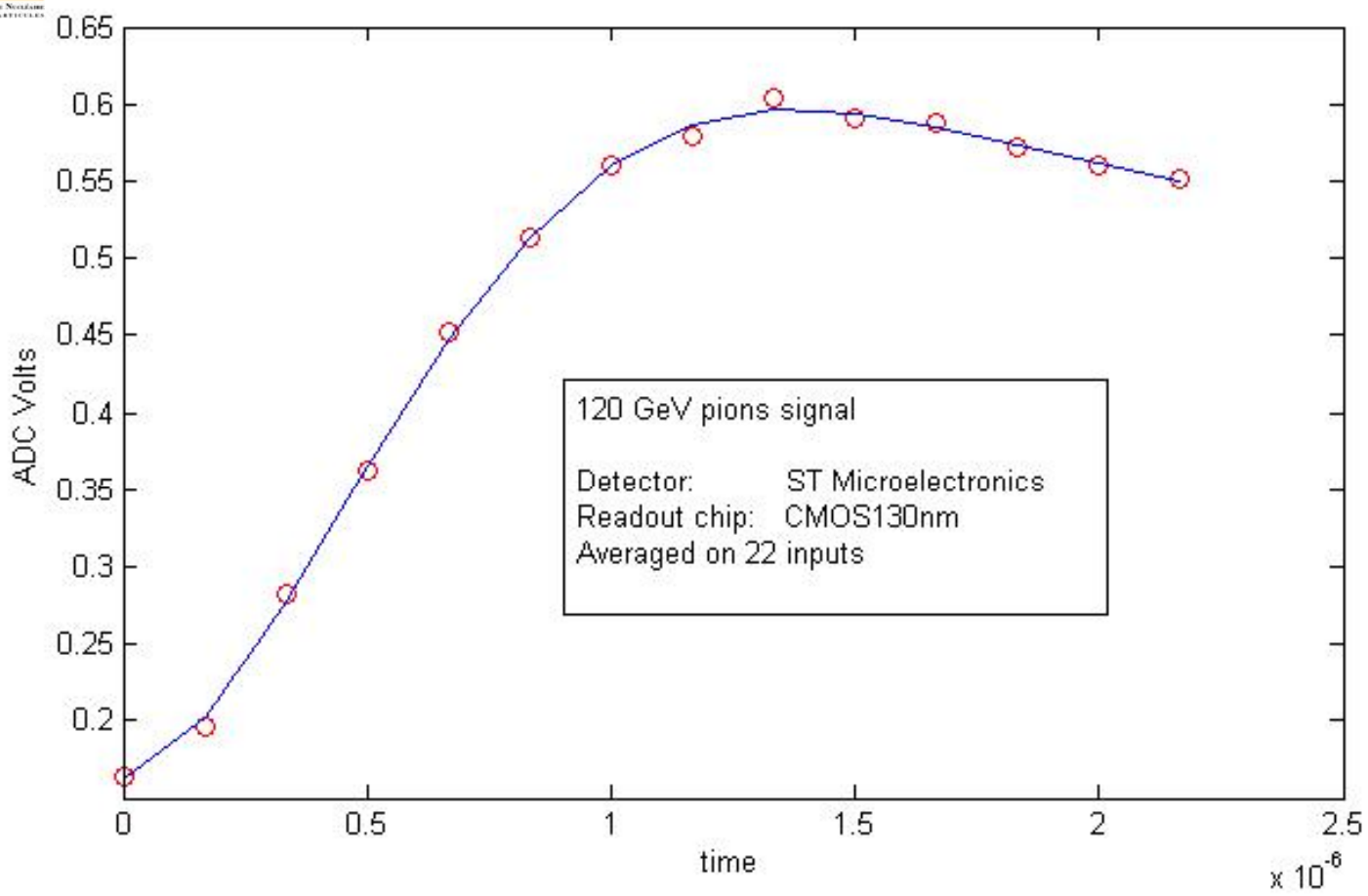
+INLrms = 2.74 LSB

+DNLmax = 7 LSB

+DNLrms = 1.36 LSB

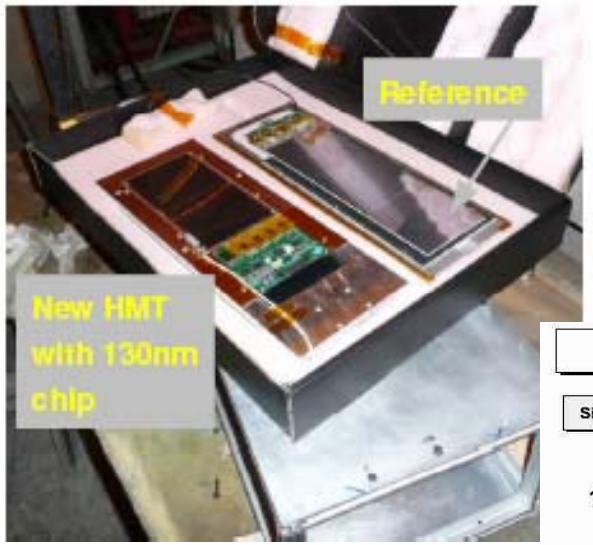
→ ~ 9b effective in the worst case

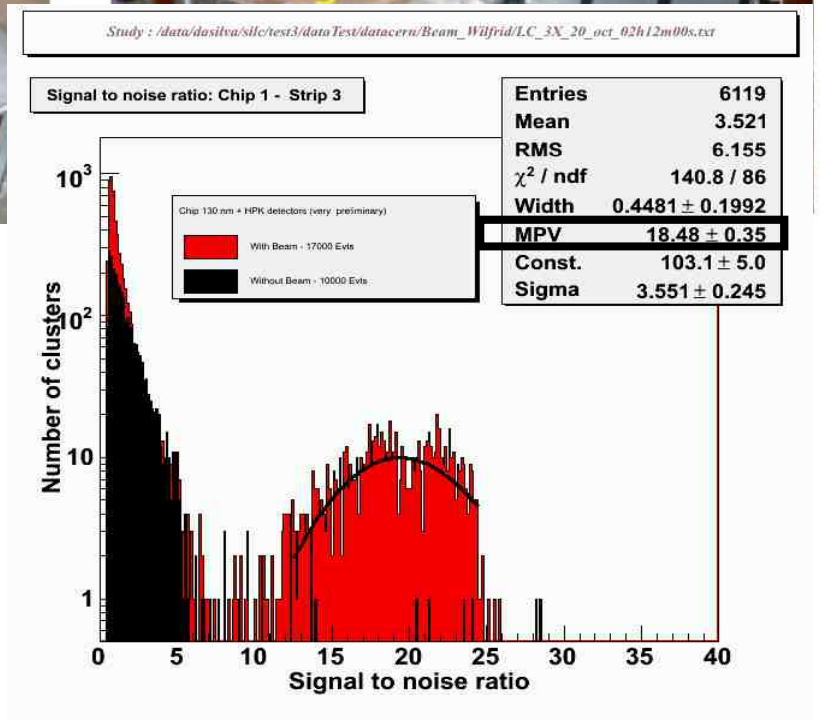
CERN Beam tests results



- Averaged response of 120 GeV pions through 500 μm thick Silicon detector
- Pedestal subtracted off-line, then digitized shaper waveform OK.

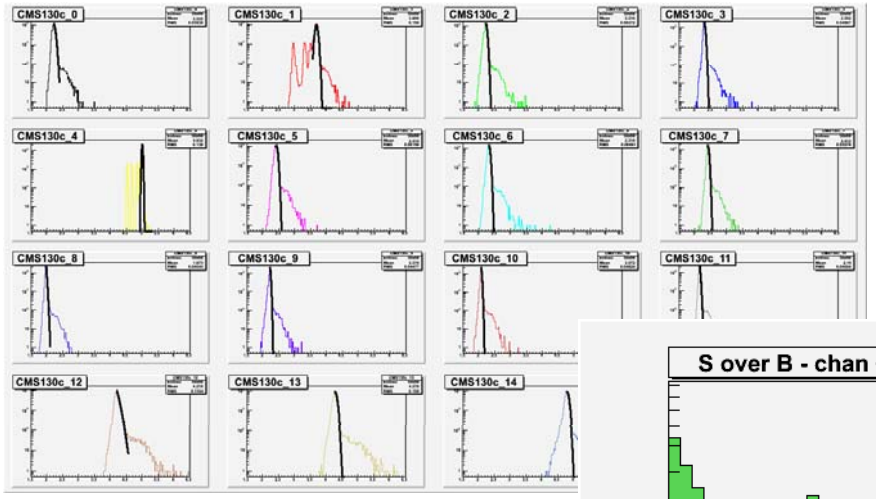
130nm chip test-beam response

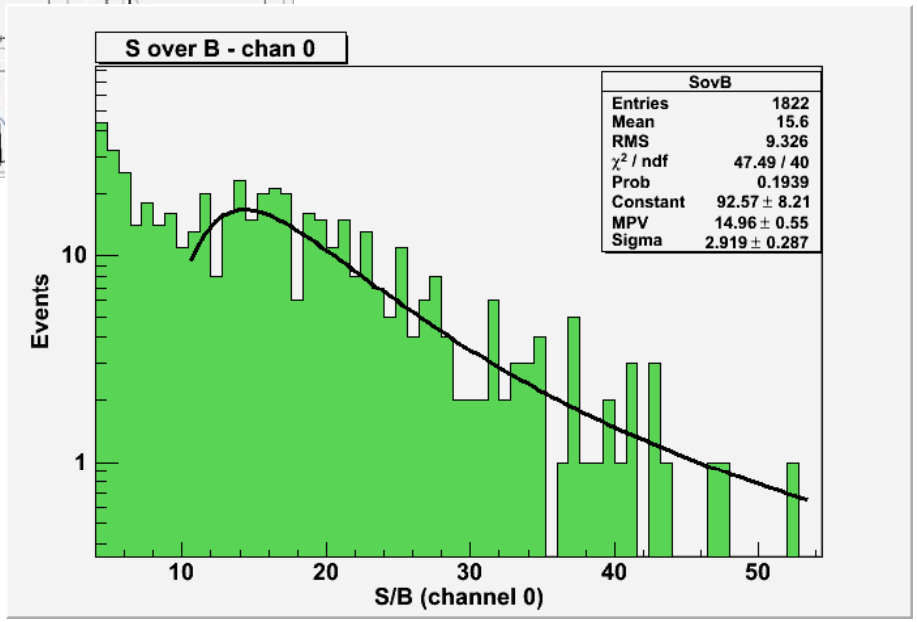




Signal to Noise ratio
From beam-tests

130nm Sr^{90} radio active source





Signal to Noise ratio From Sr^{90} radio-active source (HPK sensors)

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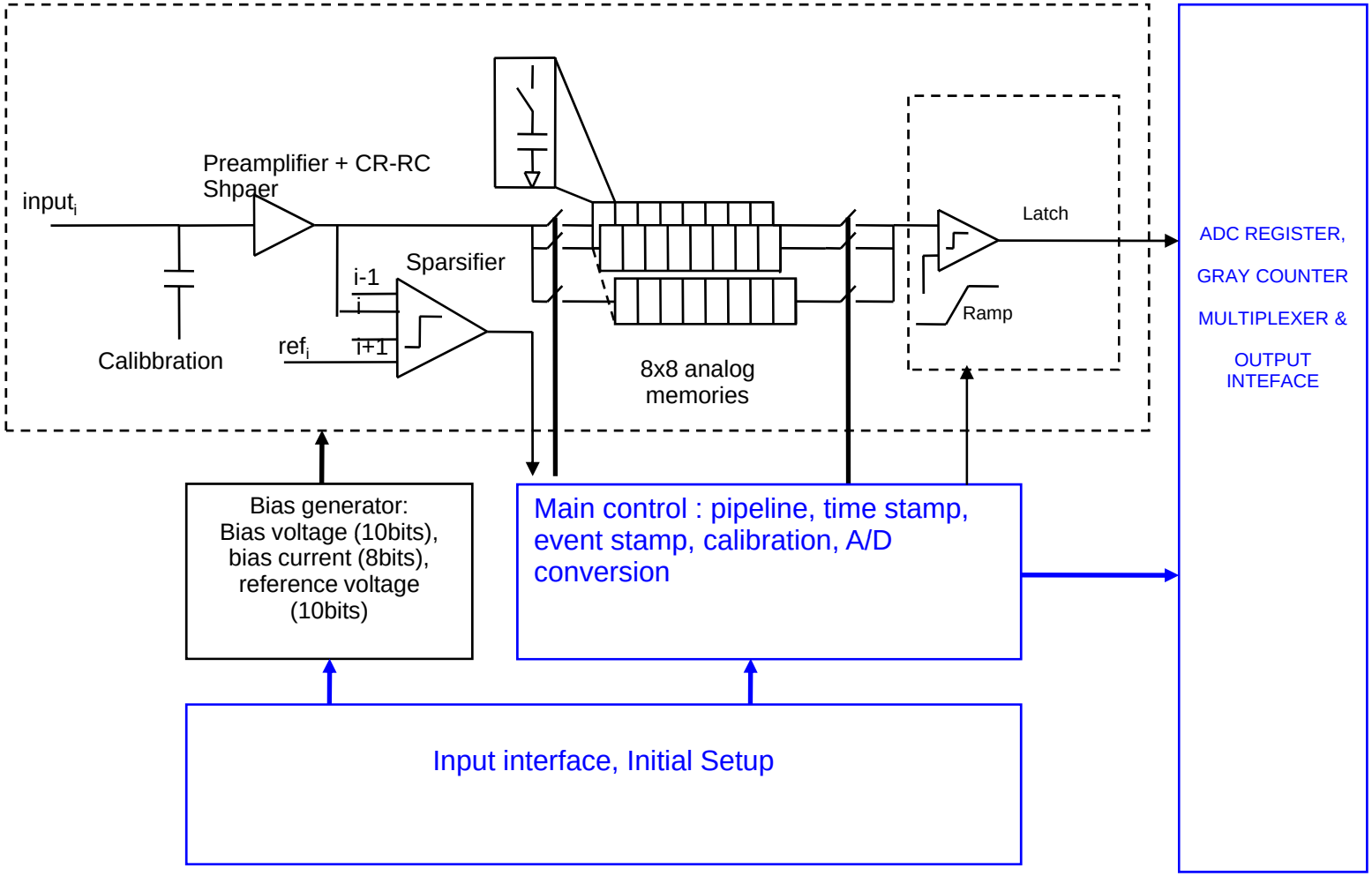
Block diagram



88 channels chip

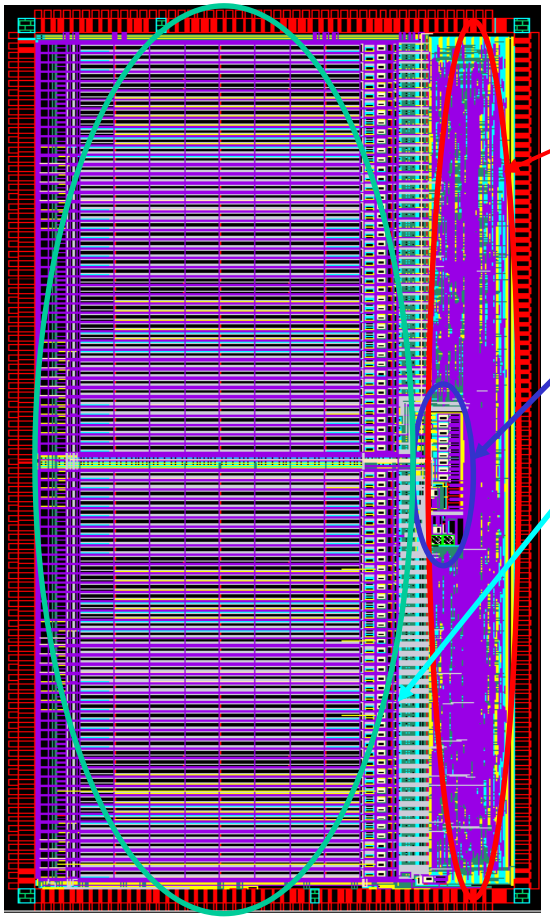
Electrics:
-Consumptions : ~ 1.1mW/channel
-LVTTL digital IN/OUT

Features:
- 88 channels in 130nm CMOS
(Preamplifier, Shaper, Sparsifier, 2D 8x8 analog memories,12 bits ADC)
  - Integrated calibration
  - Power switching
  - Digital controls

(Bias, threshold, sampling, zero suppression data out, time/event stamp, power switching control, serial in/out interface)

Two samples :
60 naked dies
20 packaged dies

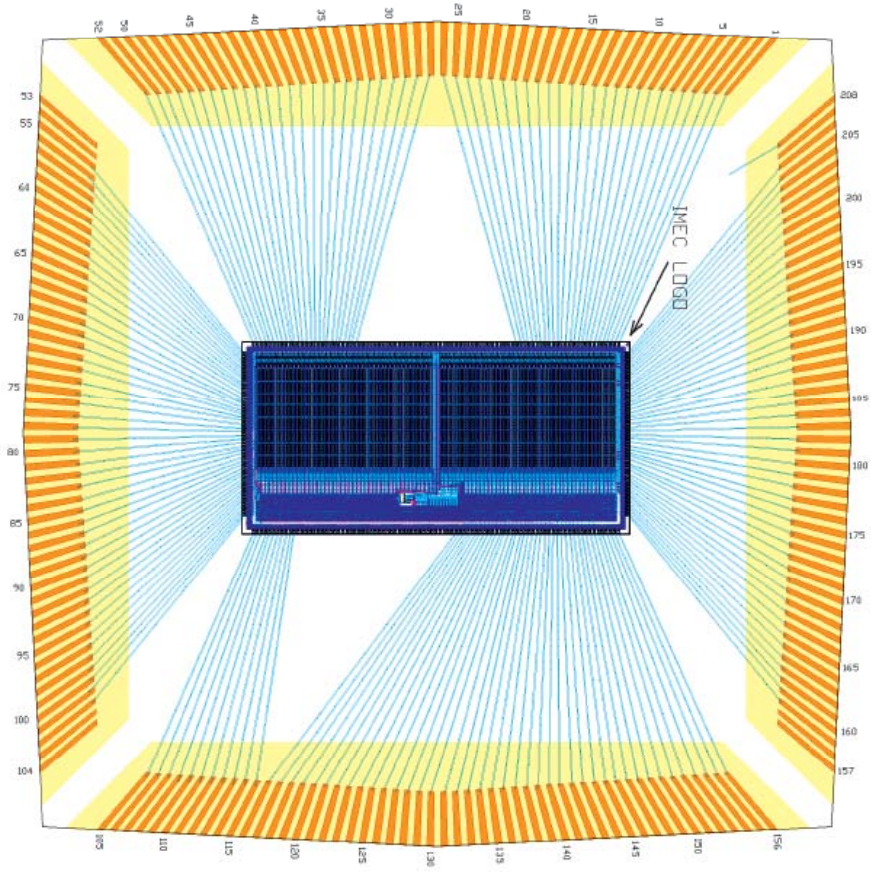
88 channels chip



Layout of 88 channels readout circuit (5mmx10mm)

Designed :
Jan/08 – Juin/08
Contribution:
Analog : LPNHE
Digital : UB
Reception:
Naked die : Sep 12th 08
Packaged die : Mid Octorber/08 (Expected)

88 channels chip



CQFP 208

- 50 analog input including 1 test channel

-> Functional test, productivity

88 channels chip

❖ **Functional test with packaged chip**

- Front-end board -> already designed (will be soon available)
- DAQ Software
  - “simplified” version -> charged by University of Barcelone
    - -> Initialization, probe digital signal
    - -> Confirm the functionality of the chip
    - -> Power test (bias voltage, current)
    - -> Test channel : Preamplifier, Shaper …
  - “developed” version -> under development, charged by LPNHE+UB
    - -> ADC characterization
    - -> Calibration scan
    - -> Optimization …

❖ **Beam/radio active source test (detector + naked die)**

- Front-end board -> already designed (4 naked chips/module)
- DAQ Software
  - Previewed extension in actual acquisition system (FPGA board + soft)

(see Alexandre’s talk)

Conclusion

The CMOS 130nm design and test results demonstrate the feasibility of a highly integrated front-end for Silicon strips (or large pixels).

The new 88 channels chip is available for the test. This chip will be able to equip the large silicon strip modules and confirm the strategy of the developement

The end...