Design of EUDET Prototype

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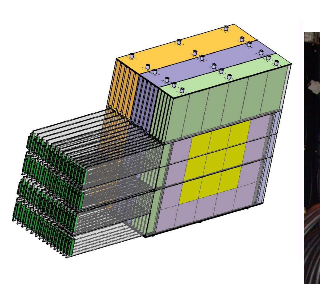
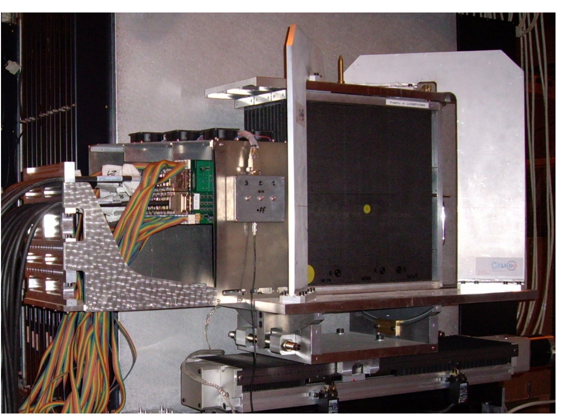
This talk summarizes the TDR for the EUDET Ecal
eudet-memo-2008-11
and is the result of a collaborative work
between

EUDET Annual Meeting NIKHEF Amsterdam/Netherlands Oct. 08

EUDET Prototype

- Logical continuation to the physical prototype study which validated the main concepts : alveolar structure , slabs, gluing of wafers, integration
- Techno. Proto : study and validation of most of technological solutions wich could be used for the final detector (moulding process, cooling system, wide size structures,…)
- Taking into account industrialization aspect of process
- First cost estimation of one module





- **3 structures : 24 X_0 (10×1,4mm + 10×2,8mm + 10×4,2mm)**
- **sizes : 380×380×200 mm3**
- **Thickness of slabs : 8.3 mm (W=1,4mm)**
- **VFE outside detector**
- **Number of channels : 9720 (10×10 mm²)**
- **Weight : ~ 200 Kg**

Technological prototype

3×15 cells

Short detector slabs (×14)

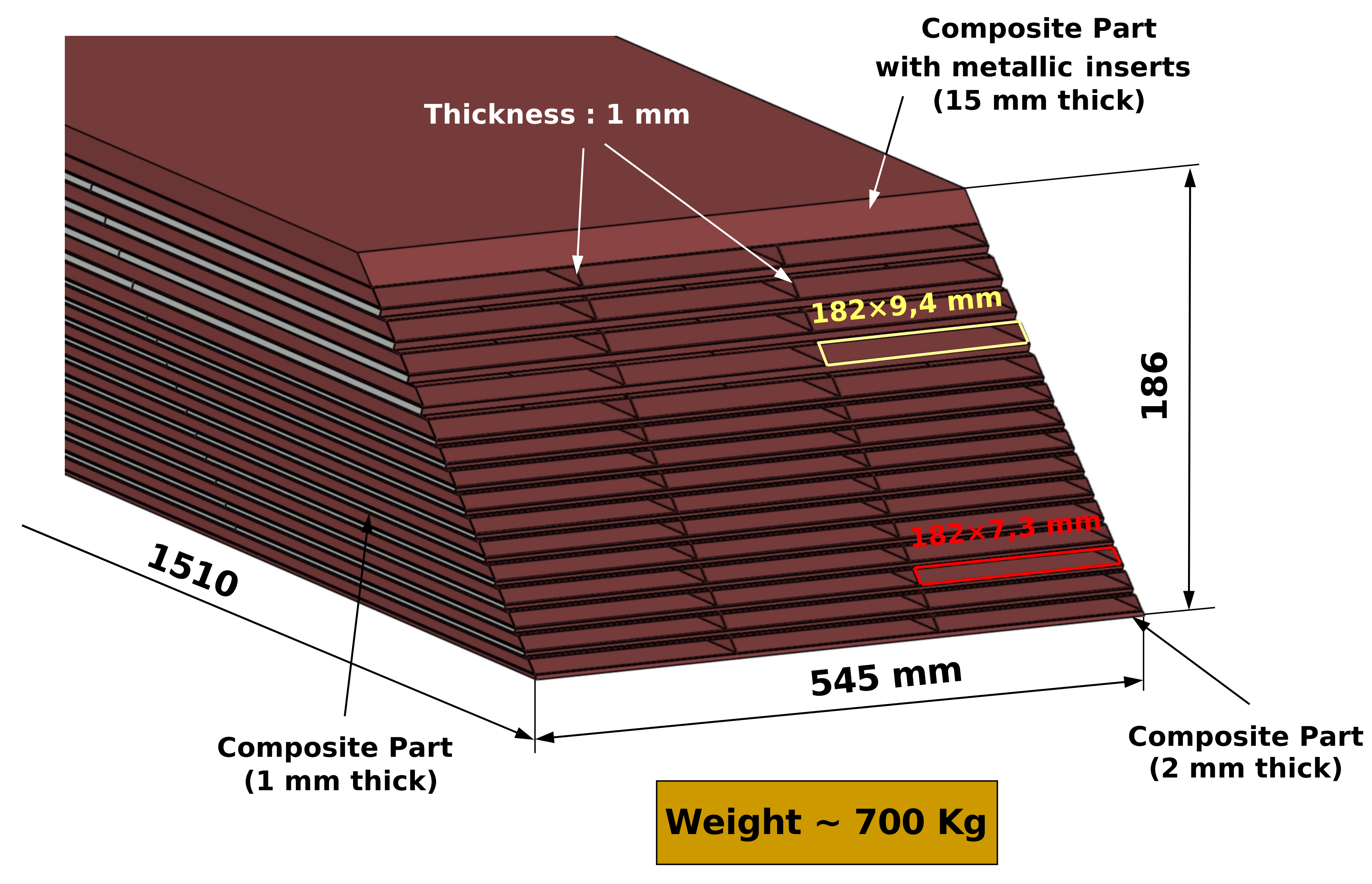
Long detector slab (1)

Complete Tower of 4 wafers = 18×18 cm²

EUDET

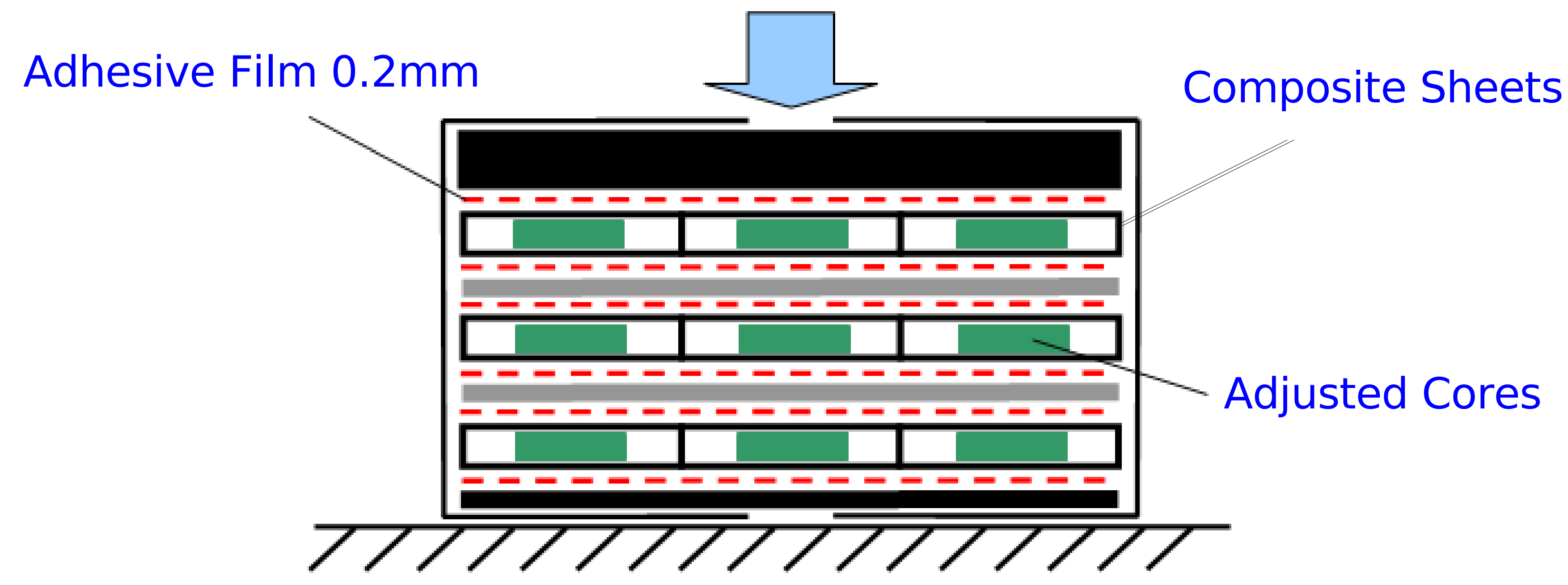
- **1 structure : ~ 23 X_0 (20×2,1mm + 9×4,2mm)**
- **sizes : 1560×545×186 mm3**
- **Thickness of slabs : 6 mm (W=2,1mm)**
- **VFE inside detector**
- **Number of channels : 45360 (5×5 mm²)**
- **Weight : ~ 700 Kg**

Alveolar Structure



Weight ~ 700 Kg

Assembly Mould for Alveolar Structure

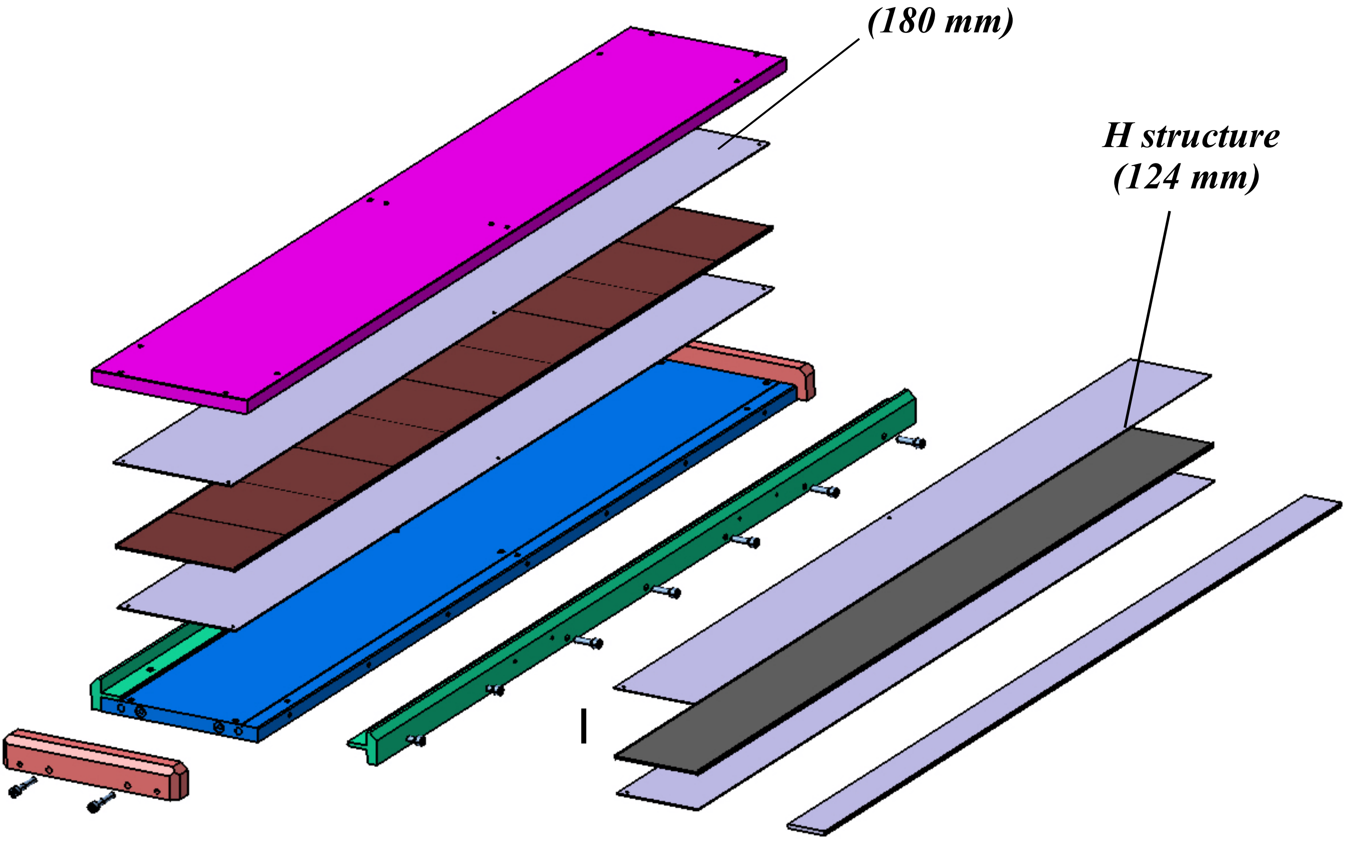


- Not entirely fixed but well advanced
- Issues: prevent damage to composite sheets
  Protect shape of alveoli – e.g. Insertion of Aluminium Dummies

Composite H Structure

Study and manufacturing of one mould for whole structures (feb 2008):

- Same principle than the mould used to do H physical prototype structures (autoclave)
- One long mould for both long and short H structures and 2 width (124 and 180 mm)



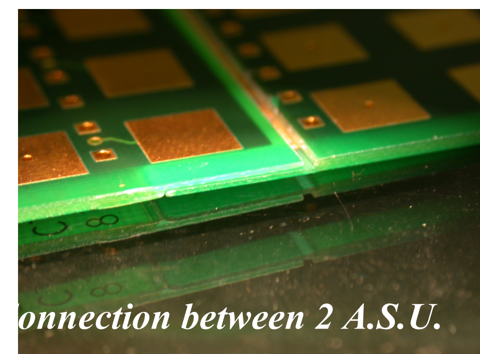
EUDET Milestone report on moulds and structures by end of June

Detector Slab Principle

Long slab is made by several short PCBs :

A.S.U. : Active Sensors Unit

- Unity of FE Chips and PCB (see later)
- Design of one interconnection « **inside** » PCB
- Easier development : study, integration and tests of A.S.U in parallel with other components of the project
- The length of each long slab will be obtained from the size of one "final PCB"



3330 ± 20
4900
900
450
89600
89960 ± 40
Back Side:
Common Anode(All metalization)
780 ± 20
1230± 20
Guard Ring P
PIXEL Size (4000 x 4000)
PIXEL Signal PAD (3800 x 3

wafer
180.5
180.5
Interconnection zone

Design of Slab – Cross Section

The expected alveolar thicknesses are 7.3 mm and 9.4mm:

Chip without packaging

Heat shield: 100+400 µm (copper)

PCB: 1200 µm
Embedded FEE

6000 µm !!

glue: 75 µm

Kapton ® film: 100 µm

wafer: 325 µm

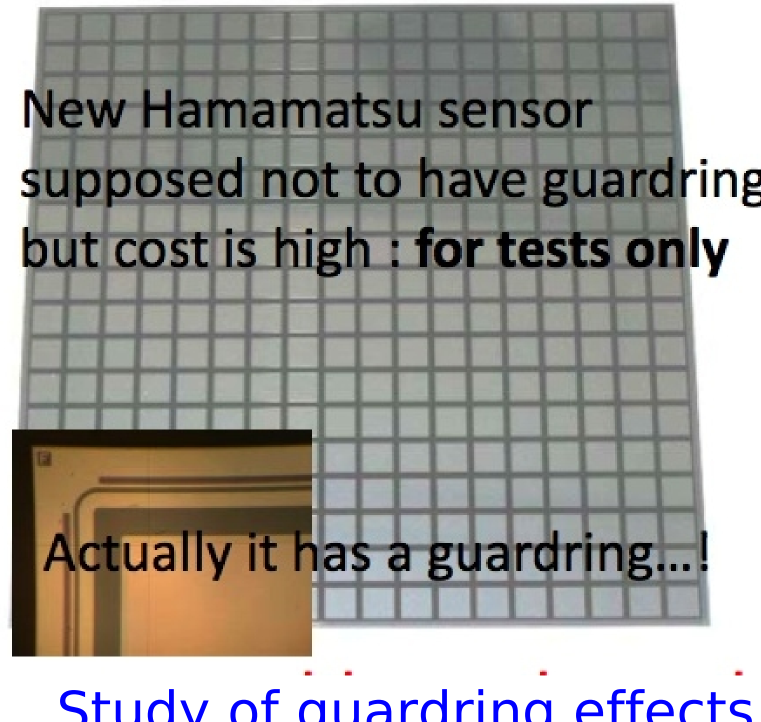
Chips and bonded wires inside the PCB

- Design of Layout fixed during summer 2008 (compare e.g. Talk at ECFA08)
- Compactness limited by PCB Thickness
- Dimensions are results of dedicated studies

Si Wafers

- 30 Wafers arrived from Hamamatsu

  - 90x90mm2 wafers for 324 cells per wafer
  - 5x5 cell size
  => 324 Cells/wafer



- Immediate start of Characterisation
  - Leakage Current (I-V curves)
  - Full depletion Voltage (C-V Curve)
  - 29/30 Wafers are found to be ok

Study of guardring effects within EUDET Project

- Can be used to test gluing with 'real' wafers

- Net Conclusion: Type of Wafers can be used for EUDET Prototype
  However, continue to study proposals by other manufacturers

Hamamatsu wafers : simulation

C(V,t) ⇔ C(V,Q) and Q(t) ?

The variation of a surface charge density Qs lead to a similar behavior as for the time evolving measurements : the effective C(V) could depend on Qs.

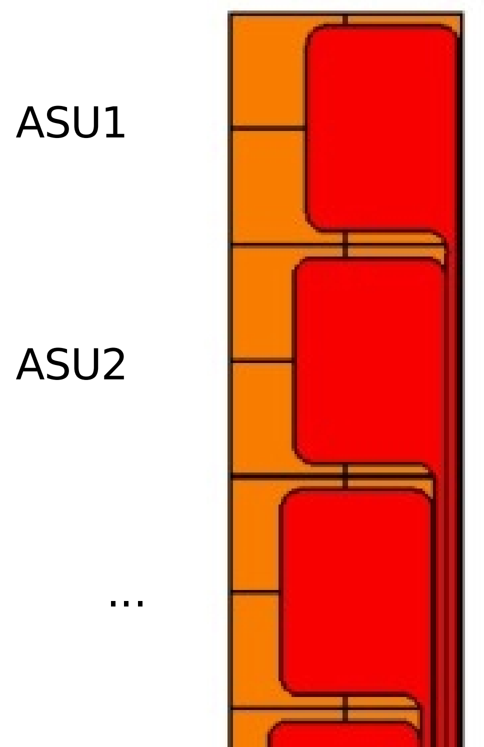
Typically, interstitial defects create trap states filled according to the time (diffusion process : exp law). Trapped charge then compensate a initial charge due to the deposition process of the materials.

Qs=Qi+Qt(1-e(-t/tau))

Charge Density effect demands to bias Wafers ~ 1 hour before usage but then ok ... .

HV Distribution to Si Wafers

Wafers have to be supplied with ~150 – 200 V Bias Voltage



- Only ~100 µm space for HV distribution

- PCB/Film based on a polyimide substrate (Kapton) allows for thin distribution system
  - conductive and insulating layer within specs

- Film must allow for disassembly

=> Individual supply for each Wafer needed

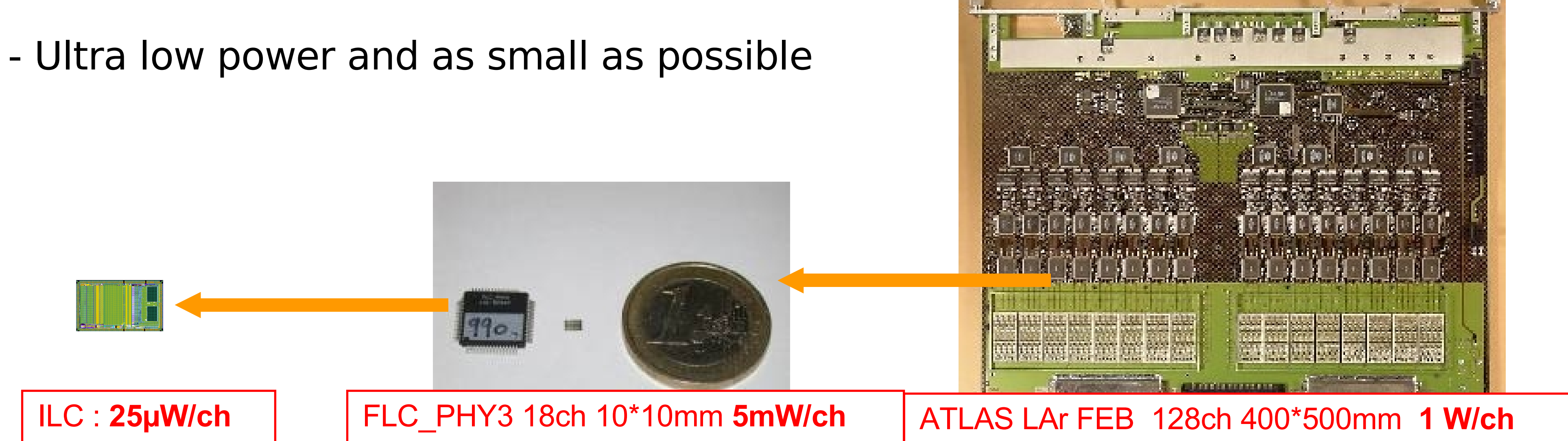
Flag shaped film is baseline solution
simple flat film also under consideration

- Connection to Power supply made on DIF side
- Length of film (~1.5m) is beyond industrial standards
  Companies have been contacted – Expect Prototypes by end of 2008

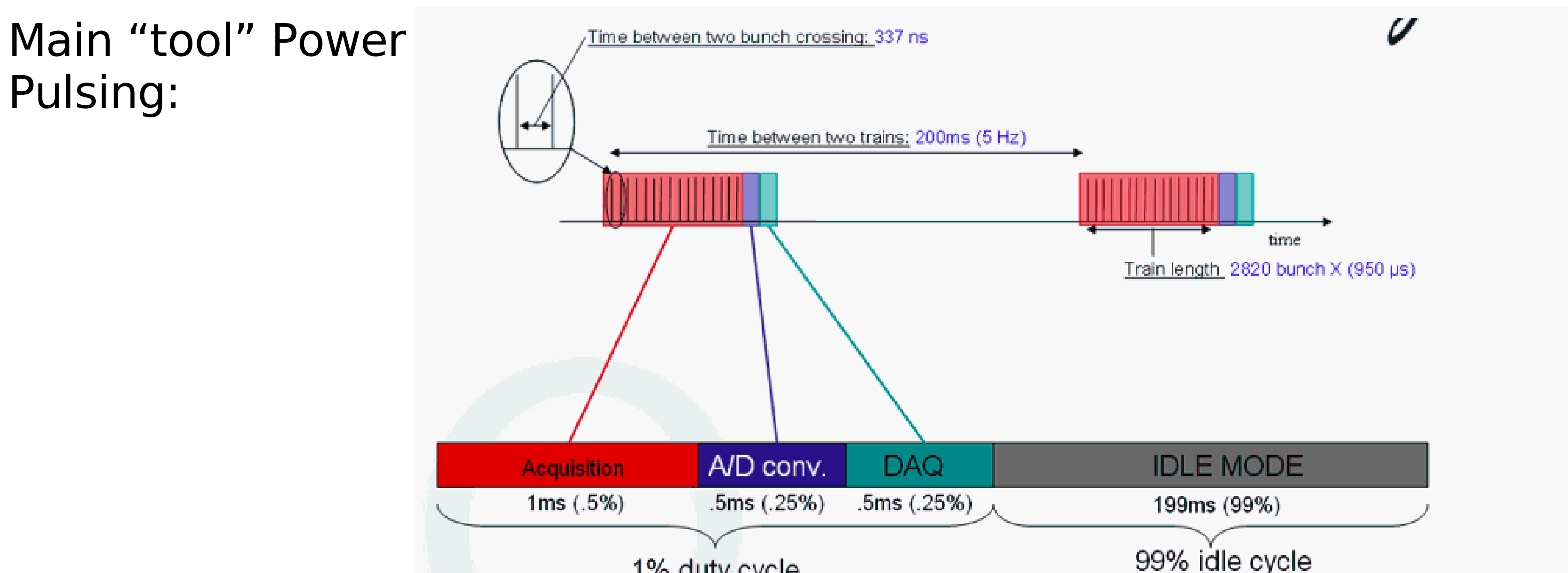
SKIROC Chip*

- Designed to read out 64 Channels => 4 Chips per Wafer

- Ultra low power and as small as possible

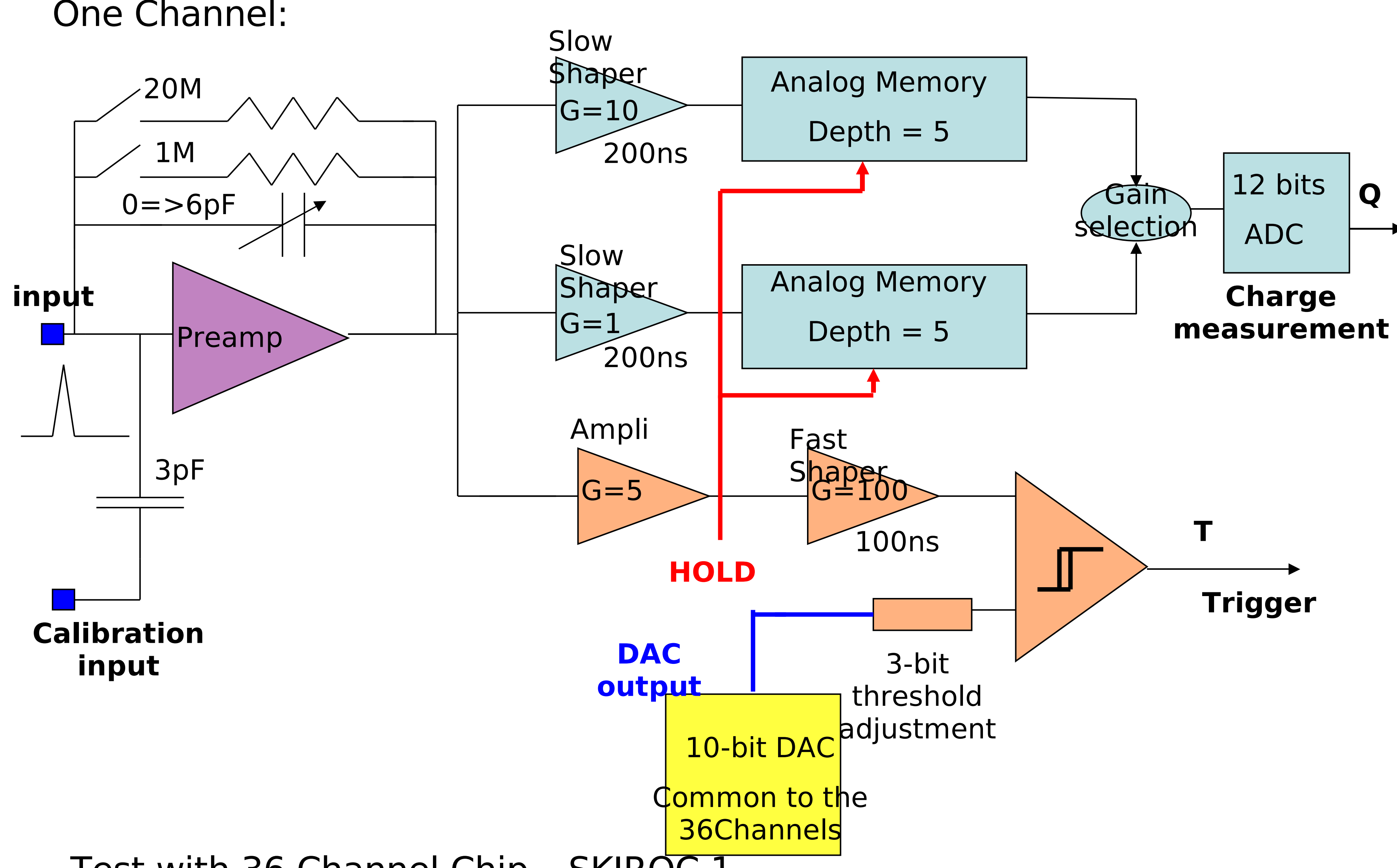


Main “tool” Power Pulsing:



*See also talk by C. de la Taille

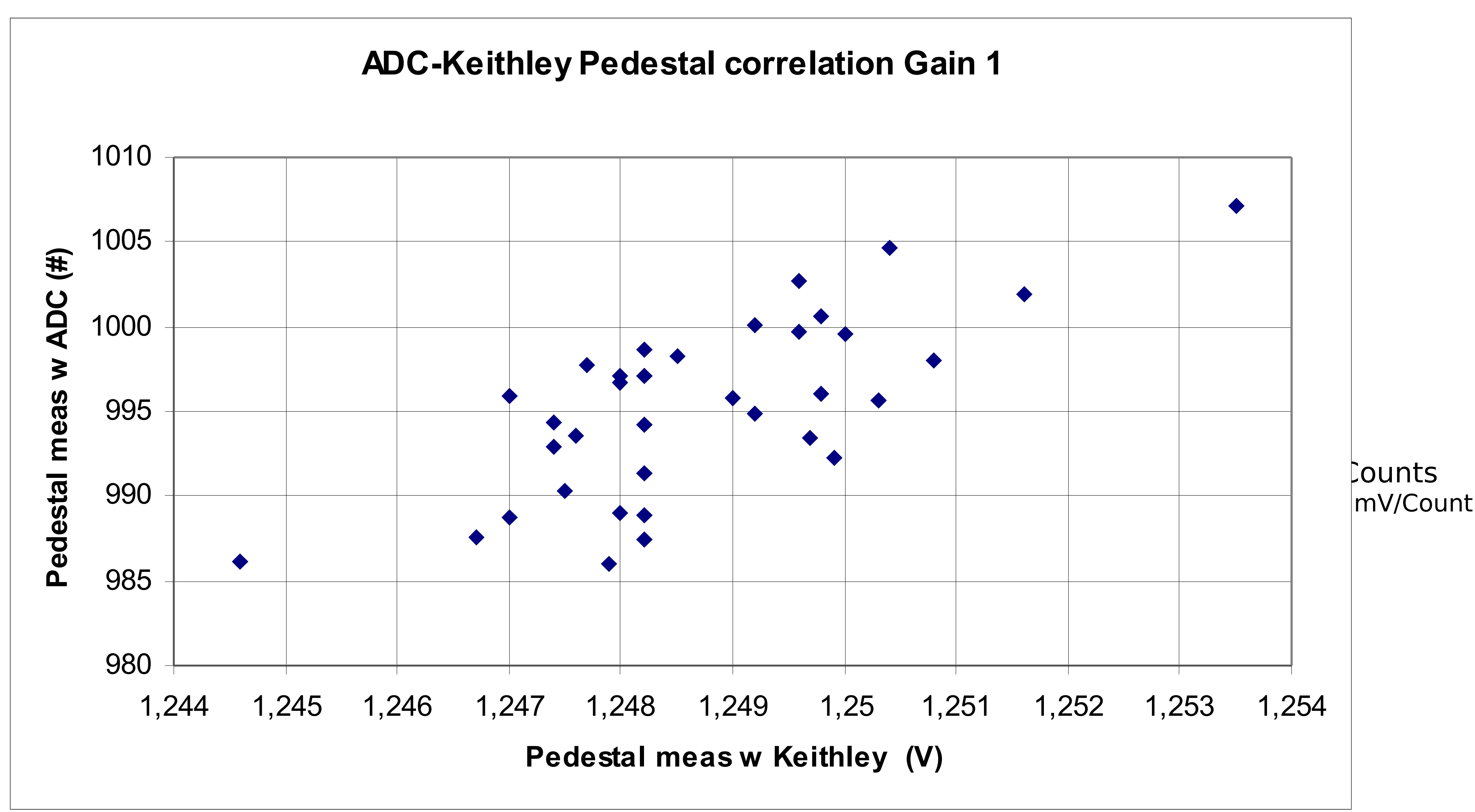
SKIROC Chip



- Test with 36 Channel Chip – SKIROC 1

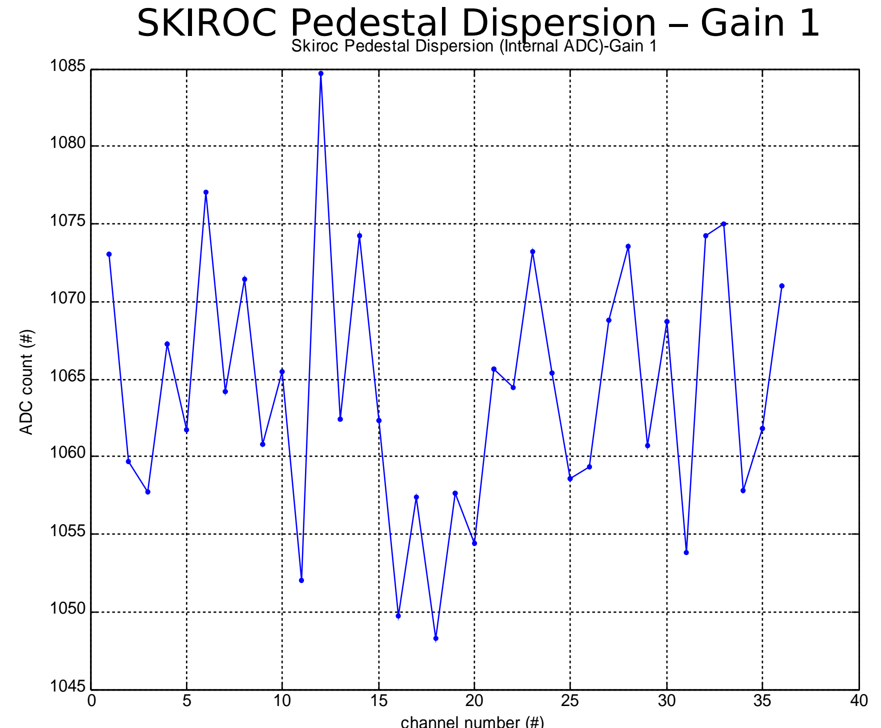
- Currently SKROC1 – SKIROC2 Submission for Production Oct. 2009

SKIROC Measurements



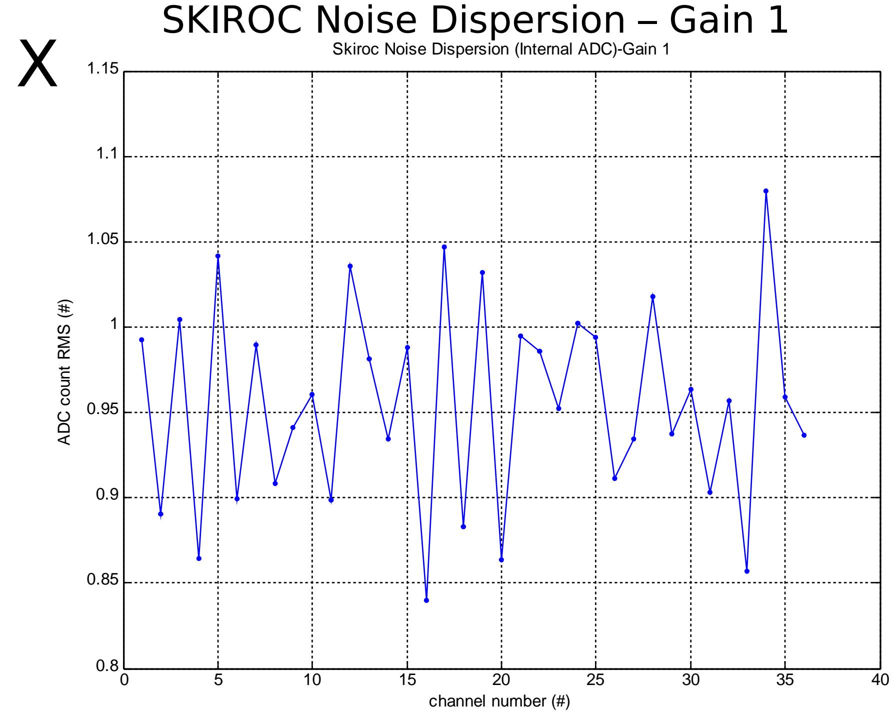
Independent measurements of pedestals compatible

SKIROC Pedestal Dispersion – Gain 1



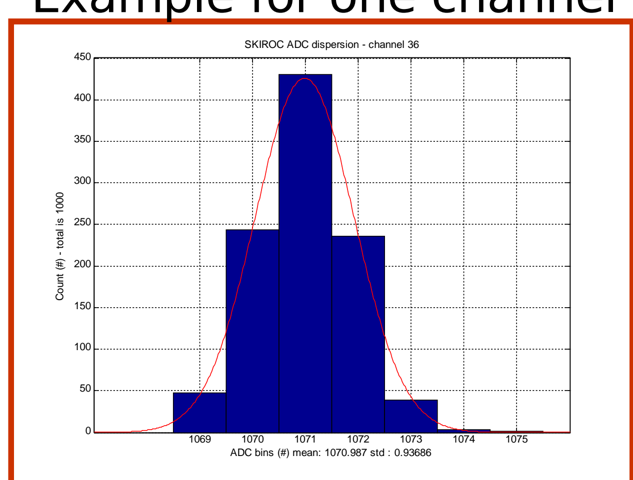
X

SKIROC Noise Dispersion – Gain 1



Random Distribution of Pedestals

Example for one channel



Gaussian Noise
~0.95 ADC Counts = 330 μ V

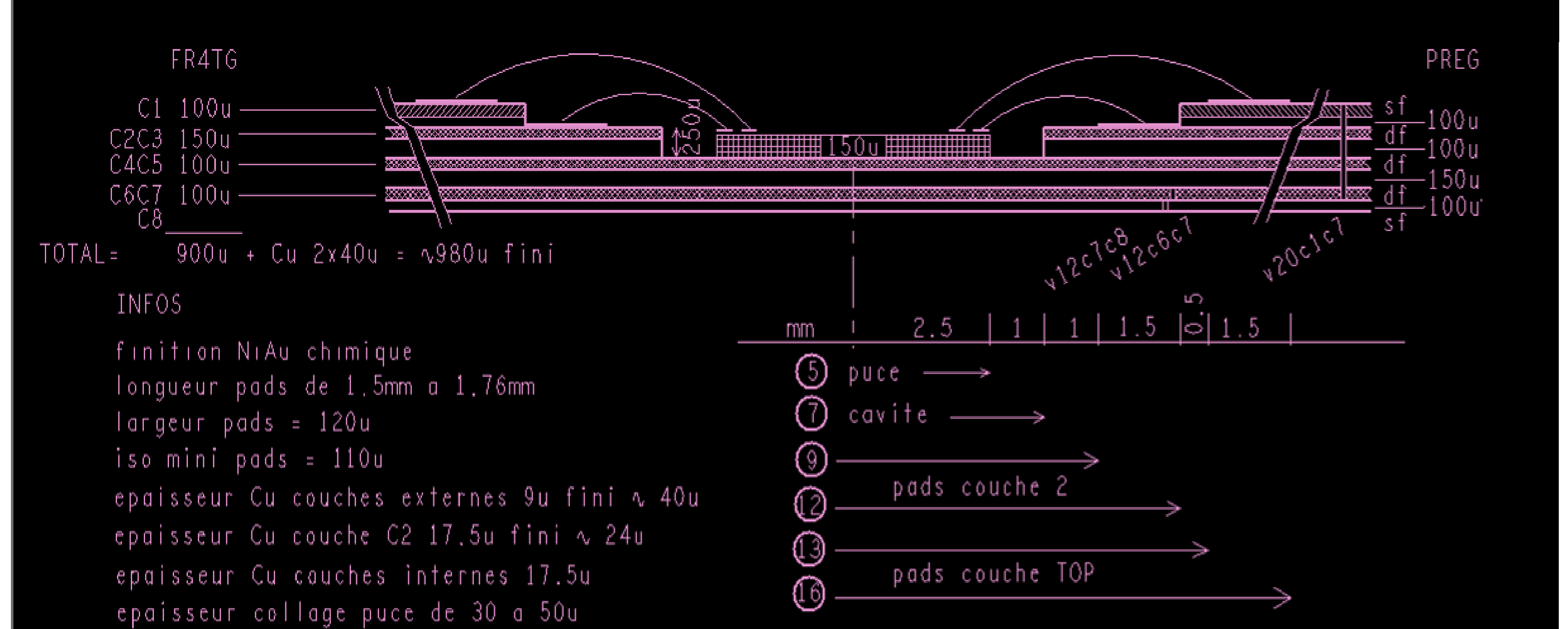
PCB Design

Pile-up

TOP	GND+routing
C2	AVDD+routing
C3	AVDD+DVDD
C4	GND + horizontal routing
C5	AVDD+ vertical routing
C6	GND+pads routing
C7	GND (pads shielding)
BOT	PADS

- Scheme envisaged for SKIROC2
- 8 layers PCB Thickness O(1mm)

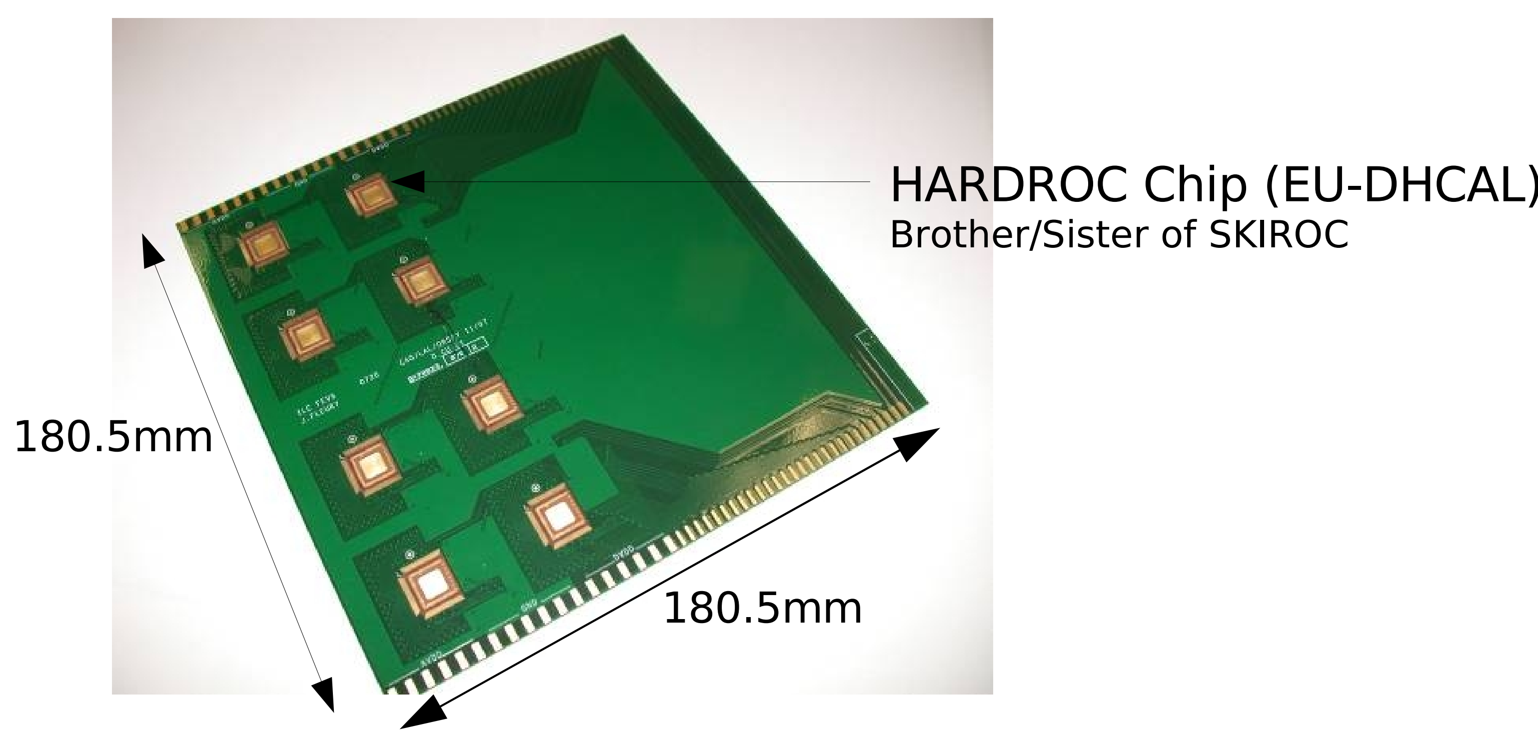
3 drilling sequences :
- Laser C7-C8 120µ filled
- Laser C6-C7 120µ
- Mechanical C1-C7



- Bonding wires from Chip to PCB challenging due to large number of channels
- Has to fit into overall mechanical tolerances (see above)

PCB Design – First Prototype FEV5

Main Purposes: - Learn how to fabricate highly compact PCBS
- Test interplay with DAQ components



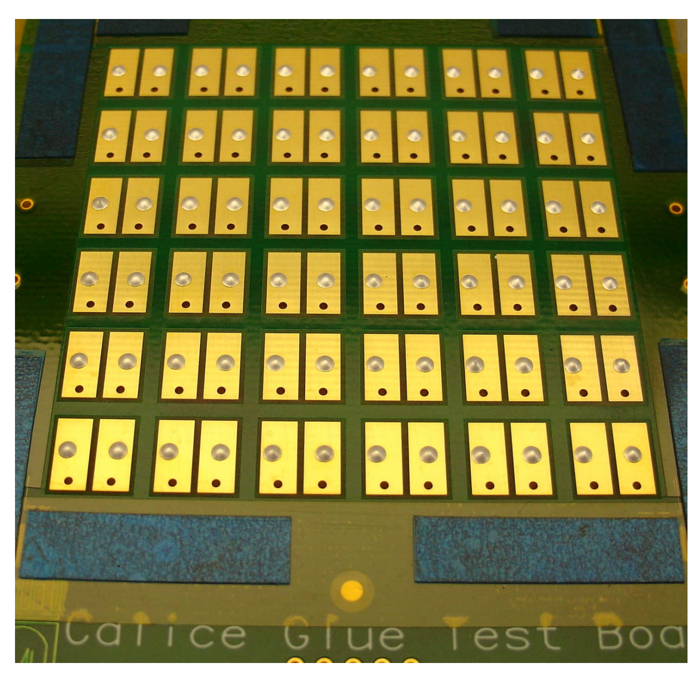
Issues: - Demand for compactness goes beyond industrial standards
- Unable to bond Chip onto PCB, lack of gold in one of the layers

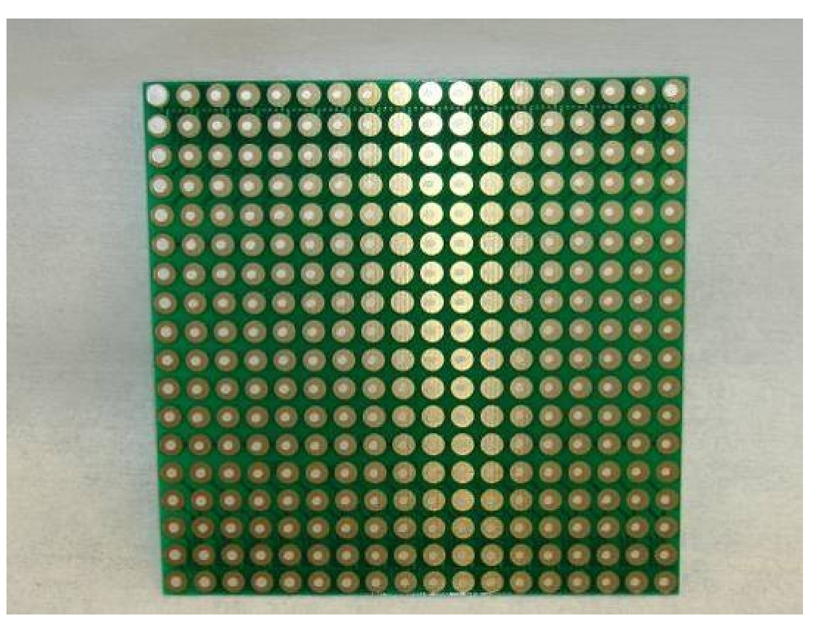
Remedy? Encouraging “contact” with Corean Groups

Interconnection between Wafers and PCB - Conducting Glue Dots

Electrical Connection by Conductive Glue – Epotek E-4110
Requirements: Thickness of Glue Dot ~ 100 µm
Diameter ~ 3mm

Glue Test Boards





Typical Values for Test Boards:

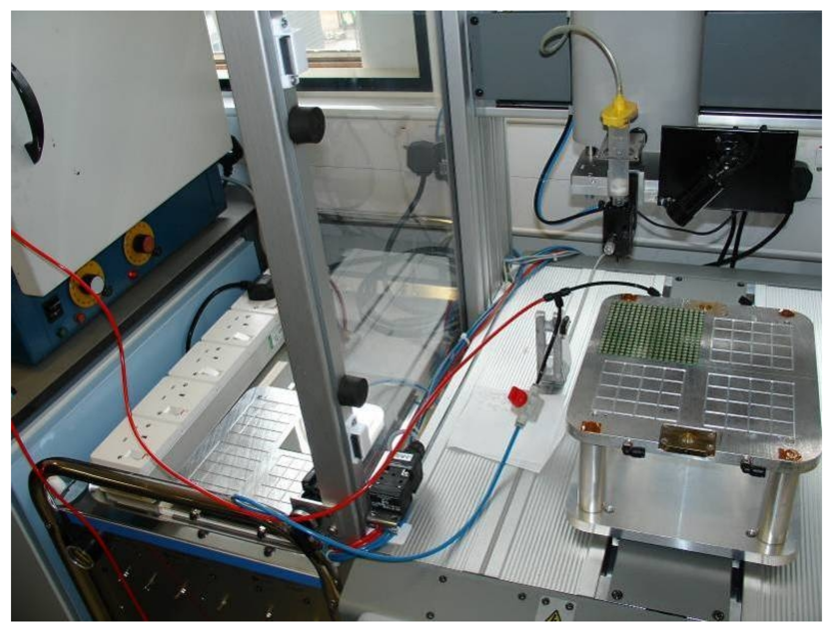
Dot Thickness: 66 µm
Dot Diameter: 3mm
$R_{Dot} < 0.005\ \Omega$

Glue Dots well within specifications – Gluing under Control

Gluing of ASUS

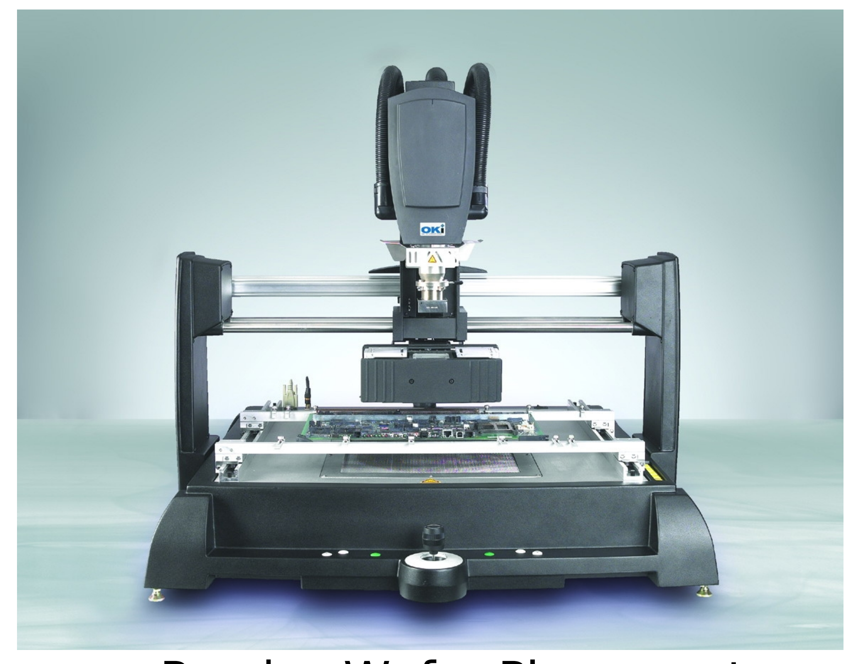
- Controlled glue dot deposition on the PCB
- The (four) Si Wafers are picked up, aligned and placed on the PCB
- Accurate thickness and planarity control via vacuum jigs
- The assembled ASU is allowed to cure

Test board with Dispenser Robot



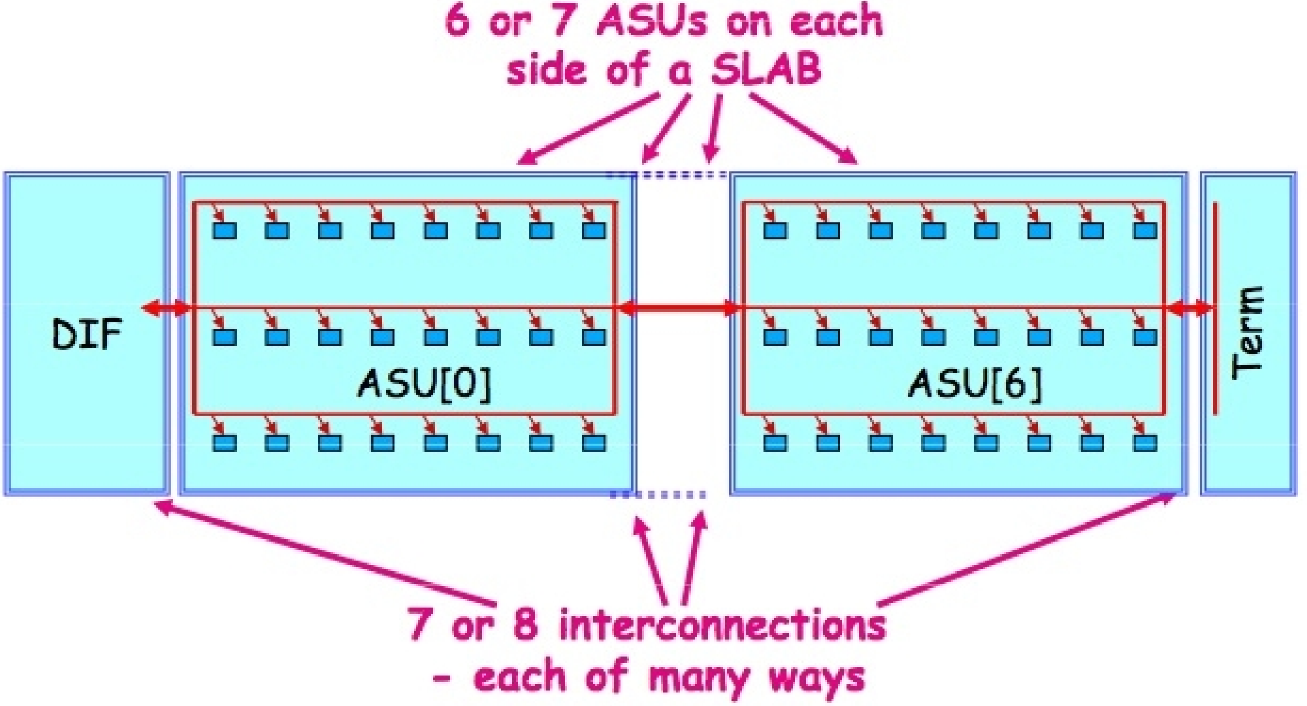
"Gluing" rate 0.4 Hz

BGA Workstation for Wafer Placement



Precise Wafer Placement
by Split Field Optics

Complete Production Chain for Automatisation of Gluing Process available



Primary Functions – Electrical Paths along length of Slab

- Low Voltage Power
- Checks and fast Control Signals
- Slow Controls via a serial path
- Data readout paths
- Monitoring signals, e.g. Temperature

Issues:

- Must not jeopardise quality of critical signals, e.g. Clocks
- Must allow for replacement of ASU

Bridge Scheme of Interconnections

FFC-Bridge
Solder
Track
800 µm
ASU
ASU

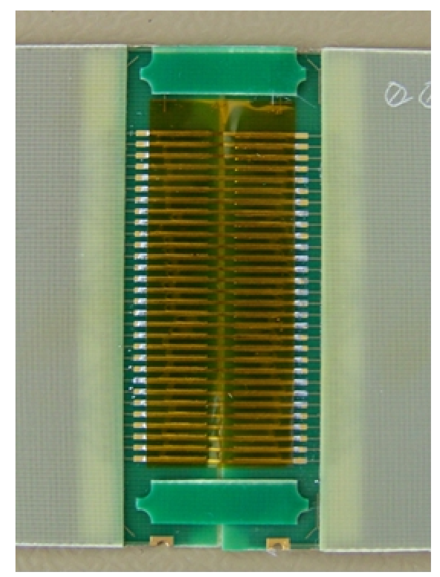
Flat Flexible Cable Bridge

PCB-Bridge
Solder
Track
800 µm
ASU
ASU

PCB Bridge

Slightly preferred scheme: FFC Bridge

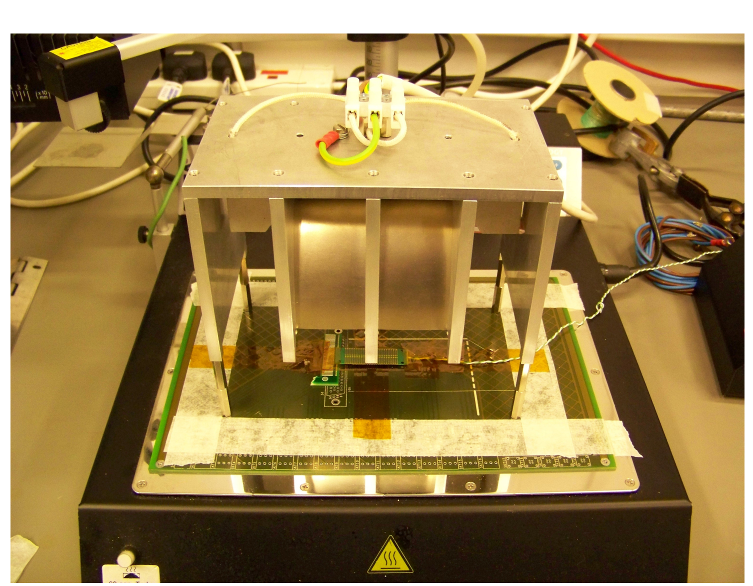
Facilitates exchange of individual ASU



Junction

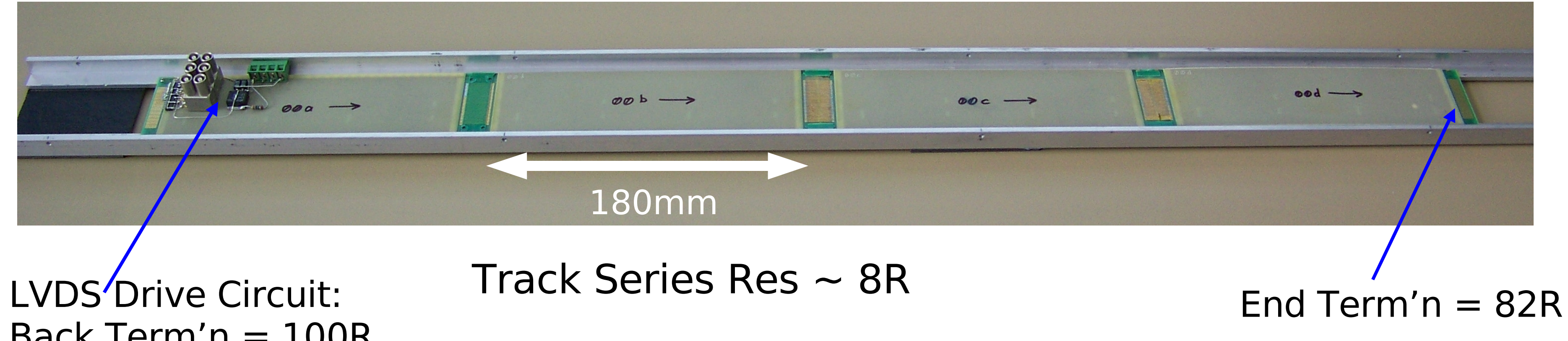
realized with …

Imaging Halogen IR Source



Signal Propagation an Cross Talk

4 Section ASU-Test Assembly



LVDS Drive Circuit:
Back Term'n = 100R

Track Series Res ~ 8R

End Term'n = 82R

(LVDS) Signal Propagation along Slab

Probes along Slab

$A_{\text{far End}}/A_{\text{near End}} \approx 80\%$

$A_{\text{near}} = 840\text{mV}$

- Reasonable small signal loss
- Cross talk O(10mV)

Slab interconnection well under control

ECAL SLAB Interconnect

DAQ Architecture – Overall view

~150 VFE ASICs on each side of SLAB

ODR

LDA

LDA

LDA

LDA

DIF — SLAB

DIF — SLAB

DIF — SLAB

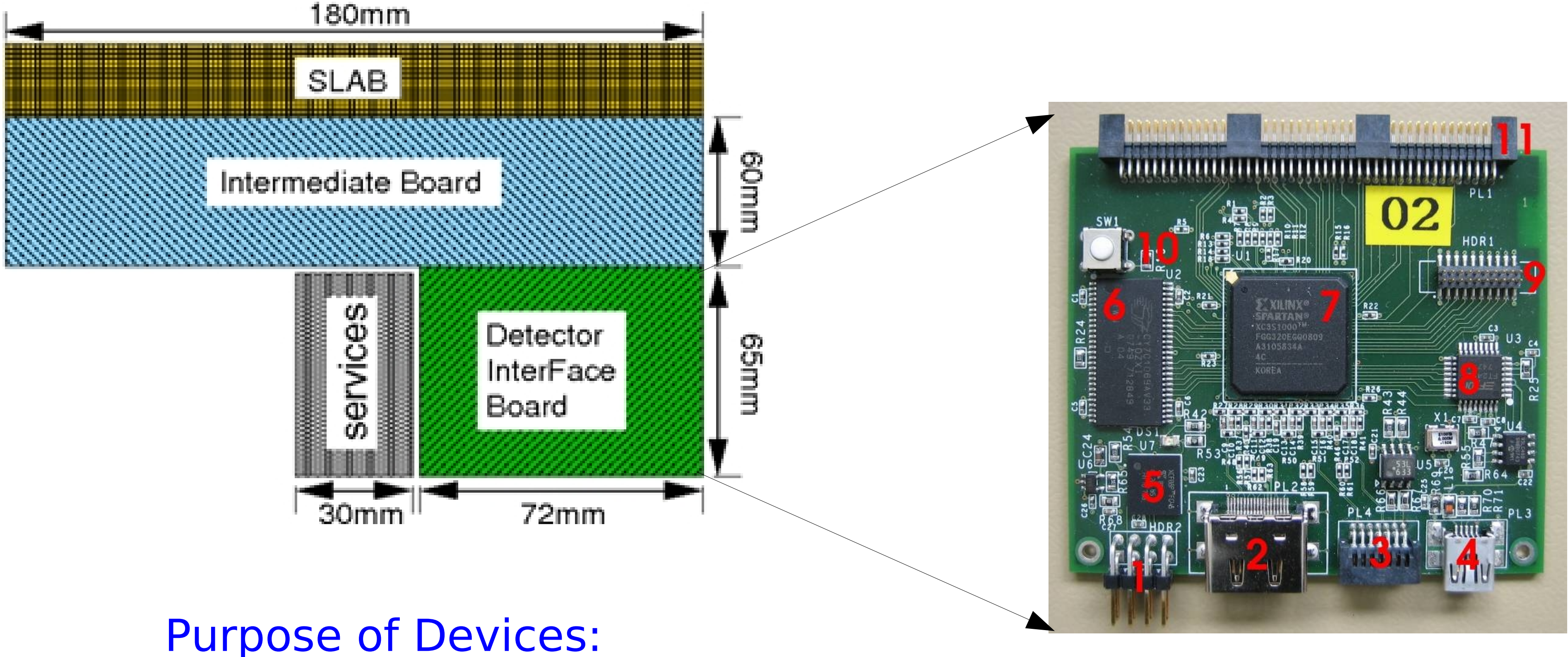
DIF — SLAB

DIF — SLAB

DIF — SLAB

Maurice Goodrick & Bart Hommels , University of Cambridge

DIF and Intermediate Board



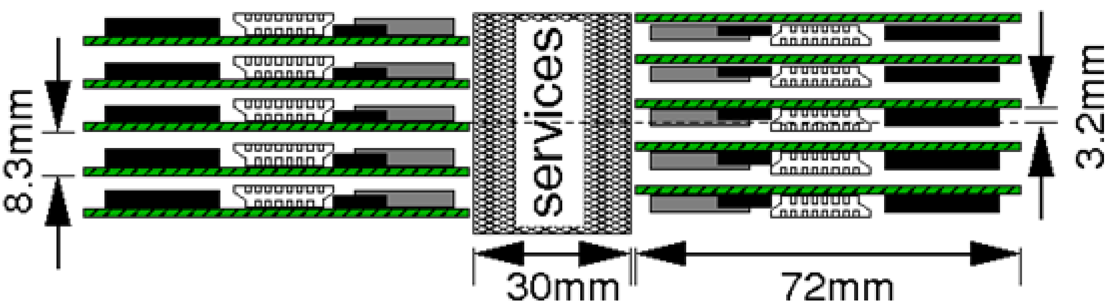
Purpose of Devices:

DIF:
- Clock and Control Signals to the VFE Chips
- Interface to DAQ

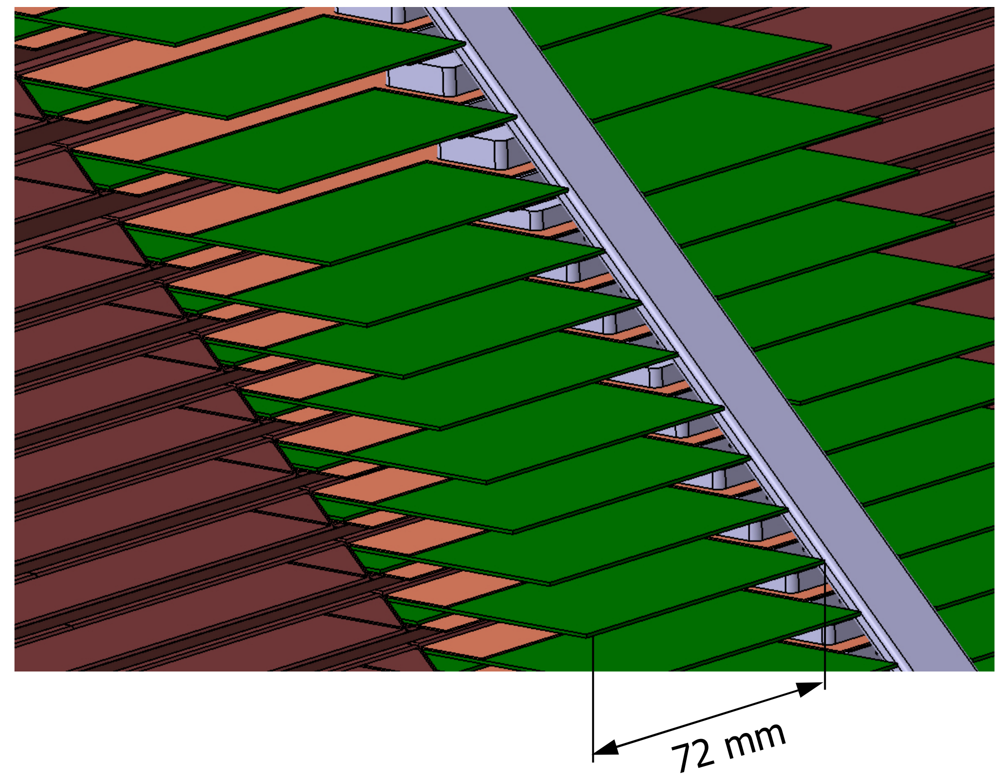
Intermediate Board:
- Interface to Slow Control and Detector Monitoring
- Power Supply Electronics

DIF and Intermediate Board - Integration

Front View

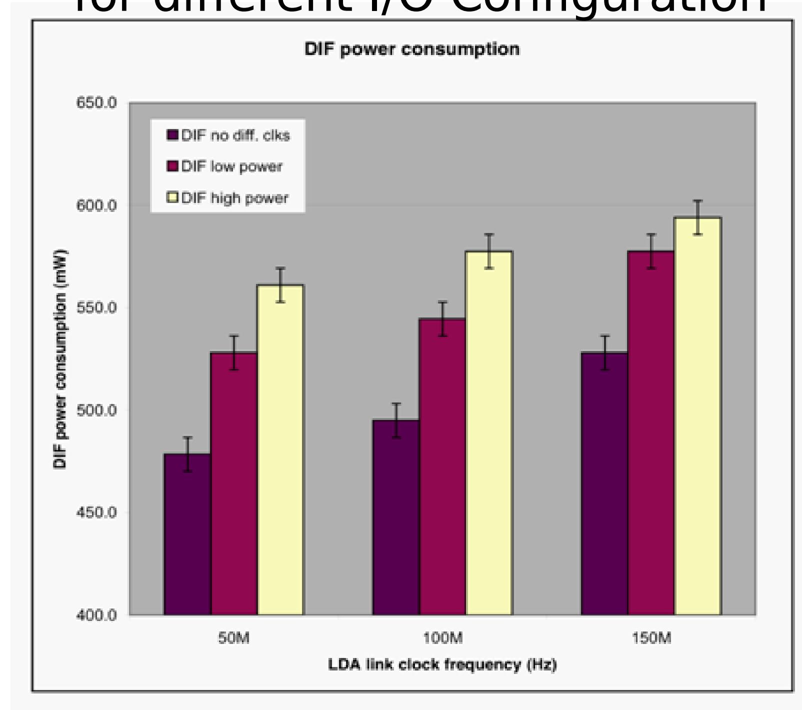


Side View



Prototype optimised for functional versatility
Space can/will be gained by removing USB h/w

DIF Power Consumption
for different I/O Configuration



- DIF Power Consumption well below 1W
- IB Consumption to be added

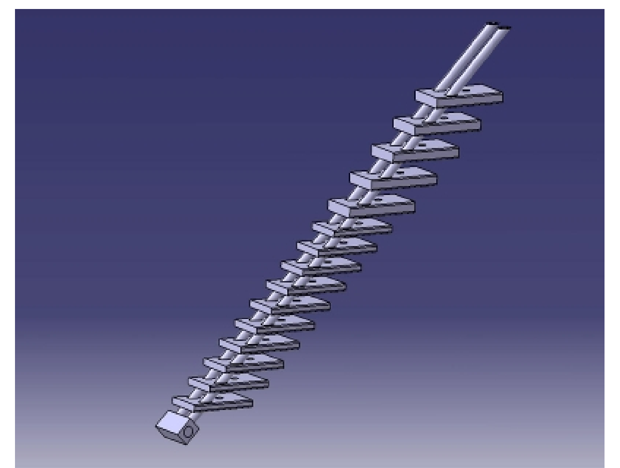
With contingency:

2W

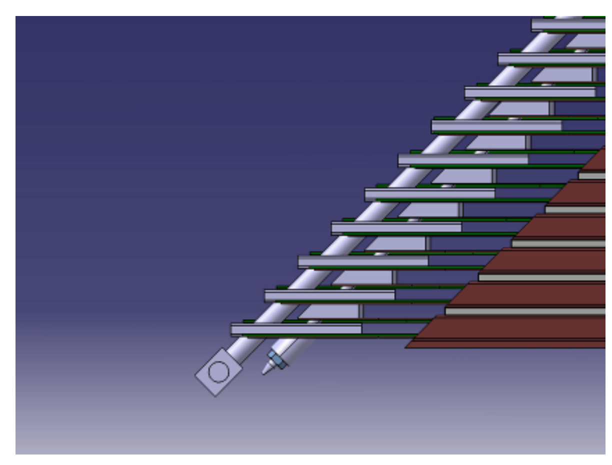
Power Cosumption of DIF/IB Combination

Cooling System

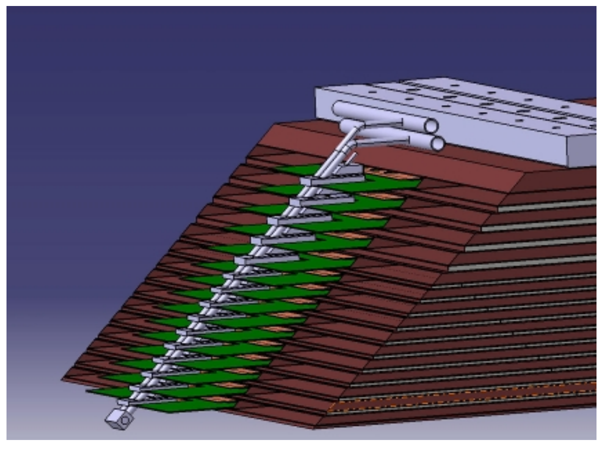
Oriented to the needs for an ILC Detector



Cooling Pipes and
Copper Bloc



Clamping to coloumns
of Slabs

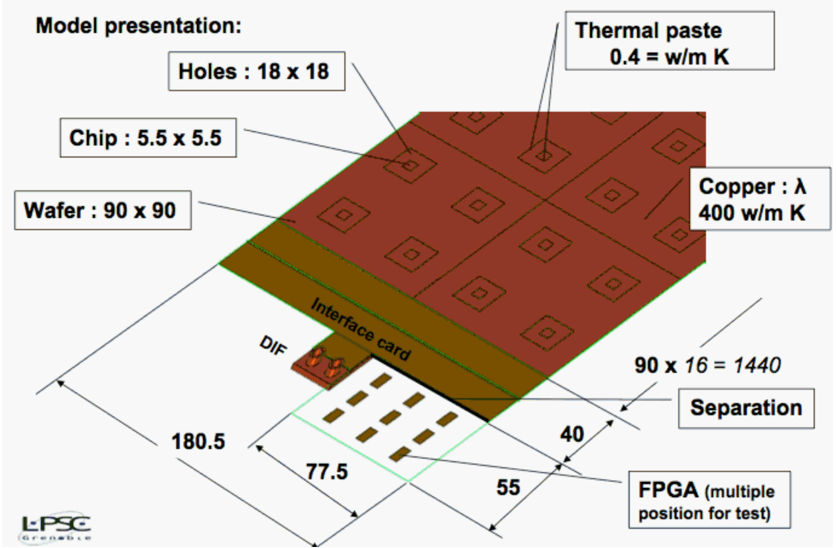


Connection to a Cooling Network

- Limited Space for Cooling System
- External Cooling Service has to cool the entire set of slabs
- Cooling System available end of September

Thermal Analysis and Heat Dissipation

Heat Evacuation from inside of the slab:
Copper Envelope (and thermal agents of top of chips)



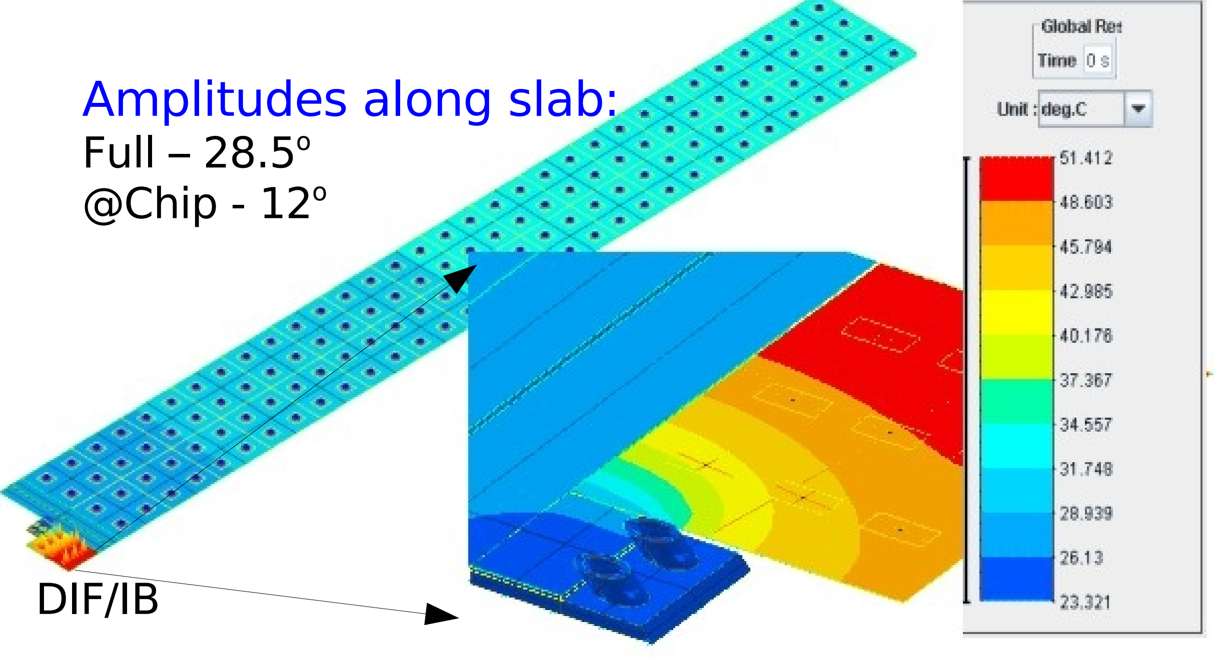
Load Case:

Wafer Power: 0.21W
DIF/IB Power: 2W
Copper Envelope: 300+100µm
Slab Length: 1.55m

Limit Conditions:

Temperature at Slab Center: 20°

$\lambda_{X\upsilon}$ = 400 W/m/K



SLAB Integration

- Thickness budget & Tolerances
- Integration Cradle & H structure Fastening
- HV Kapton & ASU insertion + interconnection
- Copper Shield & Housing installation
- DIF plugging with possible clamping to Cu shield
- SLAB Link to Cooling device & Electronic Setup
- SLAB ready to Electronic Qualification Tests at operating temperature (inside alveolar sector)

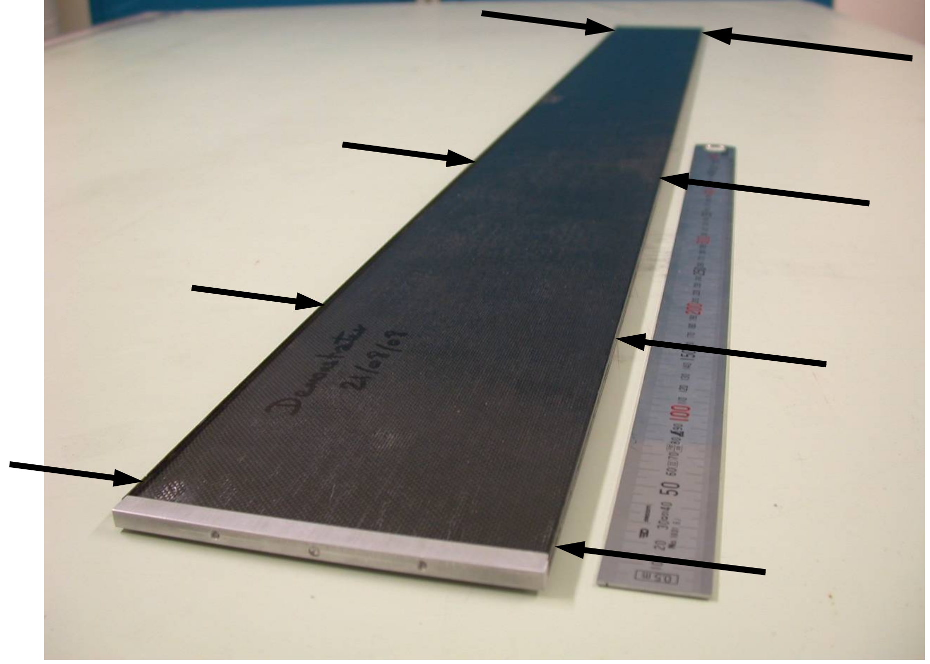
Integration Cradle and H Structure Fastening

⇨ Aluminum Rectangular Frame : fully adapted to H structure with free access to detector sensitive components {HV feeding, ASU + Terminal Boards} & Copper shielding parts.

- Lateral fastening of H structure to integration cradle {adequate screws + rubber ends on few locations along opposite H edges}
- Adjustment of the straight alignment between H structure and integration cradle line {giving common reference of slab components & proximity parts (cooling device, external supports etc…}
- Connection of 2 stable bearings to integration cradle ends {allowing 180° up side down tilt of the assembly}
- Allocation of large workshop to realise

  Construction of EUDET module

  (and beyond)



Summary and Conclusion

- EUDET Prototype is logical continuation of CALICE SiW Ecal Prototype

- Next steps towards ILC Detector Module
  - Addresses technological challenges of detector construction
  - Large scale integration
  - Power consumption

- Most of the items of the construction process are under control

- Electronics is extremely challenging
  - Analog and digital part on one chip
  - Limited space for PCB

- Design Phase concluded
  - EUDET Memo published

- Start of construction phase
  - Ordering of materiel with fiscal year 08 (as much as possible)
  - First step towards EUDET Module – The Demonstrator

First EUDET Prototype – The Demonstrator

Roman Pöschl
LAL Orsay

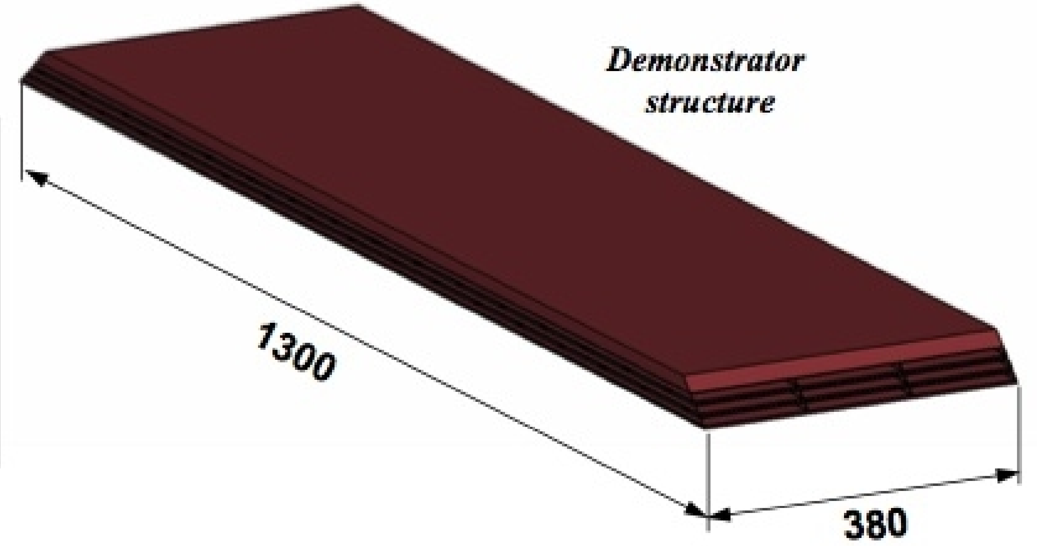
On behalf of the EUDET Ecal consortium

EUDET Annual Meeting NIKHEF Amsterdam/Netherlands Oct.

Demonstrator design

- We plan to build a first small demonstrator to validate all process before the EUDET module
- Dimensions based on physic prototype (cells width : 124 mm)
  - ➡ need to validate all Eudet dimensions !!!
- Could be used for thermal studies and analysis : design of a thermal PCB and cooling system.

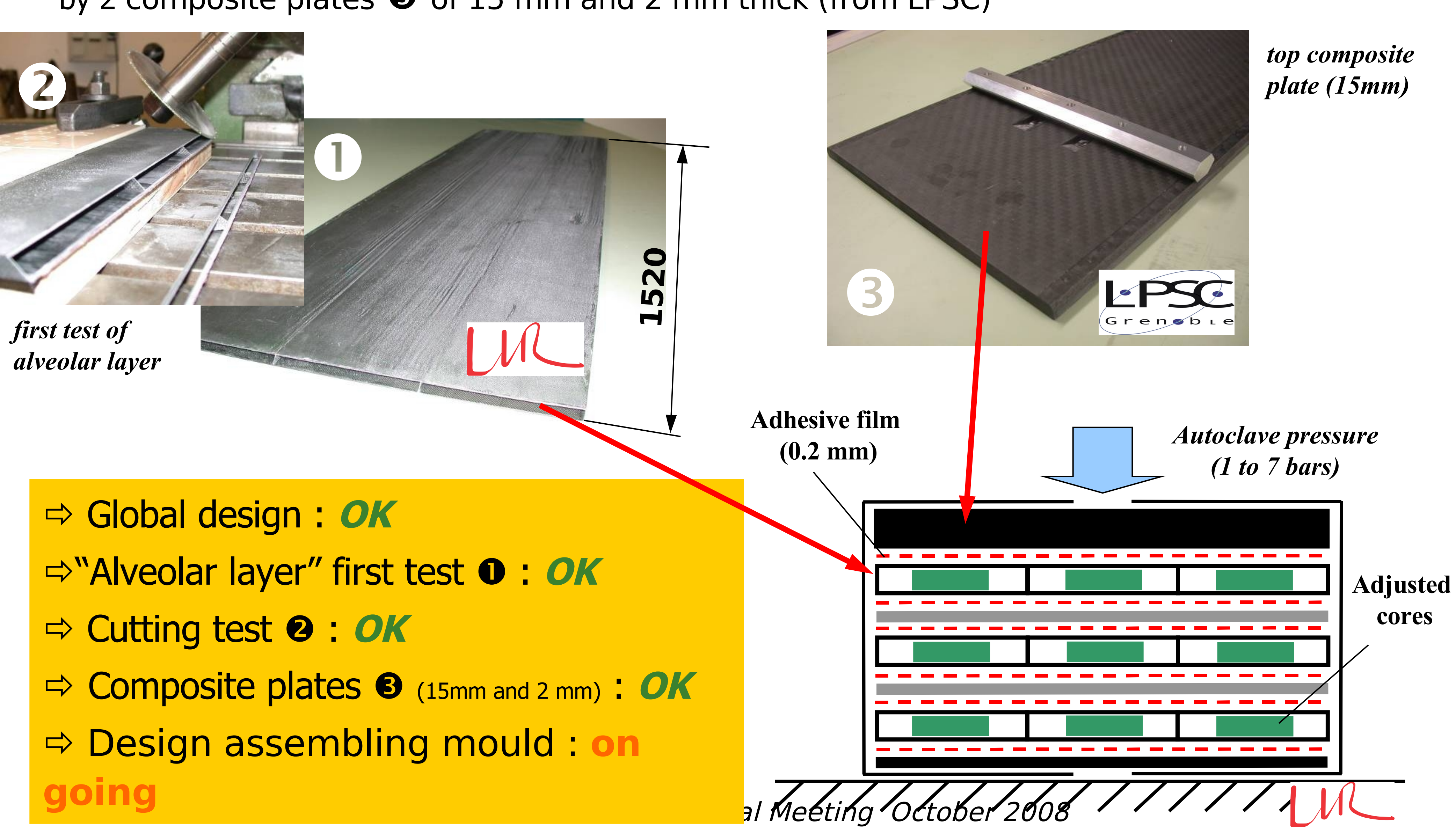
- 3 alveolar layers + 2 W layers
- 3 columns of cells : representative cells in the middle of the structure
- Thermal studies support
- Width of cells : 124 mm
- Identical global length : 1.3m and shape (trapezoidal)
- Fastening system ECAL/HCAL



M.Anduze, LLR

Demonstrator – Alveolar structure

Assembled structure : Each alveolar layer ❶ are done independently , cut to the right length and angle (❷) and bonded alternatively with W plates in a second curing step. The assembling is closed by 2 composite plates ❸ of 15 mm and 2 mm thick (from LPSC)



Demonstrator - H structure

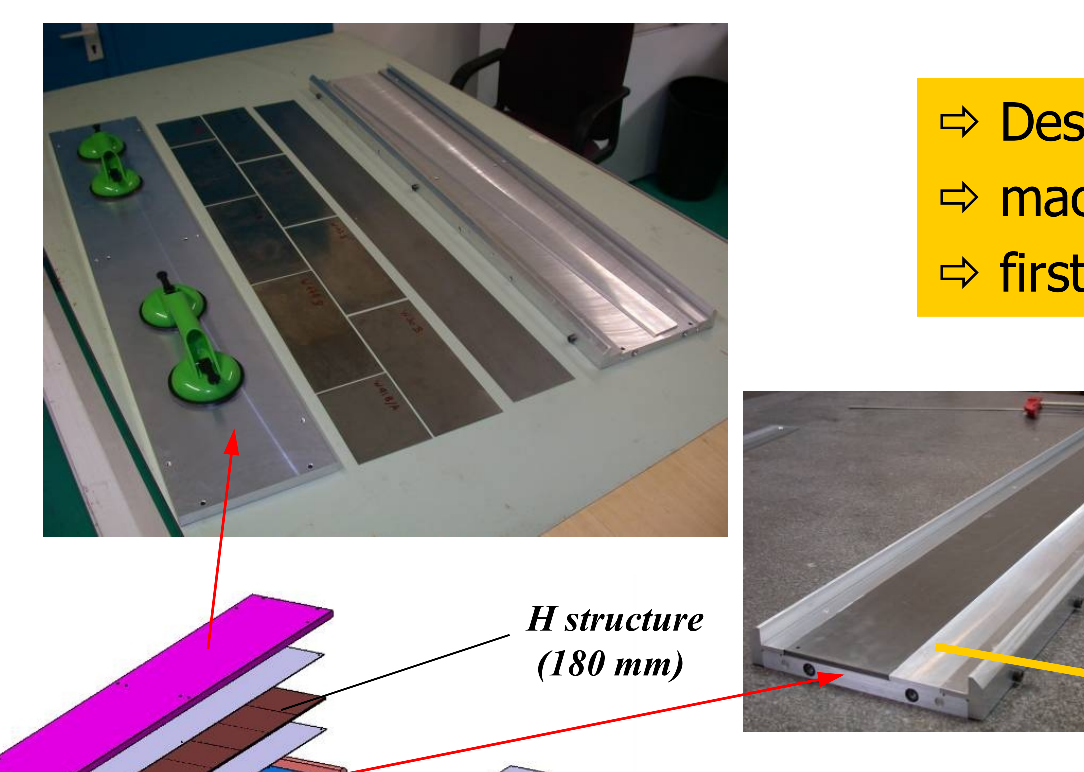
Study of one mould for whole structures:

- Same principle than the mould used to do H physical prototype structures but using the autoclave)
- One long mould for both long and short H structures and 2 width (124 and 180 mm)

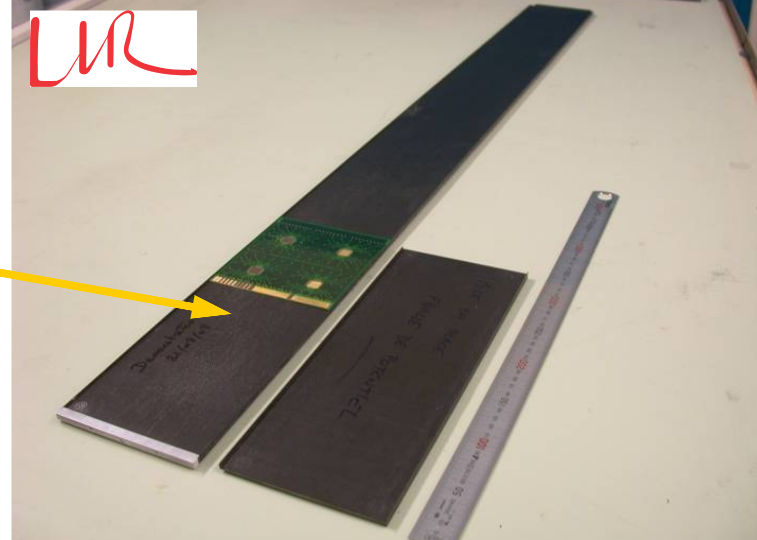
⇨ Design : ***OK***

⇨ machining : ***OK***

⇨ first H structure (1300×124): ***OK***

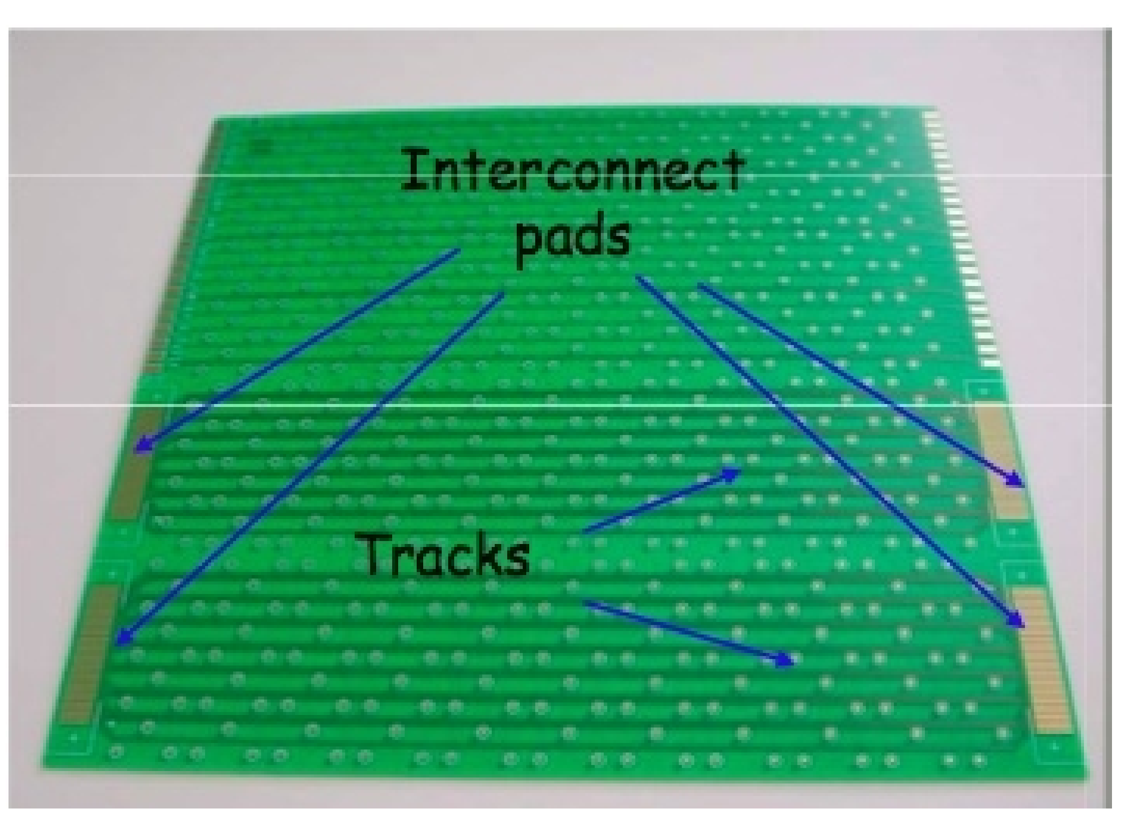


H structure
(126 mm)



PCB/"ASU" for Demonstrator

FEV6



- Simple PCB allowing for

Studying mechanical rigidity

Gluing onto glass plates

Interconnection of ASU

Heat Dissipation

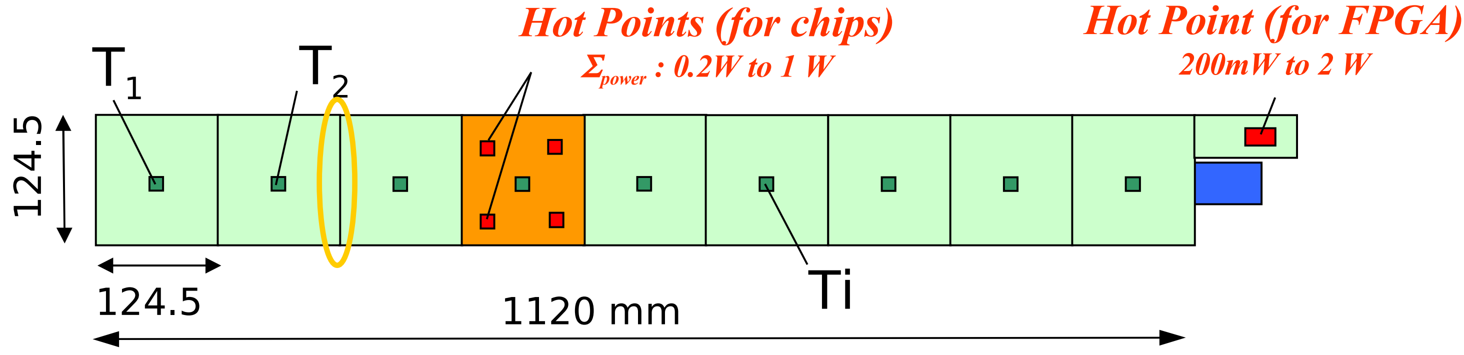
Mastering all the construction step
decribed previously

Rather an imitation than a real PCB

Demonstrator – Thermal studies

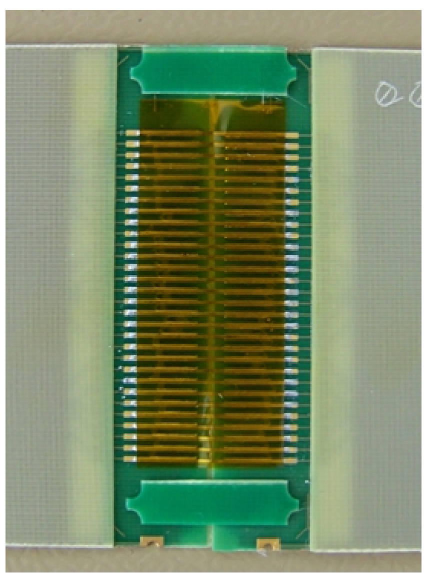
Slab cooling tests (1 Hot ASU + 8 thermal ASU):

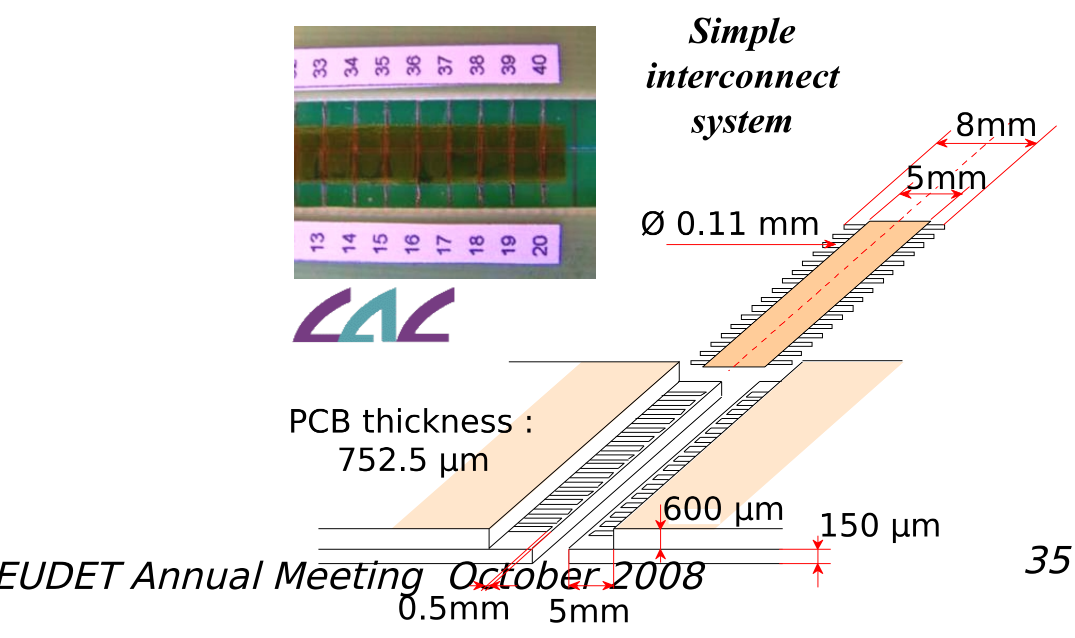
- Check a thermal dissipation behaviour close to EUDET design



Interconnections

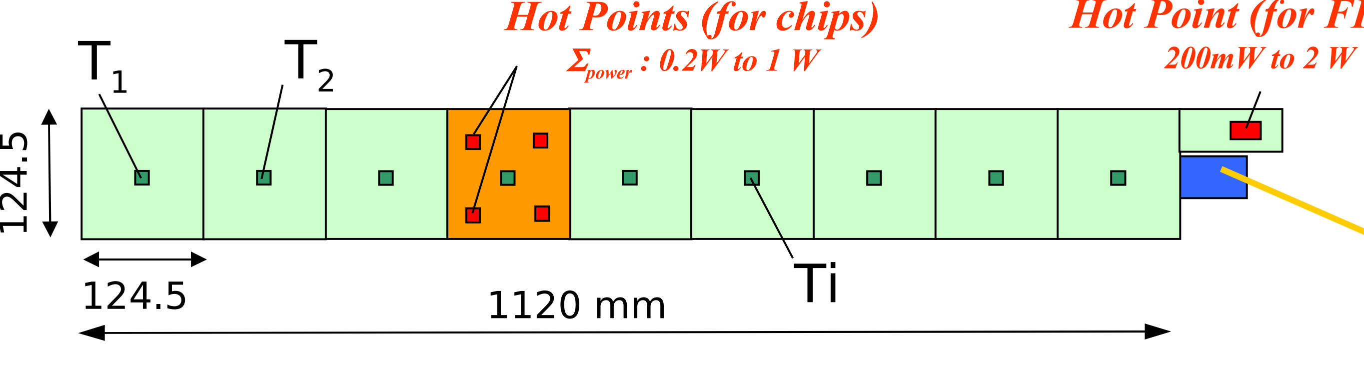
FFC (see above)



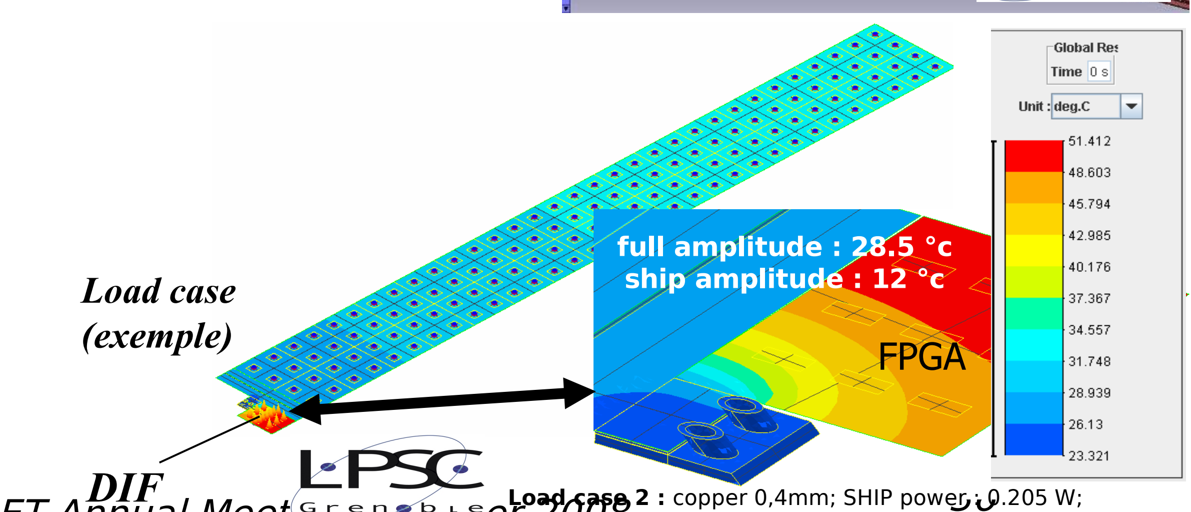


Demonstrator – Thermal studies

- Correlation with simulations (transfer coefficients, contacts …)
- Validate the cooling system (400 µm copper plate drain + pipes)



⇨ Design : OK
⇨ Simulations : OK
⇨ PCB : on going (ordered)
⇨ Copper plate : OK
⇨ Interconnect : on going
⇨ Exp. setup : on going



Demonstrator – Integration Process

- Studying handling difficulties caused of extreme fragile slabs

- Simplified Integration Cradle with vacuum pads tooling

- Handling and placing of HV feeding inside H Structure

- Cleaning of copper envelope in ultrasonic bath

  150 l
  Temperature range 30-85° C
  Transducer Power 3600 W
  Frequency 35-150 kHz

- Brazing techniques (Brazing under vacuum)

  low temperature domain (~240°C)
  high temperature (760°C)

Conclusion and Outlook

- Demonstrator consitutes important step towards EUDET Module
  - Allows for studying and validating all mechanical aspects
  - ... by reusing existing material

Major part of JRA3 EUDET Deliverable

- Most of pieces already manufactured or ordered

- Ideal opportunity to establish production chain
  - All parts of production will be examined

Results expected in January 2009

Backup Slides ...

Parties Involved

6 Laboratories are sharing out tasks in according to preferences and localization:

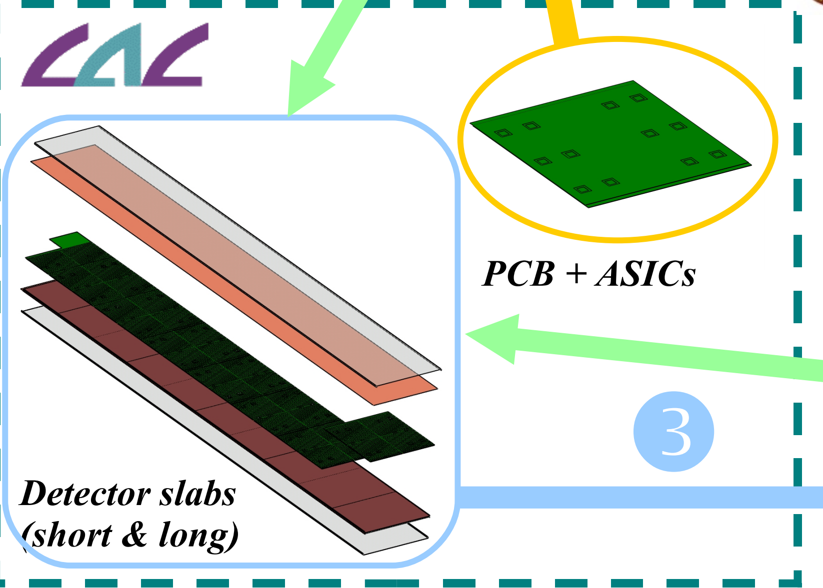
Assembling of A.S.U. (industrialization, gluing and tests) + backend system (DIF support) + services

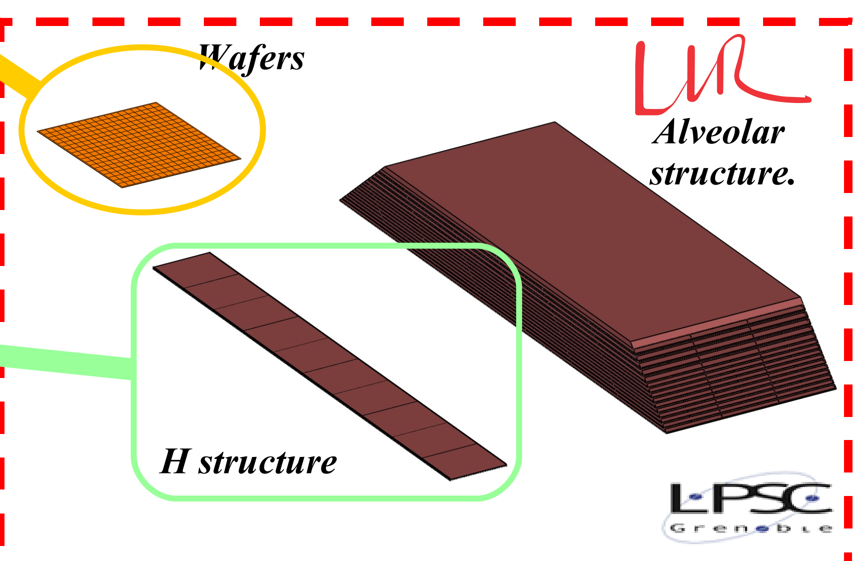
Tests of wafers
Global Design + composite Structures

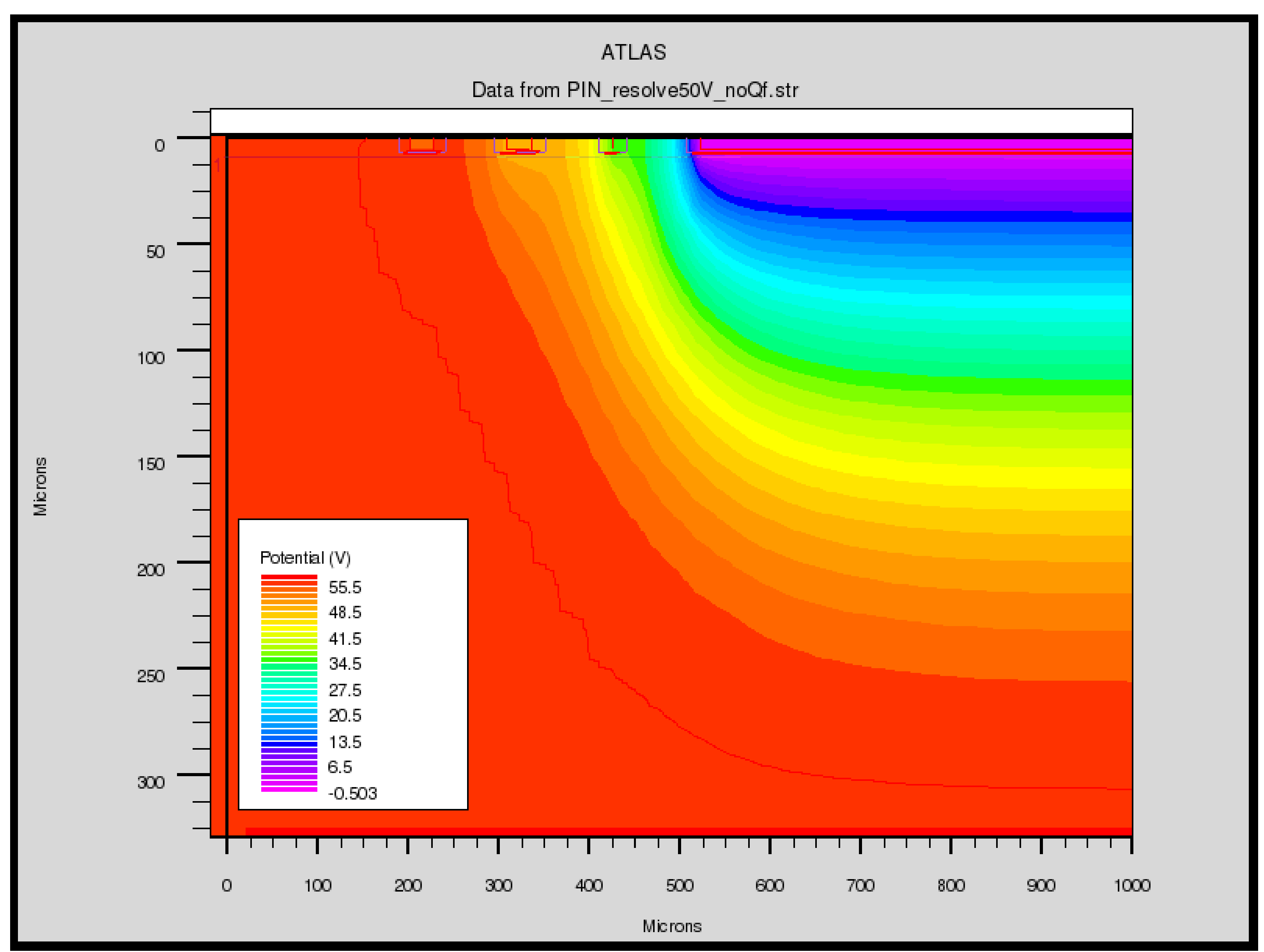
+
Thin PCB with embedded ASICs
Detector slabs integration

External cooling system (+ Manchester)
Fastening system ECAL/HCAL+composite plates

Interconnection of ASU, DIF(?)






ATLAS
Data from PIN_resolve50V_noQf.str
Potential (V)
55.5
48.5
41.5
34.5
27.5
20.5
13.5
6.5
-0.503
Microns
Microns
0
50
100
150
200
250
300
0
100
200
300
400
500
600
700
800
900
1000

Schedule (Taken from Marc Anduze)

MANCHESTER 1824

Assembling of **A.S.U.** (industrialization, gluing and tests) :

first gluing studies (glass on PCB)	**March 08**
first resistive tests according to the size of the dot	**March 08**
Backend system (DIF support)	**Jan 09 ?**
Services (cooling system participation ?)	**Jan 09 ?**

Tests of **wafers** :

reception 30 first wafers	**April 08**
set-up ("mechanical box")	

Global Design

Composite **Structures** :

mould + first H structure (126 mm)	**March 08**
"alveolar layer" mould + first layer	**April 08**
assembly mould	**June 08**
demonstrator (2 or 3 layers – 126mm)	**Sept 08**

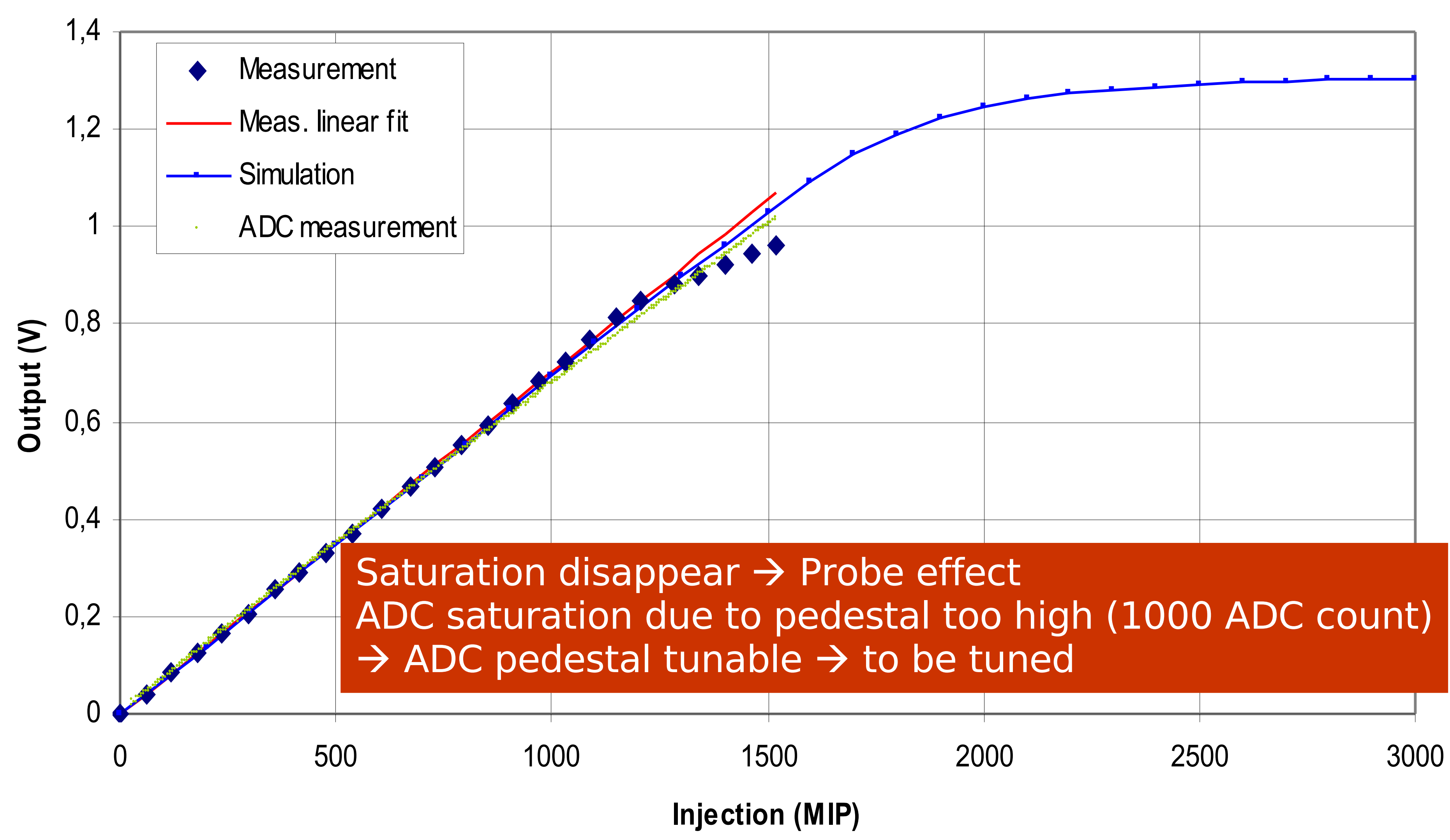
Thin PCB with embedded ASICs	**Jan 09 ?**
Detector slabs **integration**	**Jan 09 ?**

LPSC Grenoble

External **cooling system** (+ Manchester)	**June 08**
Fastening system ECAL/HCAL	**March 08**
composite plates	**Feb 08**

Lot's to be done

SKIROC - Linearity

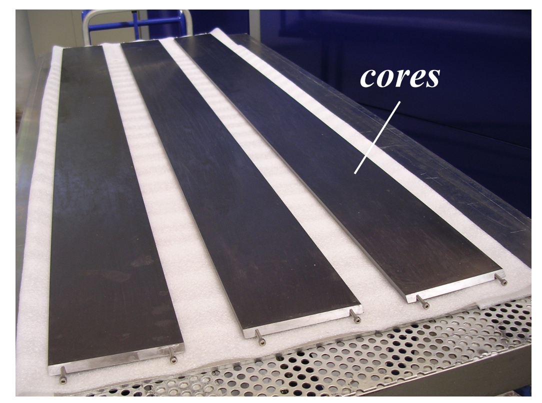


- Saturation also observed in independent measurements
- Effect about to be understood

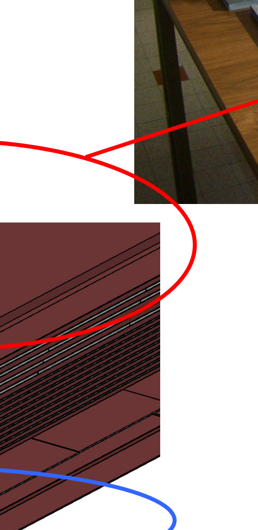
Alveolar Structure 1/2

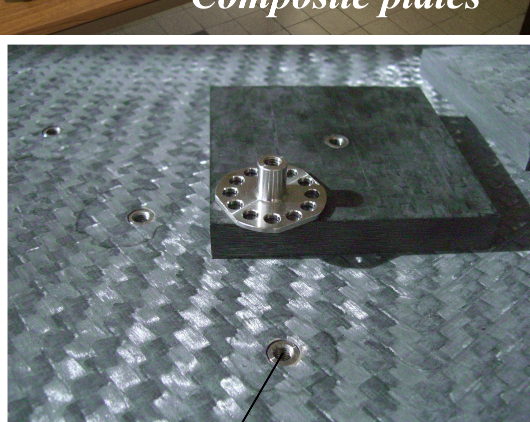
Assembled structure : Each alveolar layer are done independently, cut to the right length (with 45°) and assembled alternatively with W plates in a second curing step
(2 width of cells : 126 mm and 182 mm)

Composite plates



W layer





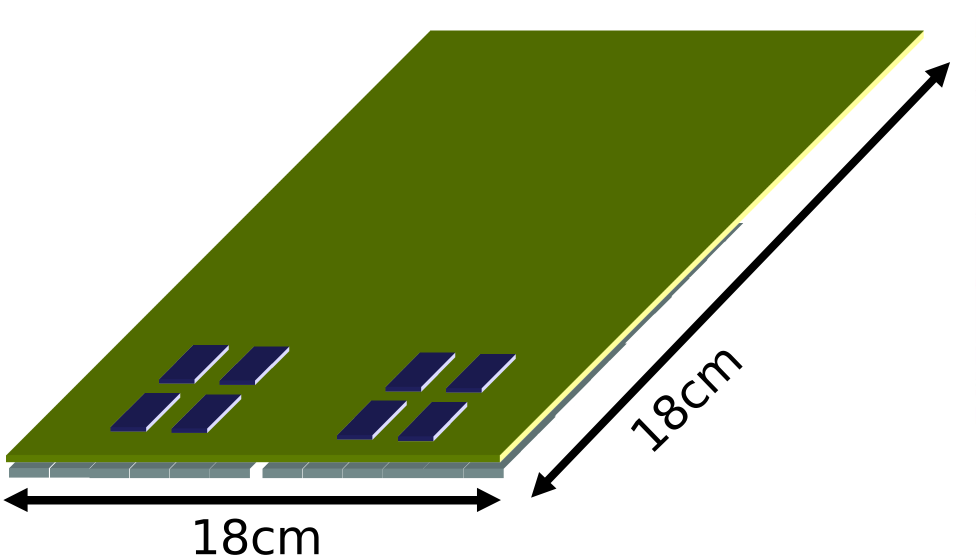
Fastening system (inserts)

« Alveolar layer » mould (first : 126 mm)

- ⇨ Global design : OK
- ⇨ “Alveolar layer” mould machining : on going
- ⇨ Design of assembly mould : on going
- ⇨ Ready : 4 composite plates (15mm and 2 mm)

PCB Design: FEVN – Parallel developments

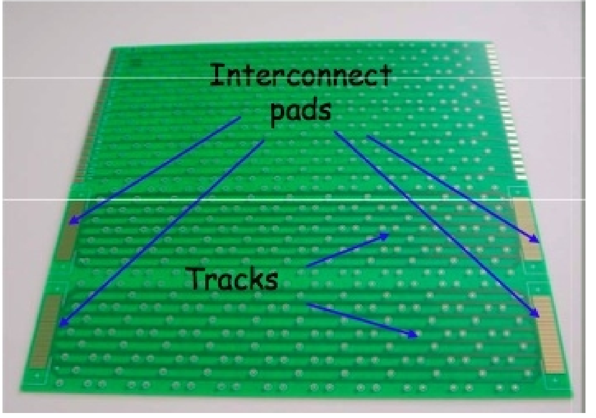
FEV5



Test interplay with
DIF cards
Dimensions?

Use HARDROC Chip (for EU-DHCAL)
to advance in PCB design
Engineering done
Expected to be ready in Jan.09

FEV6



Gluing tests
ASU Interconnection
Temperature Dissipation
Mechanical Rigidity
Dimensions

Designed and Produced

Rather a Mockup than
a fully qualified PCB

FEV7

To be designed
this summer

Employed
with
Hamamatsu
Wafers