Towards the ‘final’ JRA1 DAQ

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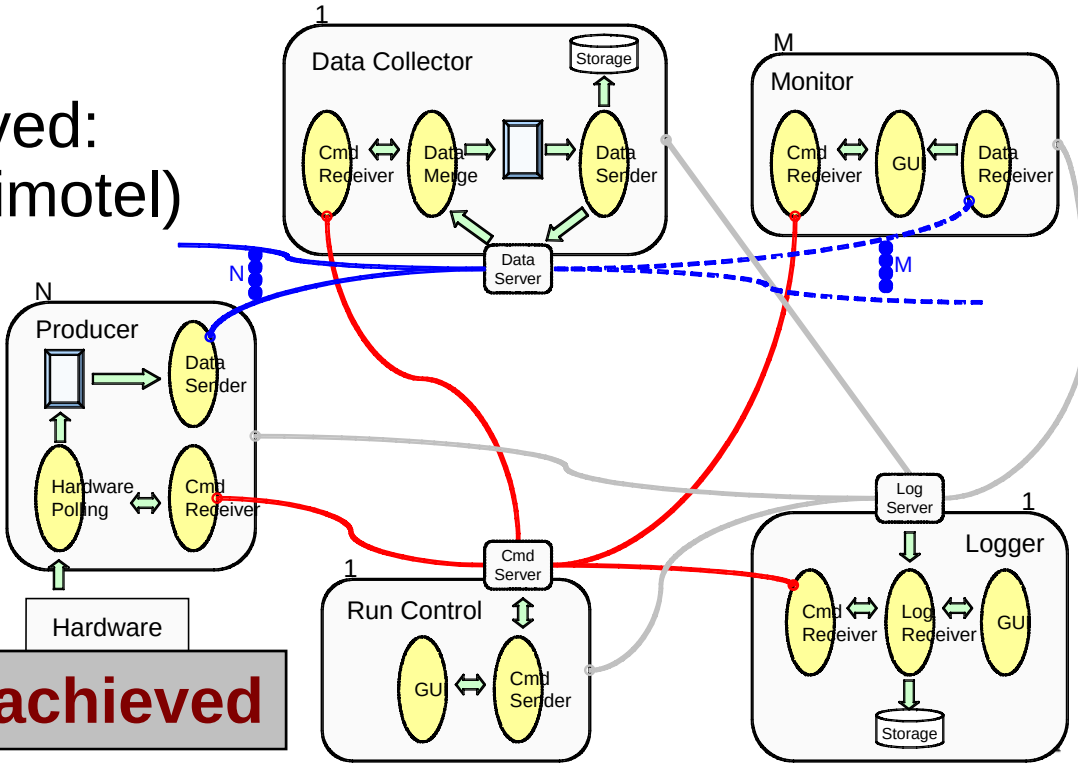
Outline

- Current Achievements & Future Goals
- Requirements/Wishlist for the final chip
- What do we need to get there?
- 1 or 2 telescopes?
- Roadmap & Conclusions

Current Achievements & Goals

- Implemented DAQ Architecture is robust, multi-platform, scalable, simple-to-use and adoptable to different users
- Lots of documentation now available
- Current Speed achieved: ~600 Hz (2 boards/Mimotel) in ZS mode
- Goals (for EU):
  - 1 kHz
  - more documentation (code)



Goals are (nearly) achieved

Requirements/Wishlist for the 'final' Chip

- TC-Mi26: zero suppressed binary outputs
- Integration Time of TC-Mi26: 100 μs → 10^4 frames/second
- Factor 10 above original goal
- 100 Mbit/s data throughput/chip

How to get there?

Hardware Requirements

- EUDRB + newly designed digital daughter card (Baseline):
  - Angelo Cotta-Ramusino will design this with input from Strasbourg group
- Alternative: digital I/O board from CAEN
  - under evaluation by INFN

I prefer EUDRB+daughter card: more experience and less expensive

Software/Firmware Requirements

- Current VME driver could transfer data from 6 cards at around 1 kHz
  - 'only' running at 80 MB/s, not yet full 2e SST speed (160 MB/s)
  - mainly waiting for boards to be ready
- To achieve more, we need:
  - decoupling of input/output buffer in EUDRB (boards should be ready for the next frame immediately after having finished the current frame)
  - multi-event buffer in the EUDRB and 2e SST

1 or 2 Telescopes?

- Demand to continue using Demonstrator in addition to final telescope
- Needs additional hardware:
  - either more EUDRBs
  - or Strasbourg readout boards (requiring a new dedicated producer task)
  - or reduced size Demonstrator with e.g. only one arm?
- Needs additional manpower to run 2 telescopes

Roadmap

- Next 6-9 months should bring final readout
- Design of new daughtercard for EUDRB is key to success:
  - Firmware may need special attention
- Hardware requirements should be fixed before end of this year (~submission time of final chip)
  → dedicated meeting INFN/IN2P3
- Firmware should follow soon after (Q1/2009)
  → dedicated meeting INFN/DPNC

Conclusions

- From FP6 point-of-view, DAQ is ‘nearly done’, goals are achieved
- Final chip would highly profit from increased speed (x10)
- Next version of EUDRB can (hopefully) cope with the demand, at least partly
- Software would need only minor changes