

The Readout Electronics for TPC with GEM readout chamber

(and for almost any other readout chamber)

Anders Oskarsson
Lund Univ.

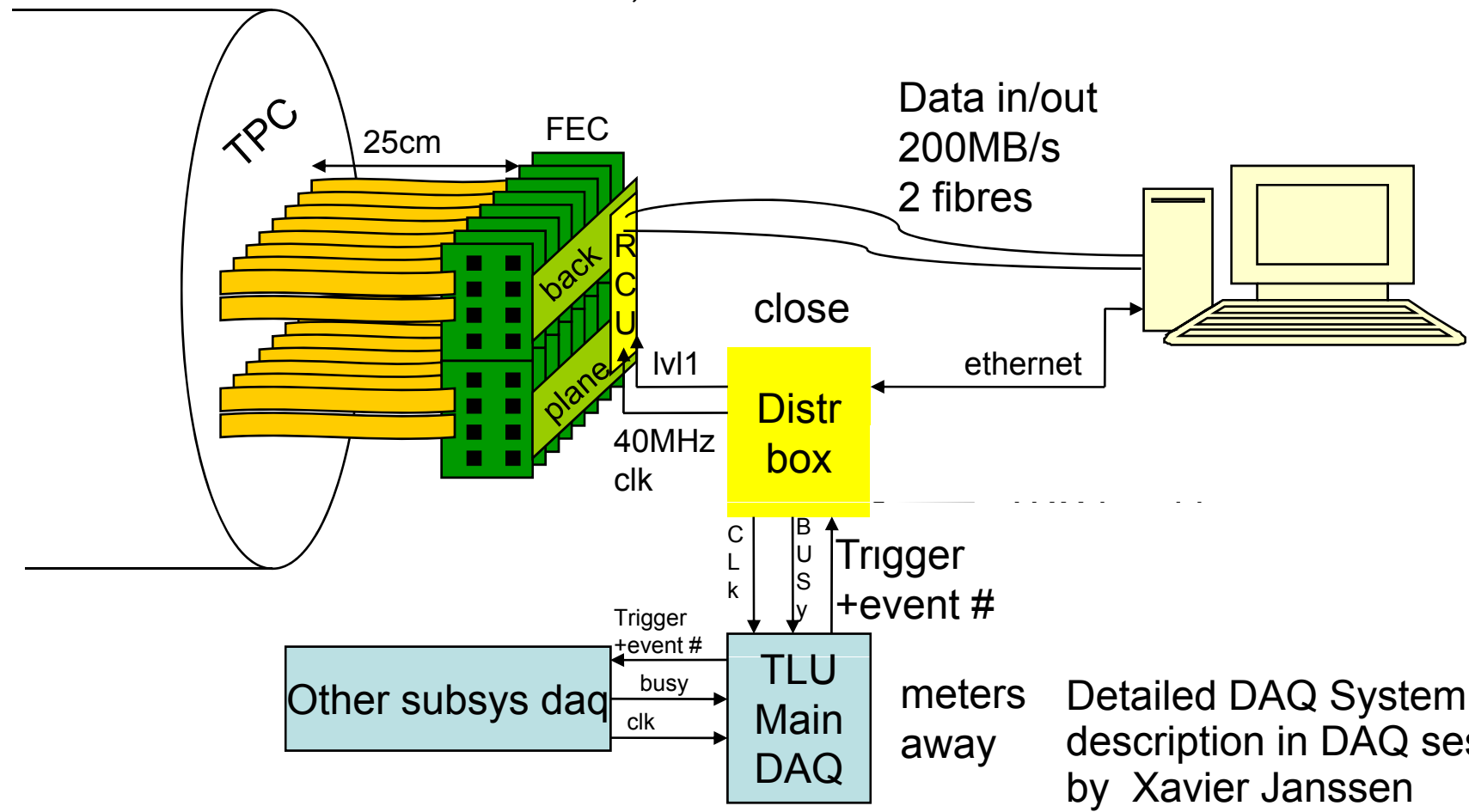
Electronics: Bruxelles, CERN, Lund
Mechanics: Desy, Lund
Small GEM-TPC: Aachen-Bonn

Outline of the talk

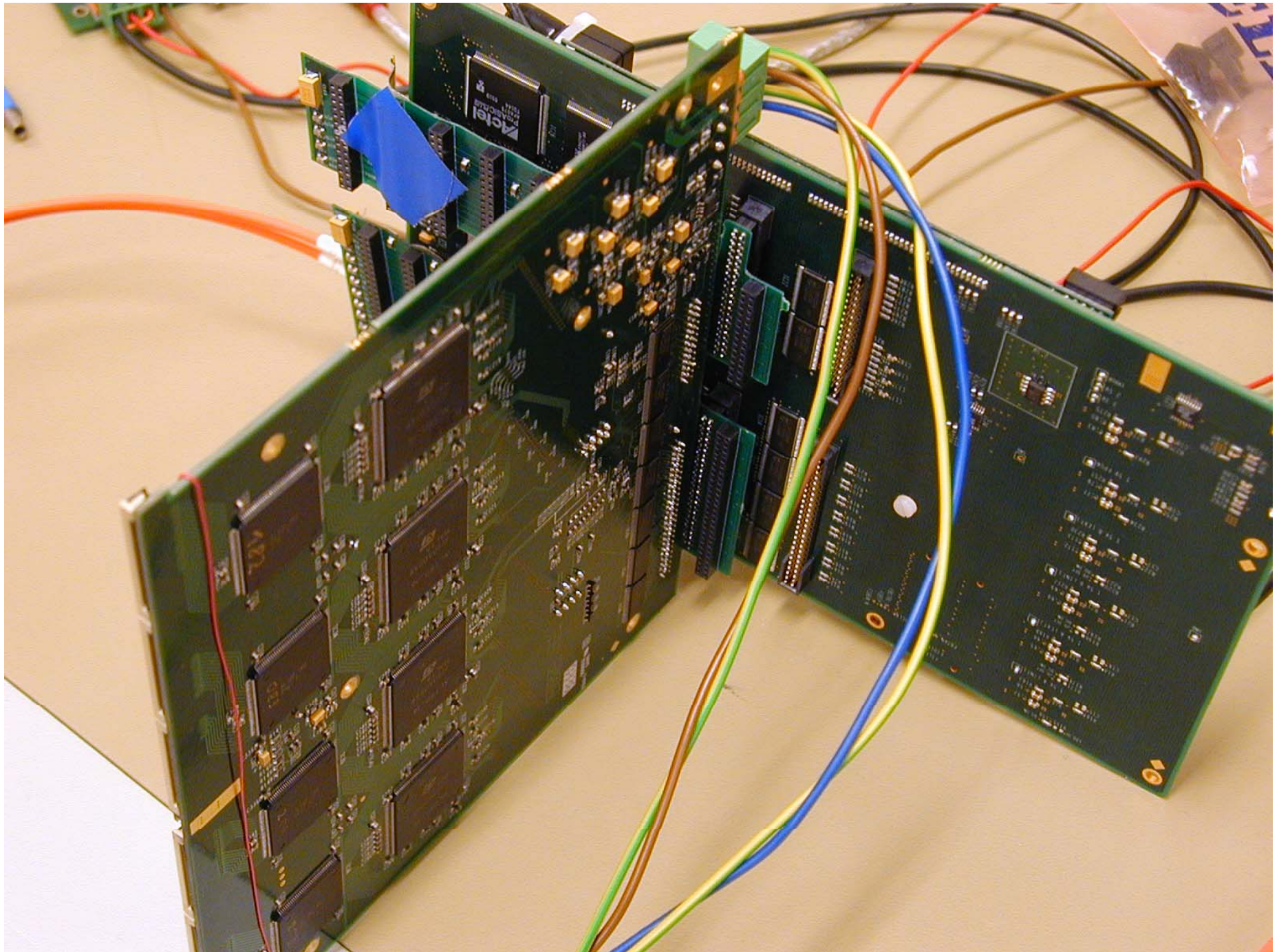
- System description
- PCA 16, the new preamp/shaper
- ALTRO, the digitizer-event storage chip
- The 128 ch Front-end card
- How to connect: Connectors and cables
- System test of 128 ch system, first deliverable (256ch)
 - On the bench
 - On small GEM TPC
- LV-system
- Mechanics for the front-end electronics
- Plan to complete

If we run together with other subsystems

2048ch, 16 FEC

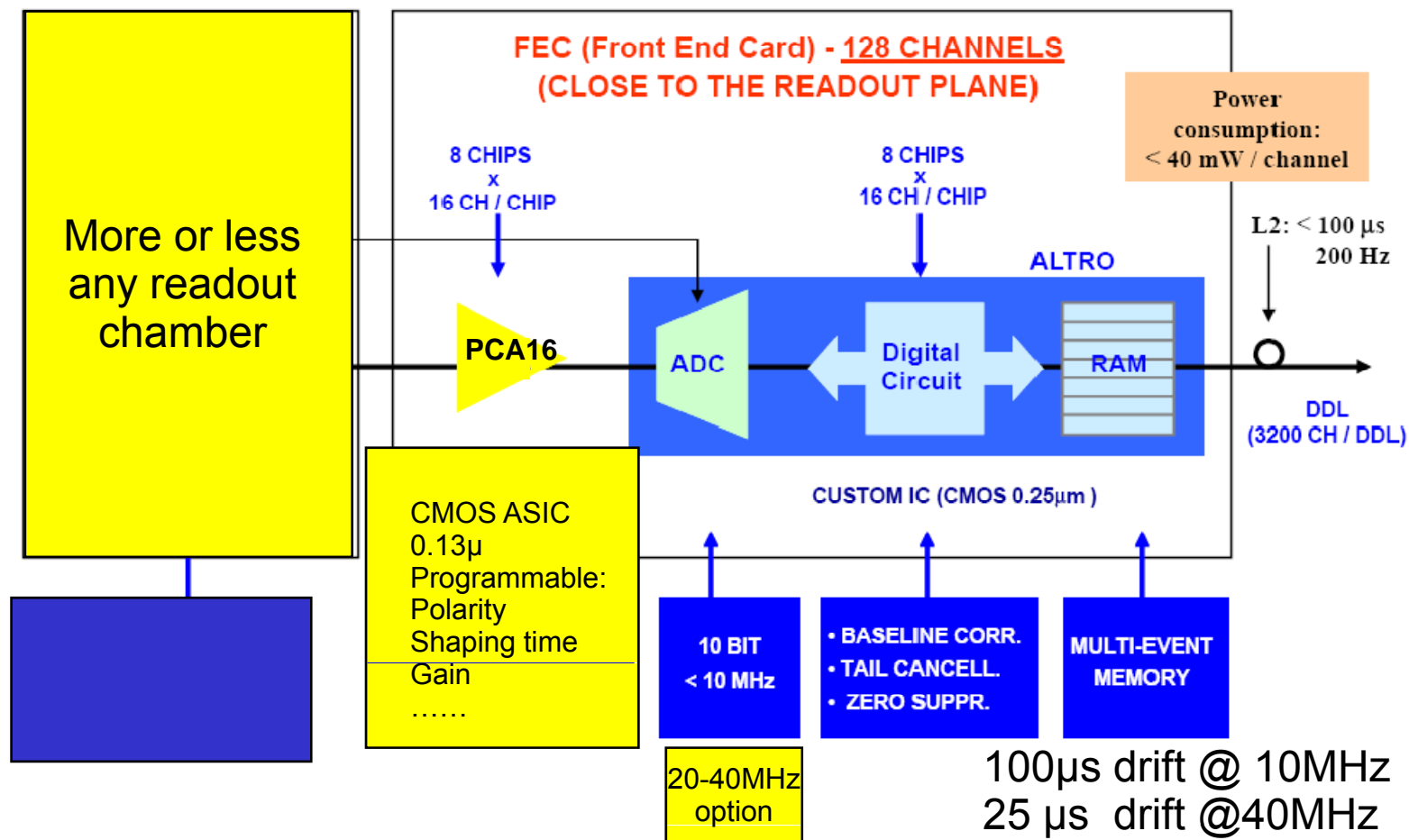


Detailed DAQ System description in DAQ session by Xavier Janssen



EUDET readout FEC

Front End Electronics Architecture



Programmable Charge Amplifier (PCA16)' (CERN design)

- 1.5 V supply; power ~ 8 mW/channel
- 16 channel charge preamp + shaper
- Ca 300 electrons noise at 10pF
- Differential output
- Programmable features
 - signal polarity
 - Power down mode (wake-up time = 1 ms)
 - Peaking time (30 - 120 ns)
 - Gain in 4 steps (12 - 27 mV/fC)
 - Preamp_out mode (bypass shaper)
 - Tunable decay constant of the preamplifier

Basically pin-compatible with PASA (Preamp-shaper, ALICE-TPC)

ALTRO digitizer+drift storage

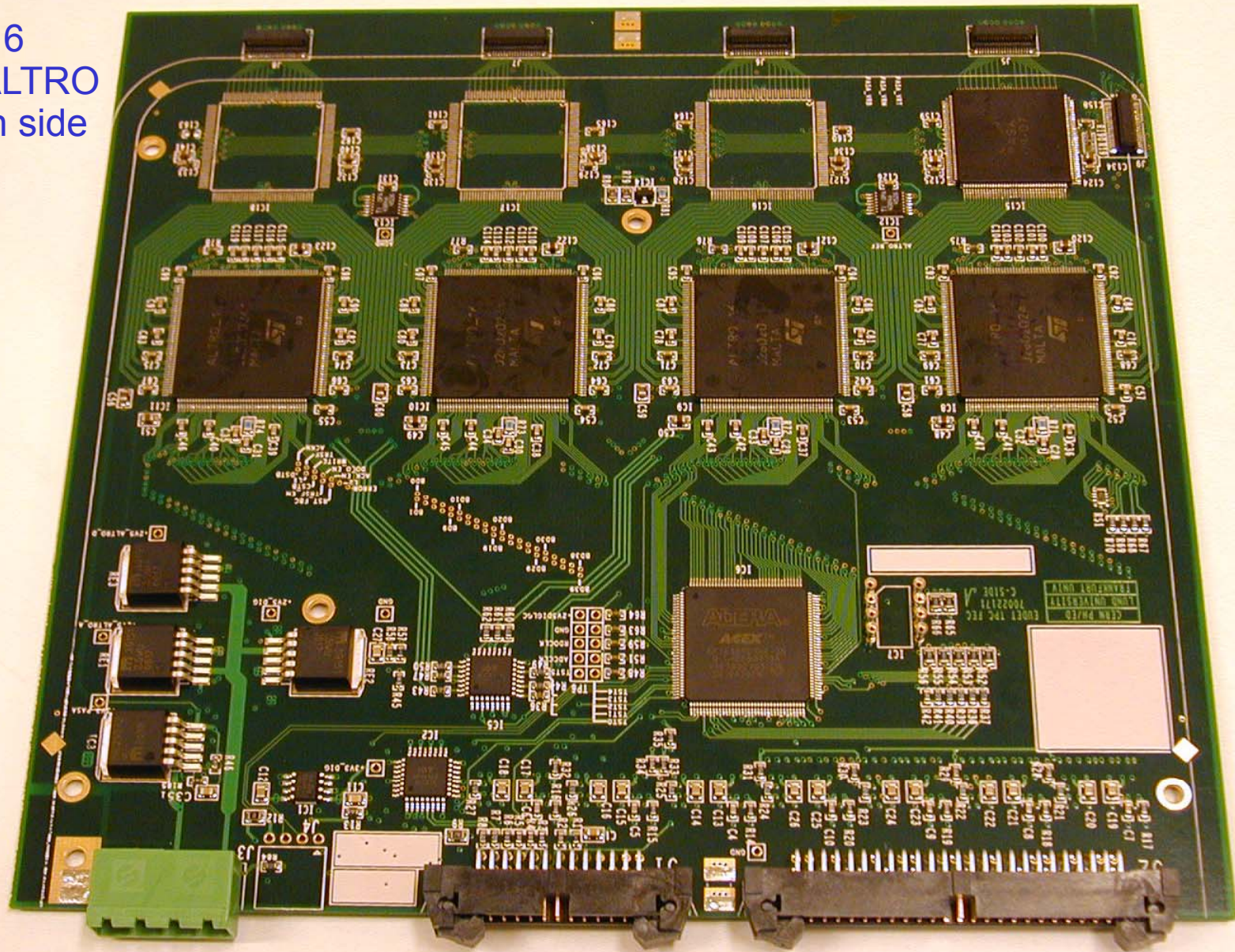
- Differential input from PCA 16
- 16 channels per chip
- 10 bit resolution, 1mV per ADC channel
- 1k samples per event

- 10MHz sampling in ALICE (100microsecs drift)
- 20MHz (50microsecs drift)
- Ca 125 chips with enhanced sampling freq. 40MHz
- Pedestal subtraction, common to all samples
- Advanced zero suppression - good data is sequence (selectable) of non-zero samples.
- Pulse data, + pre and postsamples
- 4 event buffering. (multievent buffering not used here)
- several other ALICE features for MWPC pulses are disabled

6 watts per FEC

4 connectors 32 ch plus 8 gnd in each

4 PCA16
and 4 ALTRO
on each side

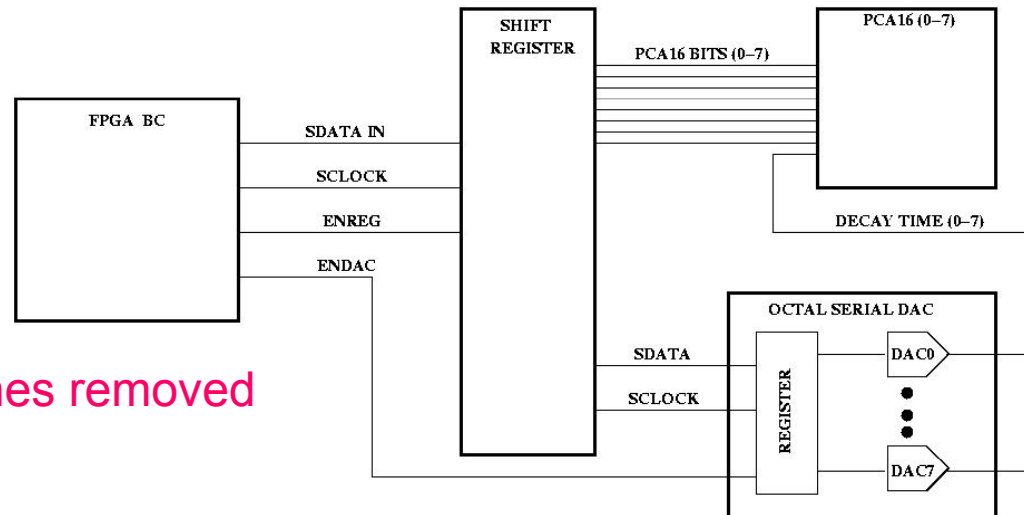


Backlane connectors to 32 bit, 40MHz bus

The main modifications relative to ALICE FEC

Remote control of PCA16 via board controller

-Optional control by switches removed in final design



-Modified grounding around ALTRO, reduced coherent noise significantly

-Modified reference voltages to ALTRO in order to accommodate all settings of PCA16. So the standard calibration is 1.2mV/ADC channel. If experience tells us that some settings may not be used, this may be changed back to 1mV/channel by changing 2 resistors per FEC).

-skipped water cooling

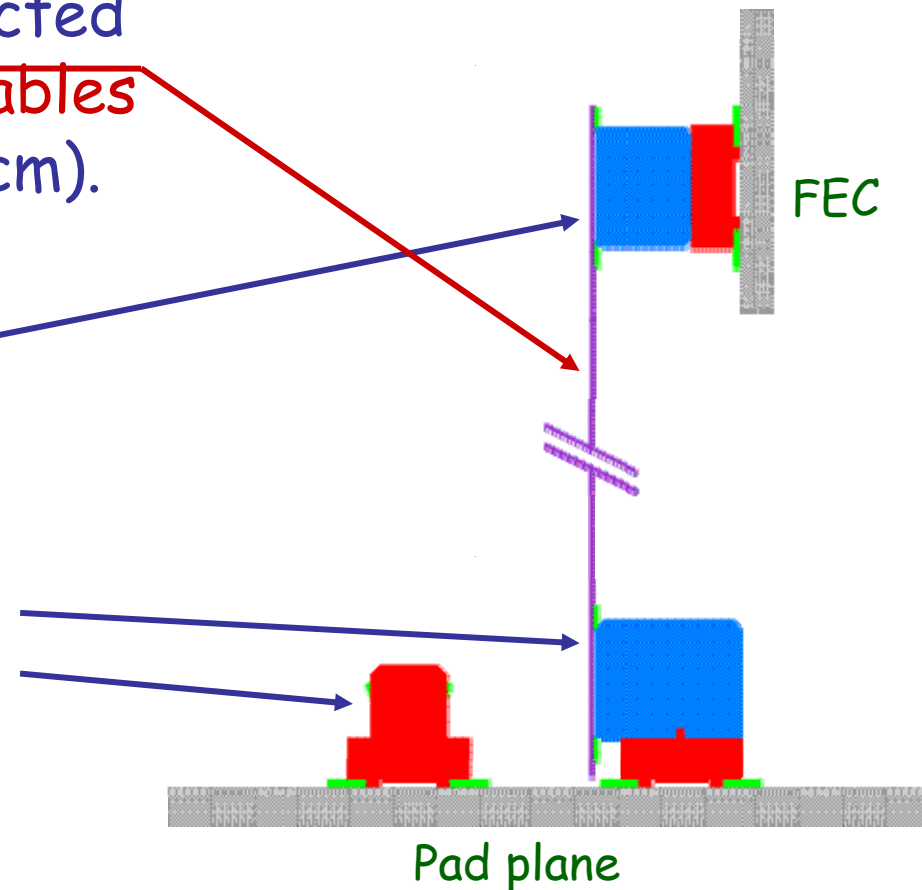
-Added one external voltage+regulator for PCA16, 1.5V. Saved ca 20% pwr.

Connectors and cables



- The front end card is connected to the pad plane via **kapton cables**
 - modified cable at hand (30cm).
- X-talk test next week

Connectors from Japan aviation.
40 pin connector (for 32 channels)
fits over 2 rows of 16 pads if
pad size is $1 \times 4 \text{mm}^2$



Connectors and cables



First cable: some x-talk problem ca, 2%, from trace on one side to closest trace on opposite side.

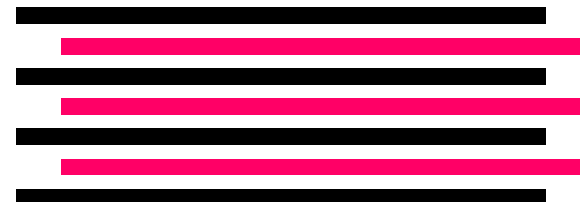
Modification without increasing overall width. Reduced ground strips on the sides and increased space between signal traces.

First cable



Spacing 0.2mm
trace width 0.2mm

Present cable

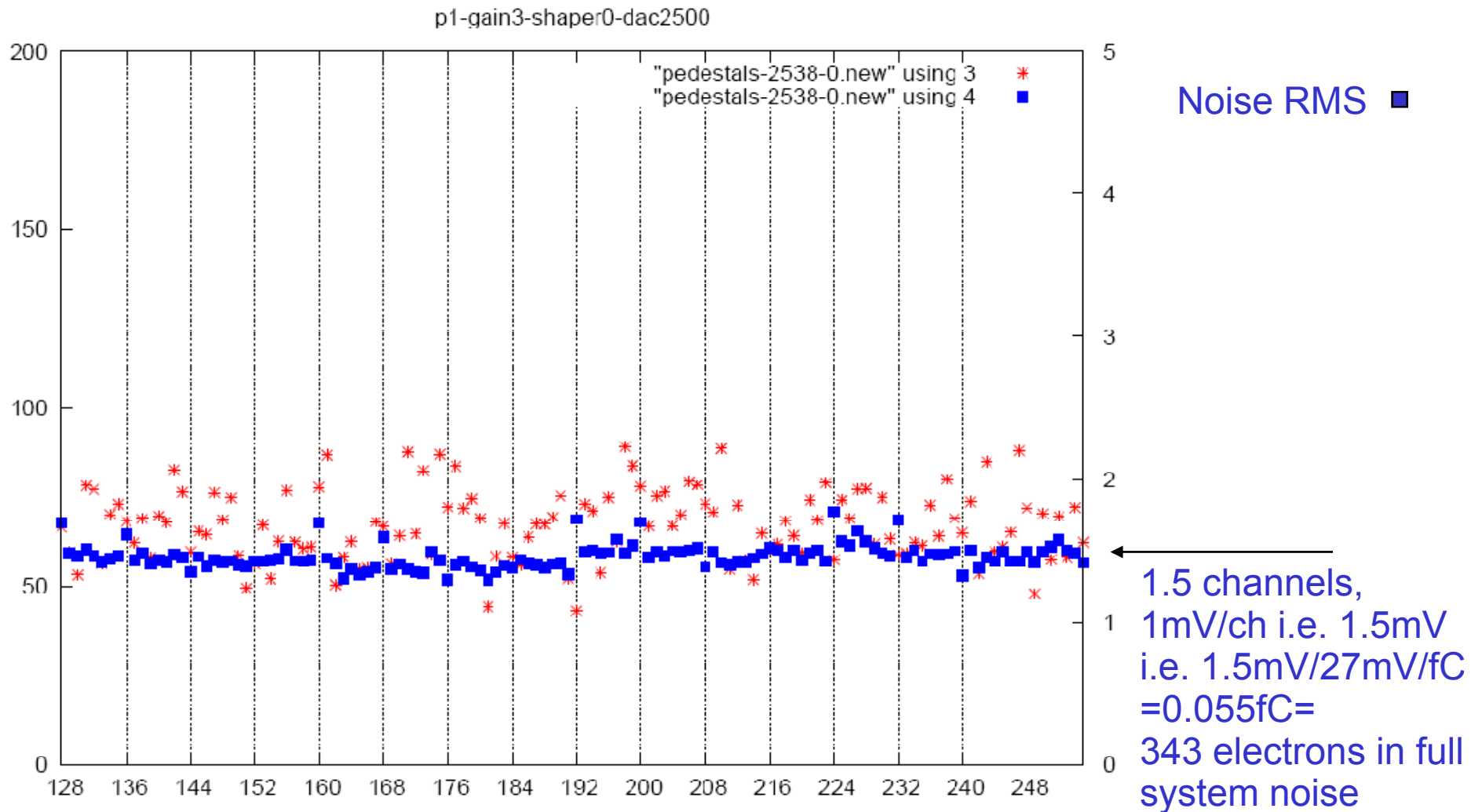


Spacing 0.5mm
Trace width 0.2mm

Black and red on opposite side.

Gain 27mV/fC, Cables on. No chamber.

Bench test result



Exceptional result. Remember few years ago, preamp chips had 500 electrons as theoretical random noise at 0pF.

COSMIC setup with small GEM TPC

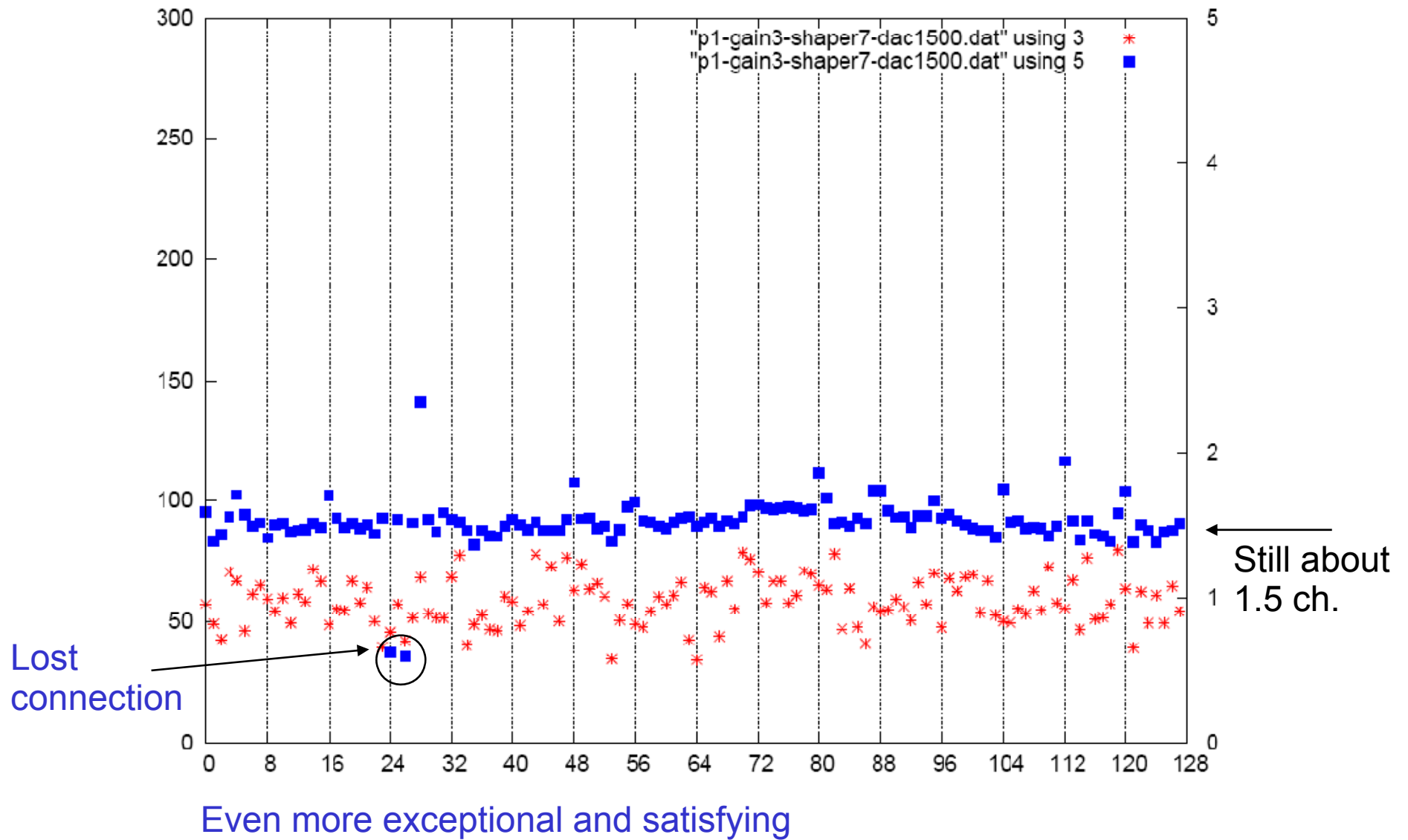


Aachen-Bonn

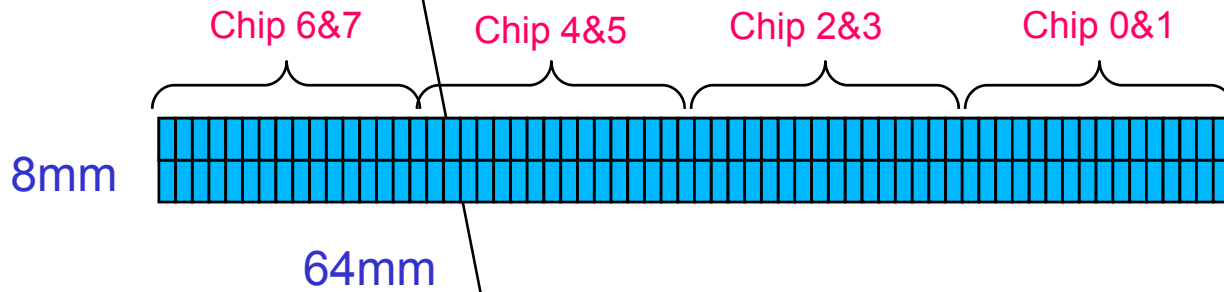
155203 D
453047
RoHS
LST

ETEA

Blue. RMS noise. Chamber connected. Real LV system
Highest gain, shortest shaping time (worst conditions)

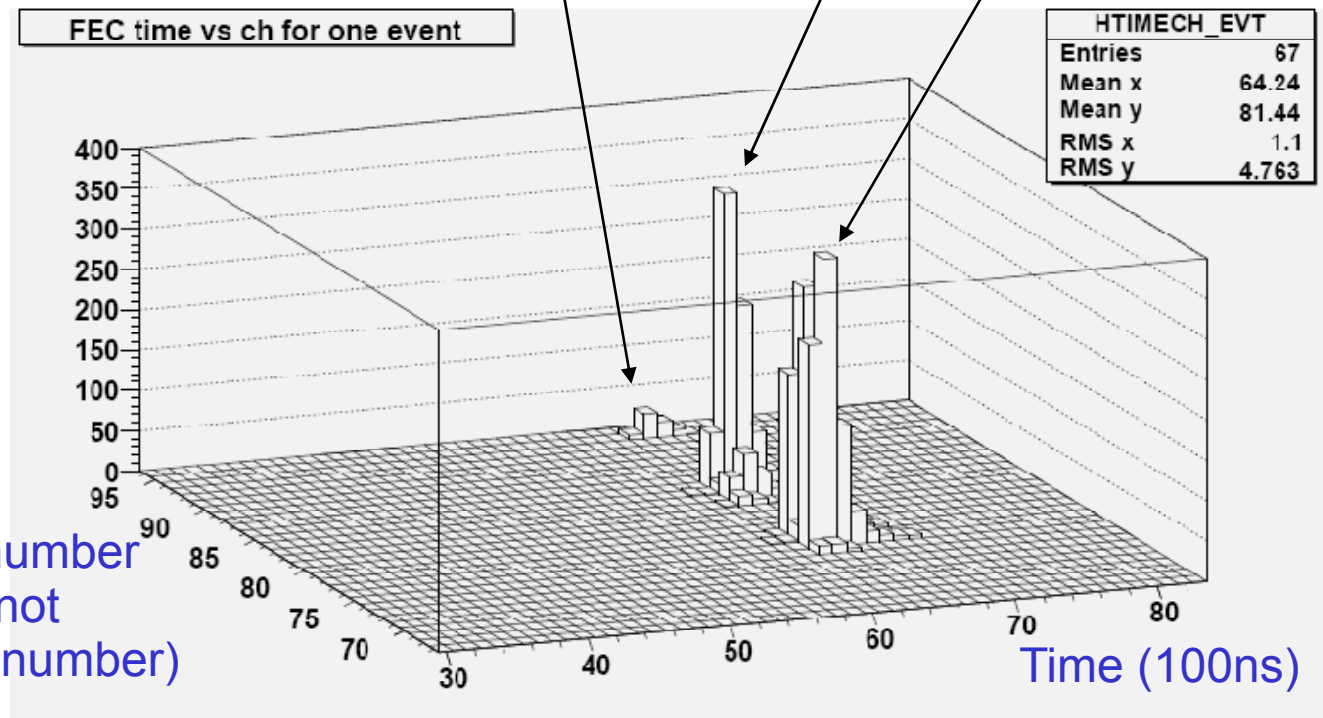


Cosmic track



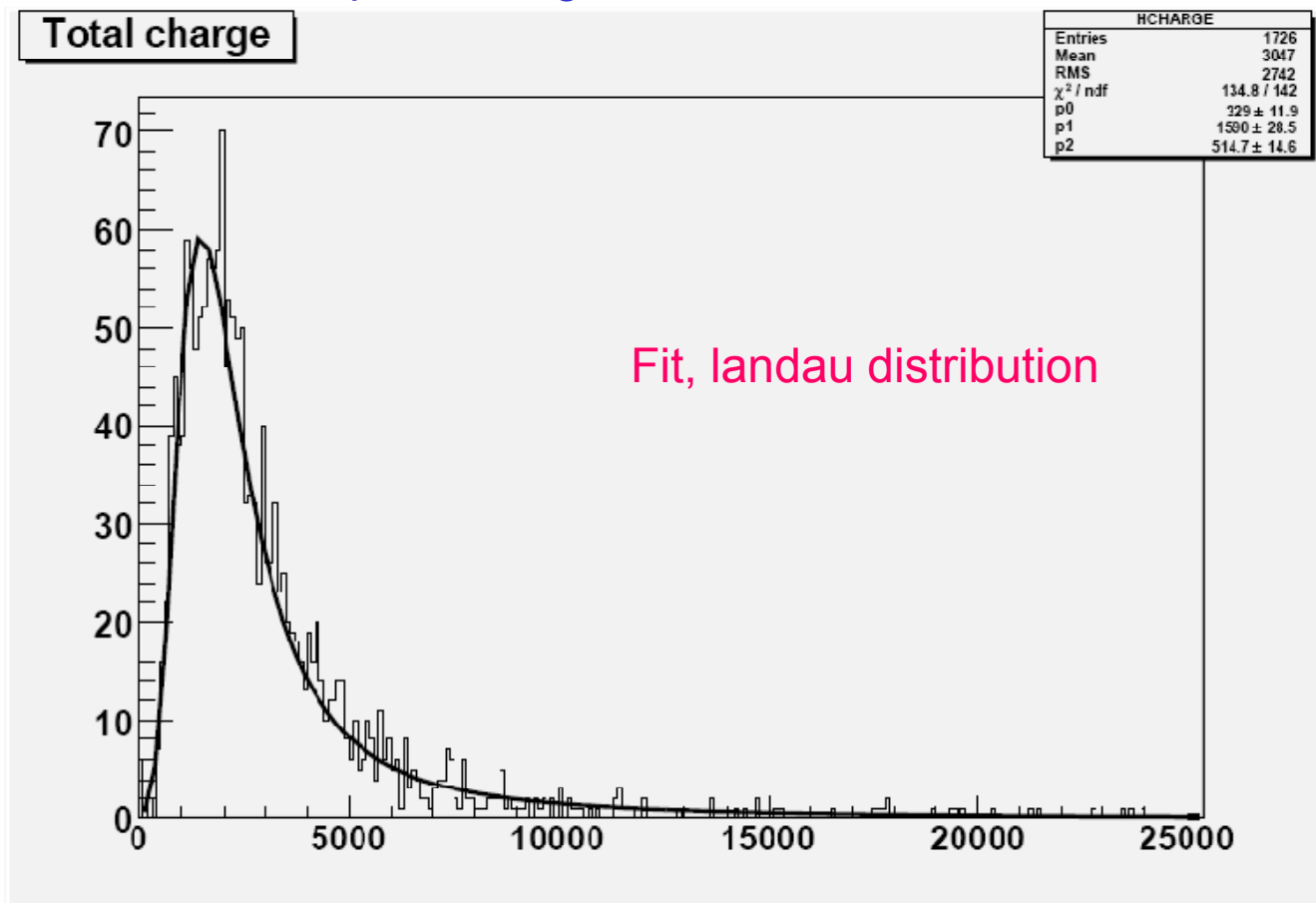
Pads $1 \times 4\text{mm}^2$

Next ALTRO Bottom row Top row



Energy loss distribution for cosmic muons.

Added all sampled voltages



CHIP availability

EUDET

- PCA16, 160 tested and available in Lund for 2048ch system
- ALTRO 25MHz, 160 tested and available in Lund for 2048ch system
- ALTRO 40MHz for high resolution sweet spot, ca 100 operational at CERN (needs desoldering from boards).

LC-TPC project

- PCA16, 772 chips arrived last week (ca 90FEC). Testing ca 2 weeks.
- 25MHz ALTRO, tested, 400 in Lund, ca 300 to get from CERN

Test robot in Lund:
Have tested ca 100000 ALT
and ca 100000 PAS



Plan to complete

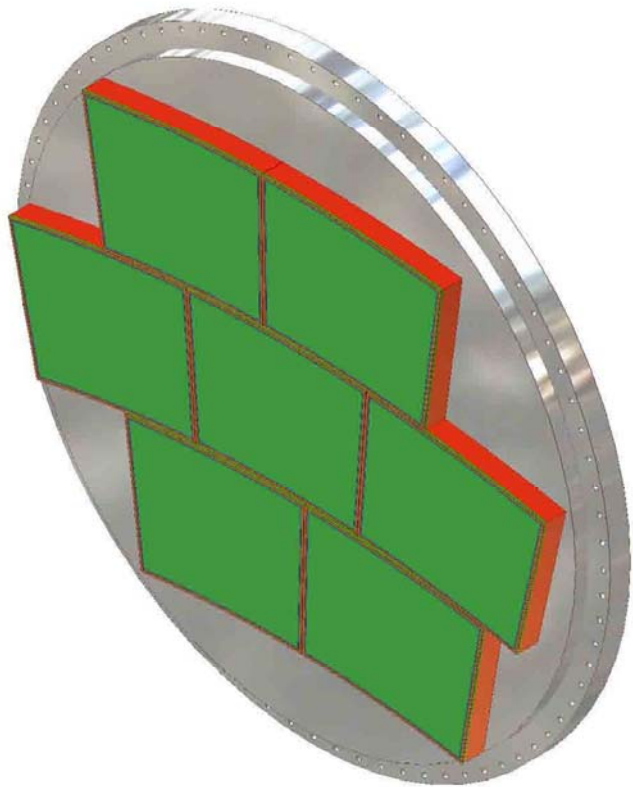
- 5 FEC assembled last week+2 existing, 1120 channels, (EUDET 1000ch system). Evaluate next week
- Oct 17: order 100 FEC Circuit boards. 3 w delivery; tests of PCA16
- Nov 10, assemble 11 (27) FEC 2w delivery
- Nov 24, 2048 ch EUDET system ready
 - (option to discuss 32 FEC max RCU system 4096 ch instead of 2048)
- Get 40MHz option operational

After experience with full crate system, finalize cooling

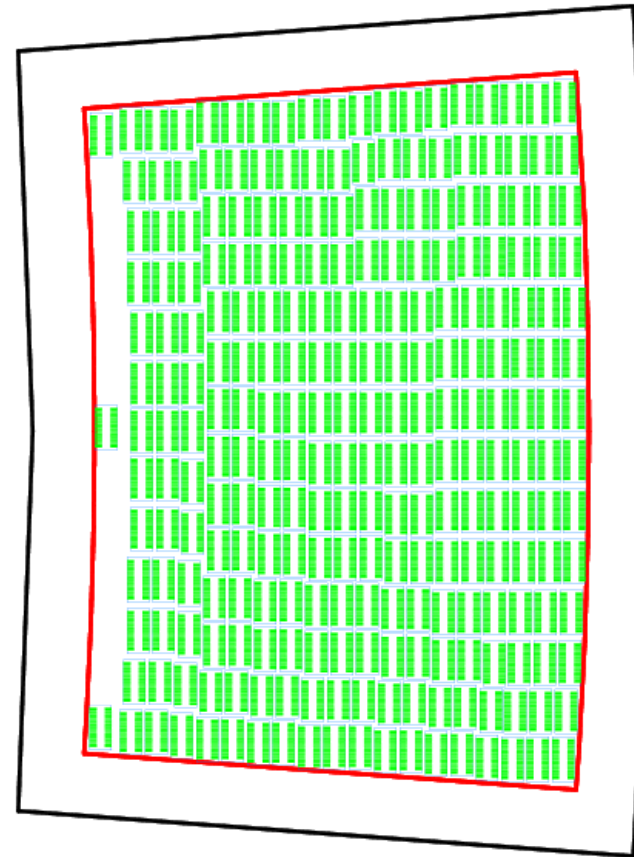
- At any time when needed, assemble remaining FECs, depends on chip yield but ca 100 FECs in total can be expected. Takes 2w after order.
- 4 parallel systems, RCU and out, ordered with delivery during October.
plus one development system in Lund and one in Brussels.
- Mechanics & cooling

End-plate and panels

Endplate with panels



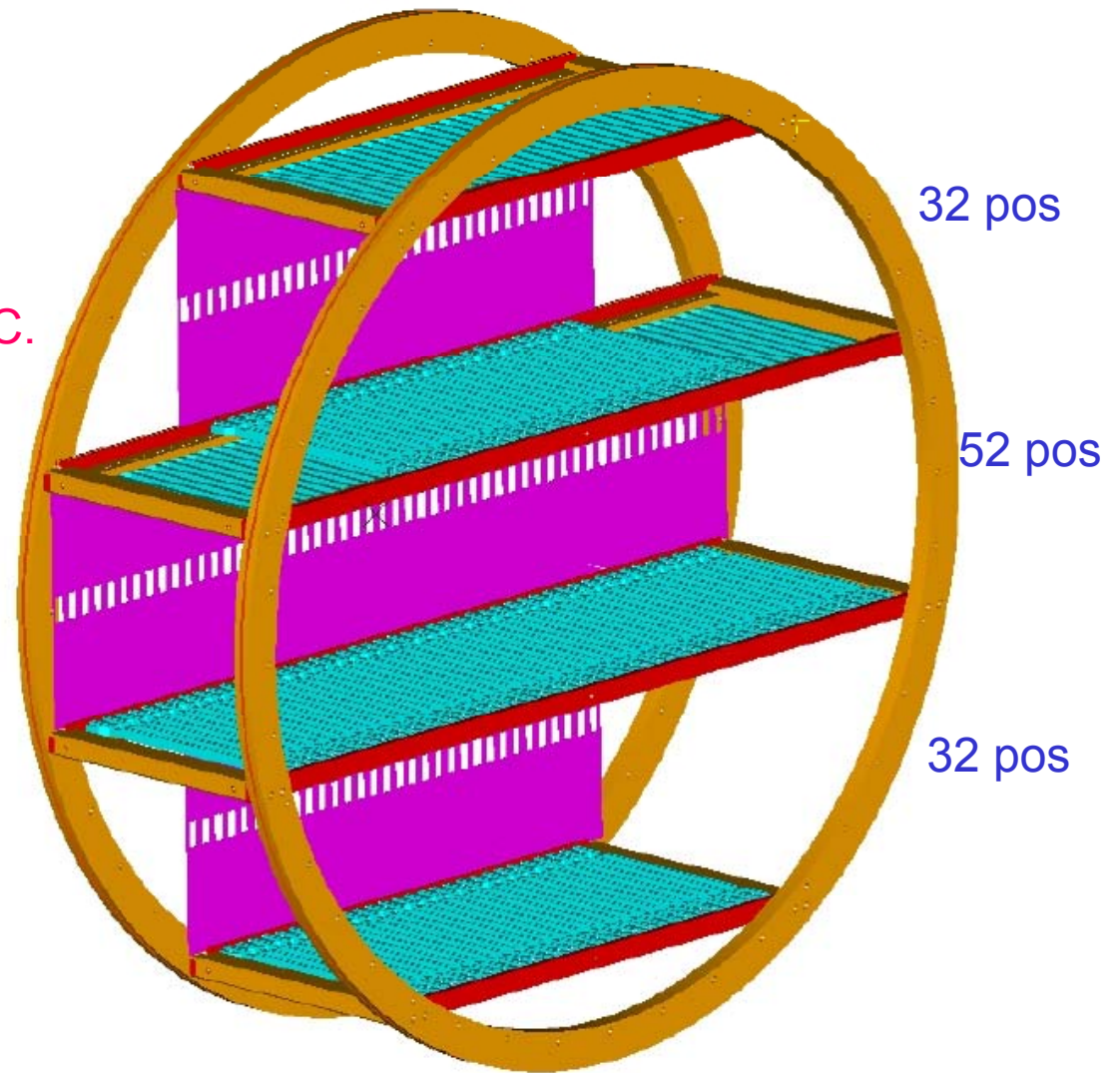
Panel with connectors
(Density for 1*4mm pads.)



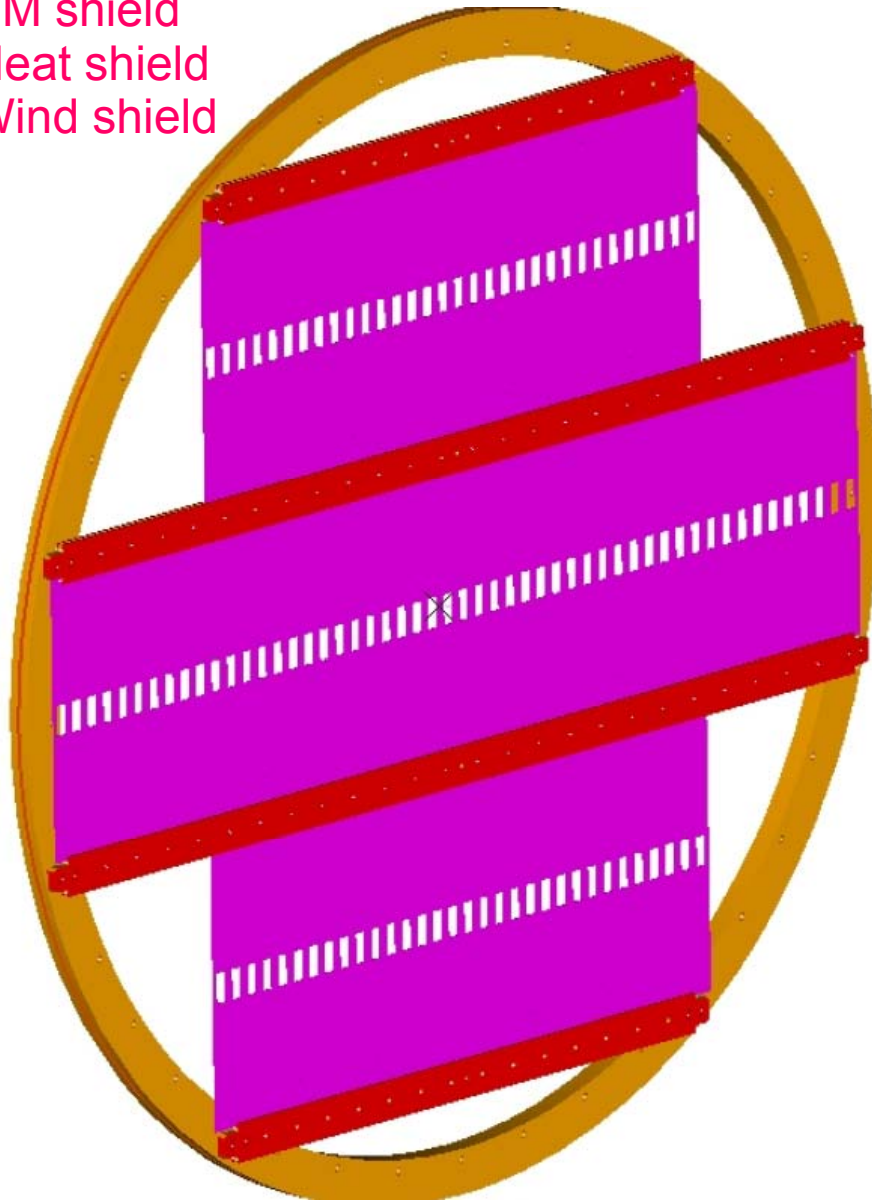
Have used the drawings 6080-102, 16 oct 2007

Electronics mounting rings

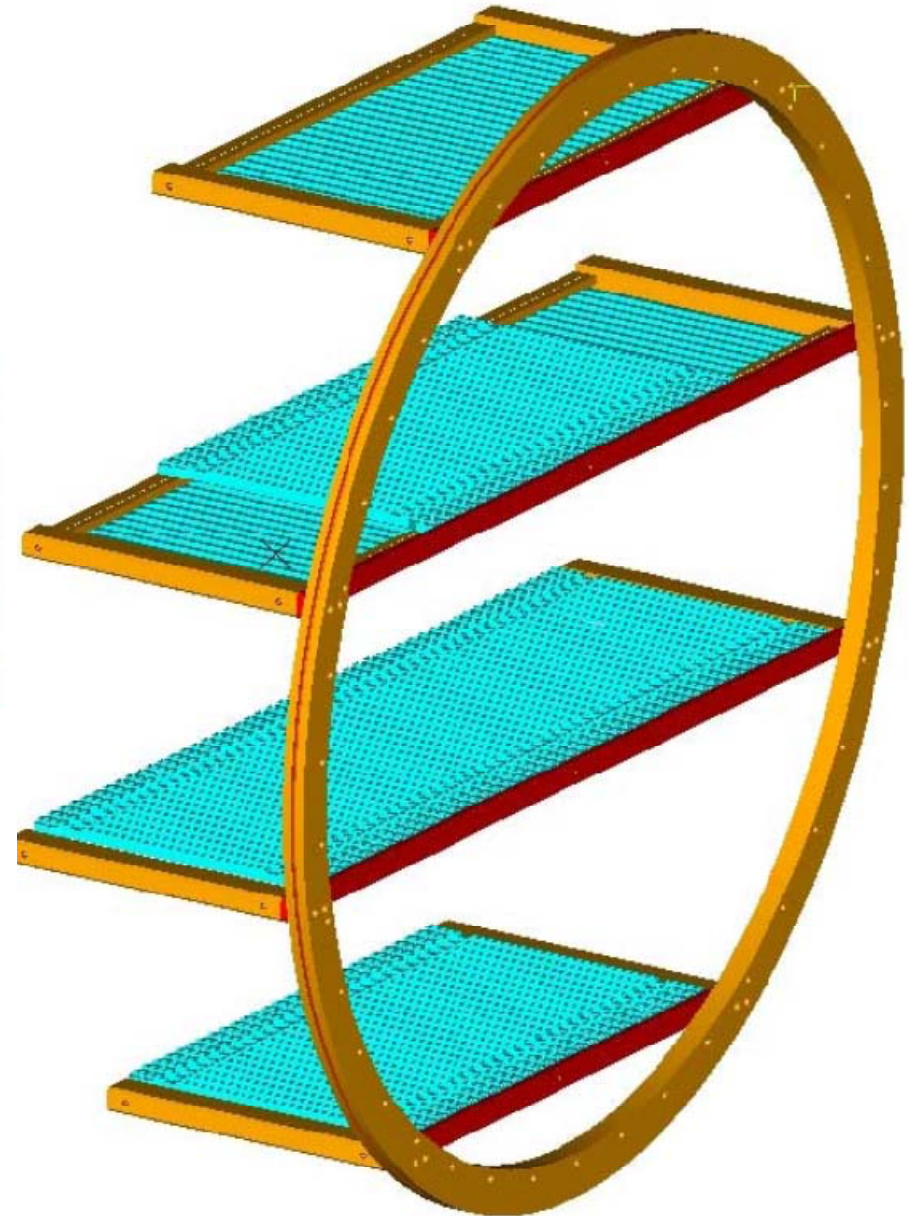
- Rings have same outer diameter as TPC
- supported on the same rails as TPC.
- Rotates and slides together with TPC
- Puts no weight on TPC.
- Ca 10cm behind TPC back flange
- 14mm FEC spacing



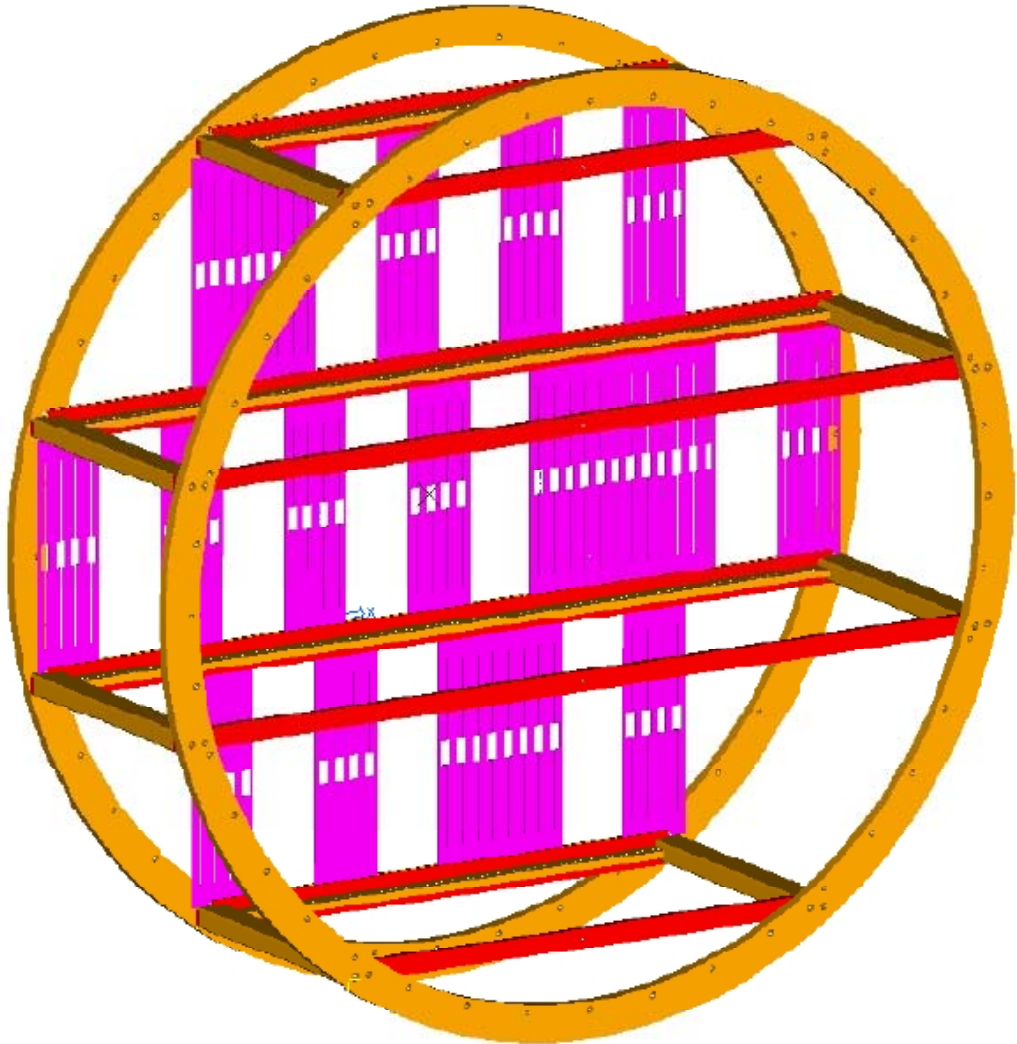
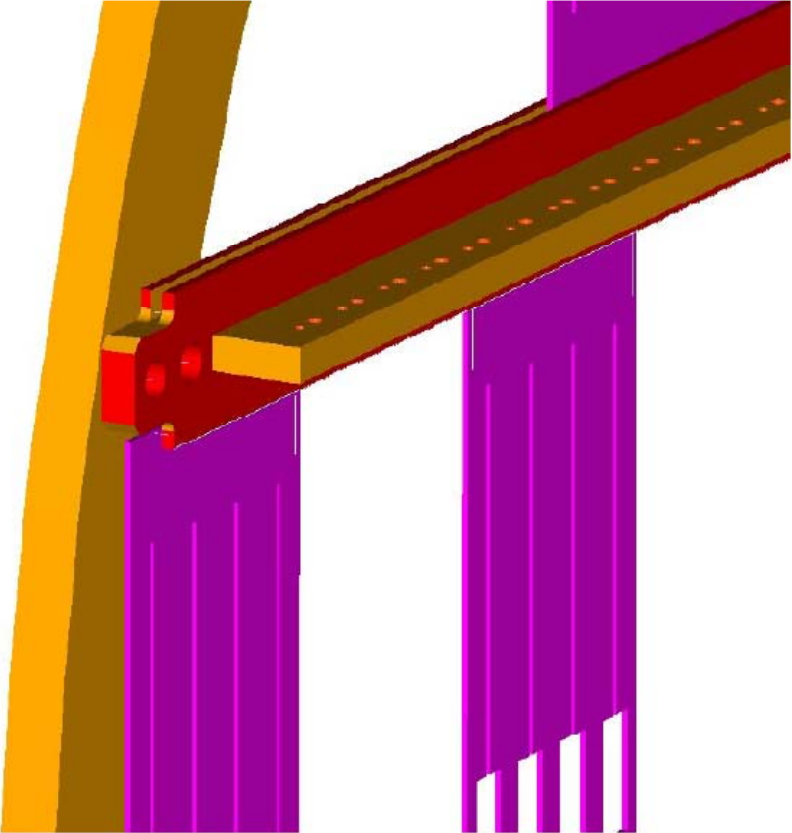
Front shield:
PC board material
Holds Kapton cables in slits
PC-board material (grounded Cu one side)
EM shield
Heat shield
Wind shield



Back ring with FEC guides
detached when mounting Kapton
cables



Front shield detail.
Units for 4 FECs (16 cables)



How to run?

A panel with $1 \times 6\text{mm}^2$ pads contains ca 4200 pads.

With 32 FECs (128 ch each) we serve 4096 pads.
This is the maximum we can read out to one RCU.

With 80 FECs

