Electronics Integration – Status AHCAL

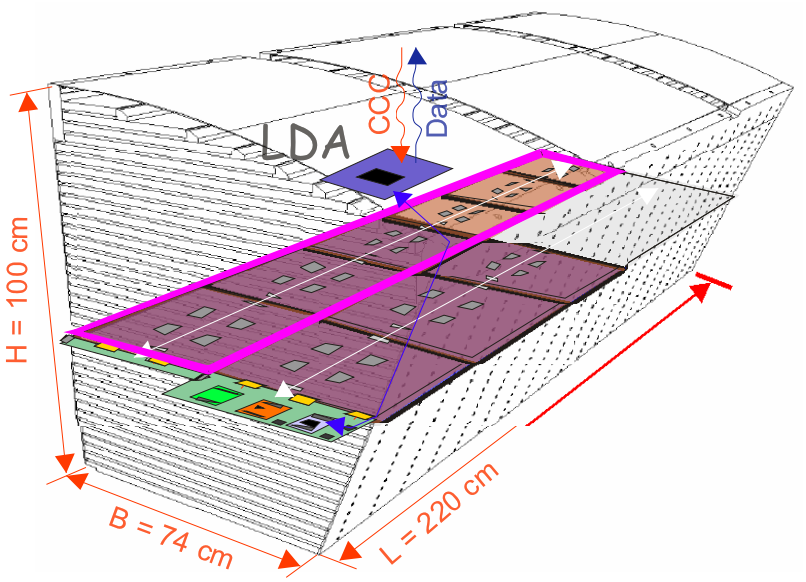
Mathias Reinecke

for the AHCAL developers

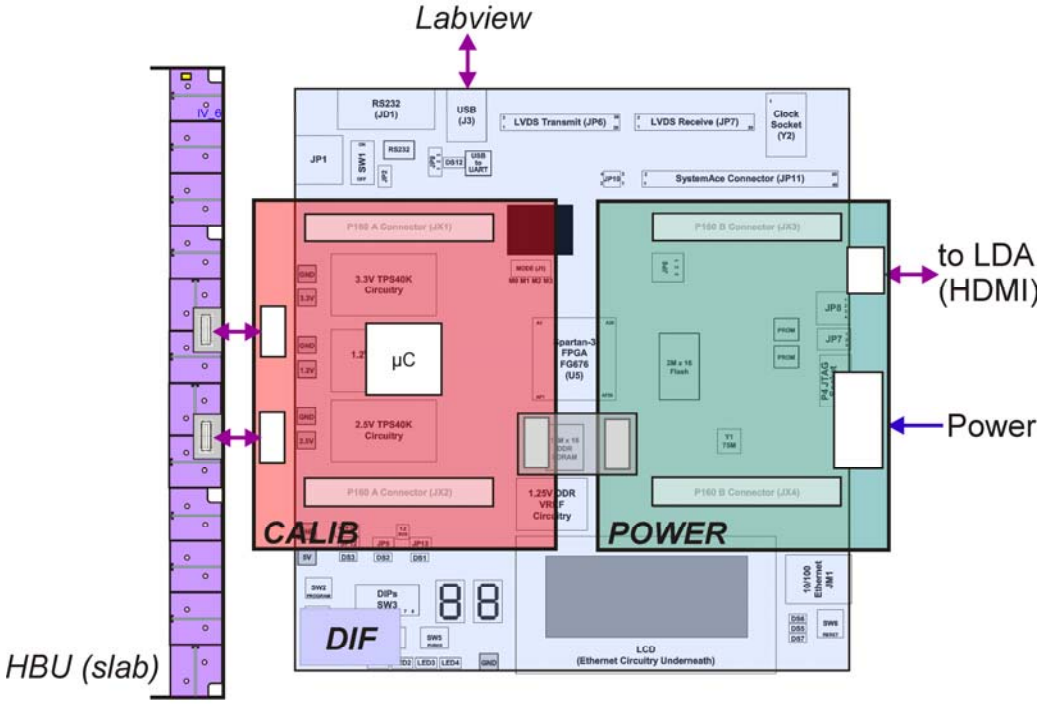
Next prototype: Architecture

FE

the future …



1st EUDET Prototype (**1st step**)



Commercial DIF, new mezzan.
(CALIB, POWER), 1HBU (later: 6)

Prototype Tiles

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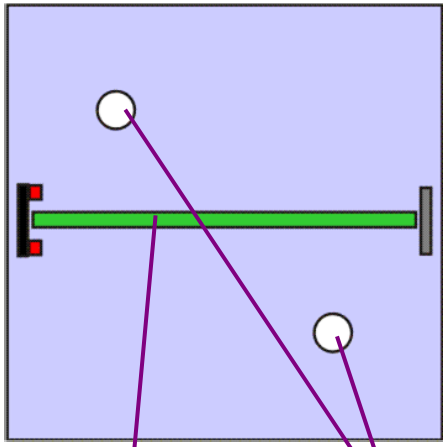
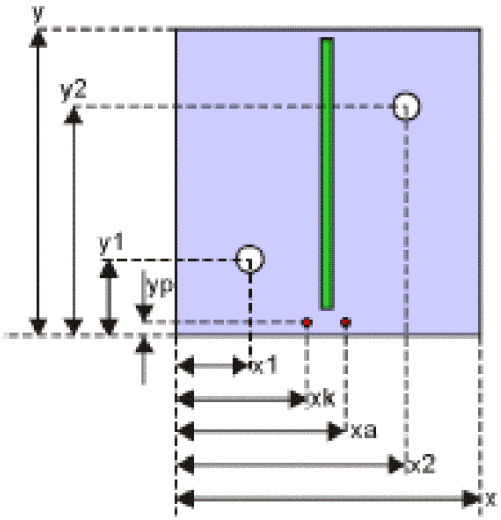
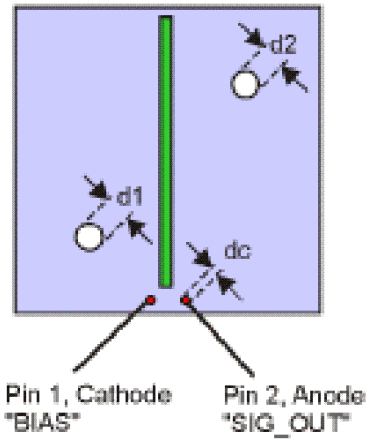
Prototype Tile for HBU

dimensions in (mm;mm)



Dimension's name	dimension (mm)	Remarks
x	30	including passivation (white border)
y	29.95	including passivation (white border)
x1	8.02	average value from Roman's talk
x2	22.19	average value from Roman's talk
y1	7.91	average value from Roman's talk
y2	22.03	average value from Roman's talk
xk	13.75	xpd = xa-xk = 2.5mm
xa	16.25	xpd = xa-xk = 2.5mm
yp	2.0	from tile's edge
d1	2.55	Clearance fit. NDK. pins nominal 2.5mm
d2	2.55	Clearance fit. NDK. Pins nominal 2.5mm
dc	0.75	has to compensate the tolerances between SiPM pins and alignment pins. Diameter of SiPM pins: 0.25mm





Is this correct? Or are the positions of "Bias" and "Sig_Out" vice versa?

100-150 prototype tiles (
Problems with SiPM asse

Tile's dimensions are fixed now! (=>HBU)

Tiles for EUDET module

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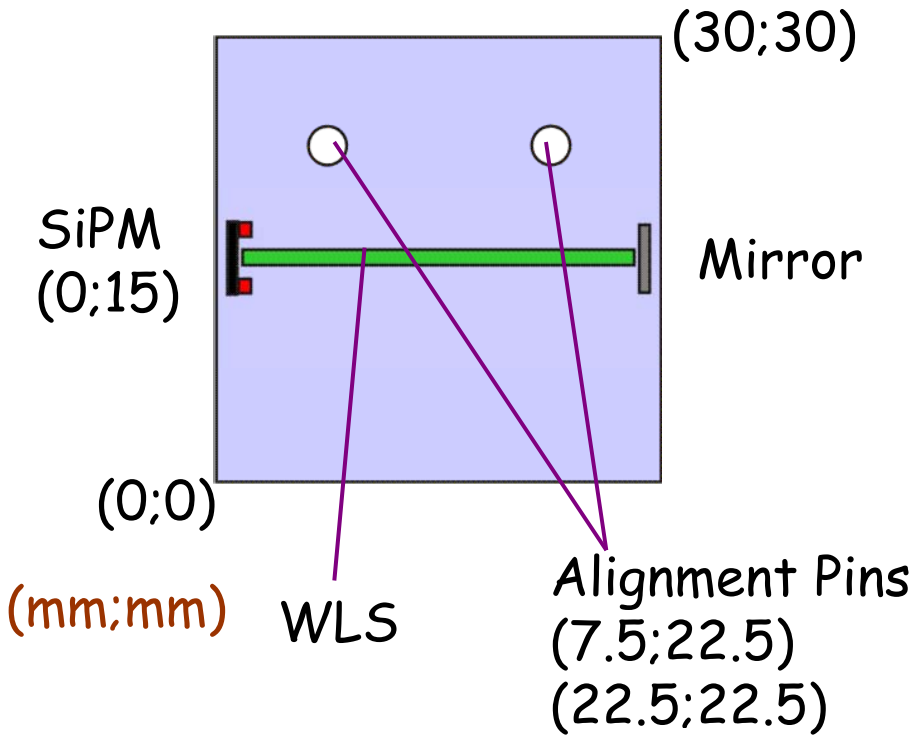
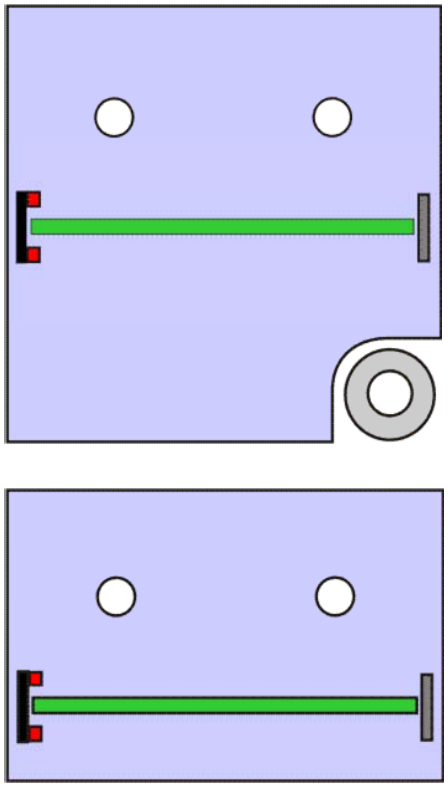
Standard Tile (moulded)





Shorted (by 1cm) tile for inter-layer sizes

No time schedule up to now.

HCAL Base Unit (HBU0)

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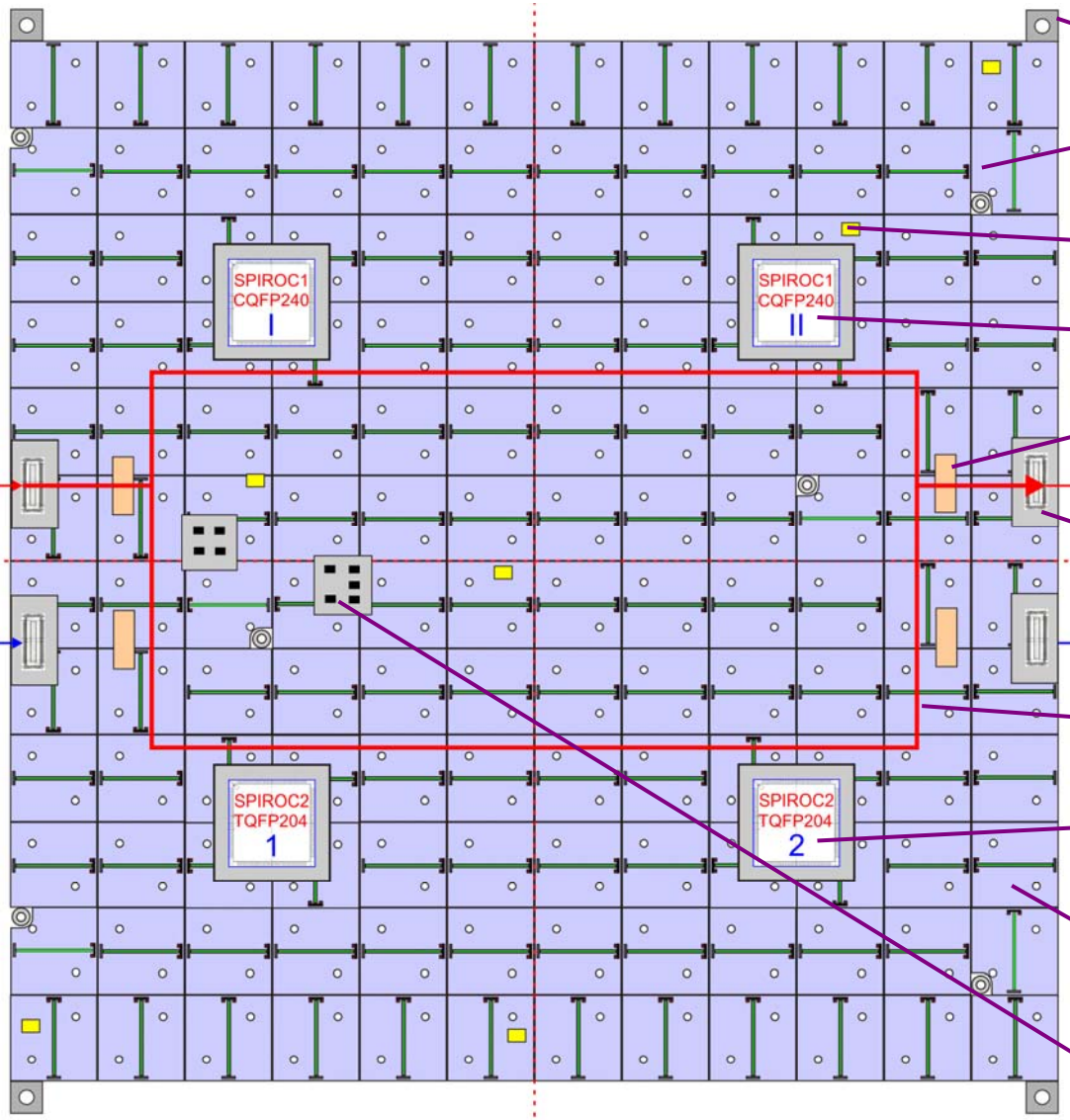

Cassette fixation

Mechanics Tile

Temp. Sensor

SPIROC1

Debug Conn.

Flexlead Conn.

Signal IN

Power IN

Two signal paths

SPIROC2

Prototype Tile

Calibration Electr.
(LED + Charge Inj)

HBU0 Status

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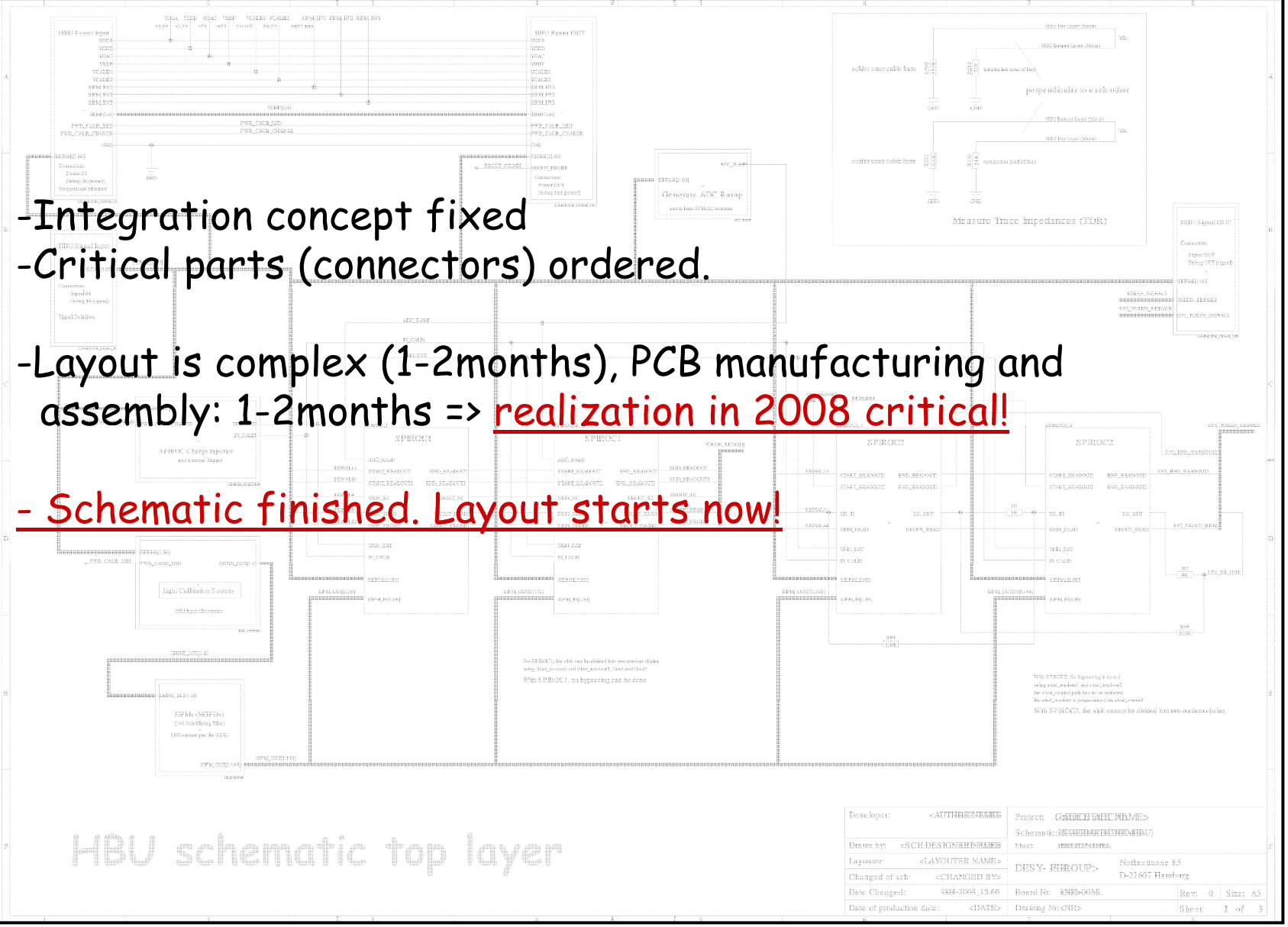

-Integration concept fixed
-Critical parts (connectors) ordered.

-Layout is complex (1-2months), PCB manufacturing and assembly: 1-2months => realization in 2008 critical!

- Schematic finished. Layout starts now!

HBU Interconnection (Flexleads)

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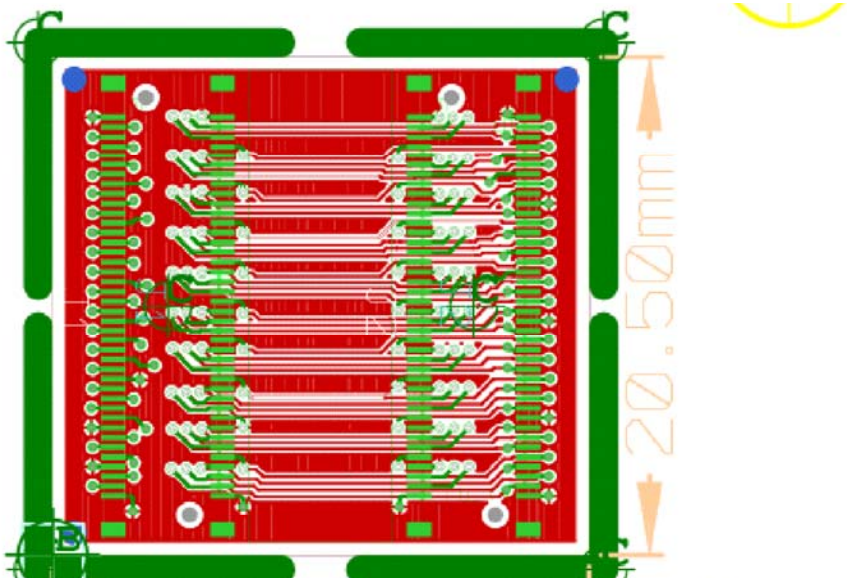
-Two types of Flexleads (for Signals, Power) have been designed (CAD)

-Flexleads allow +/-100µm displacement of connecting modules

-Magnet-field tests up to a few Tesla done: no problems seen.

-Flexleads can be ordered now!

Done!



Flexlead CAD Layout

DIF Status

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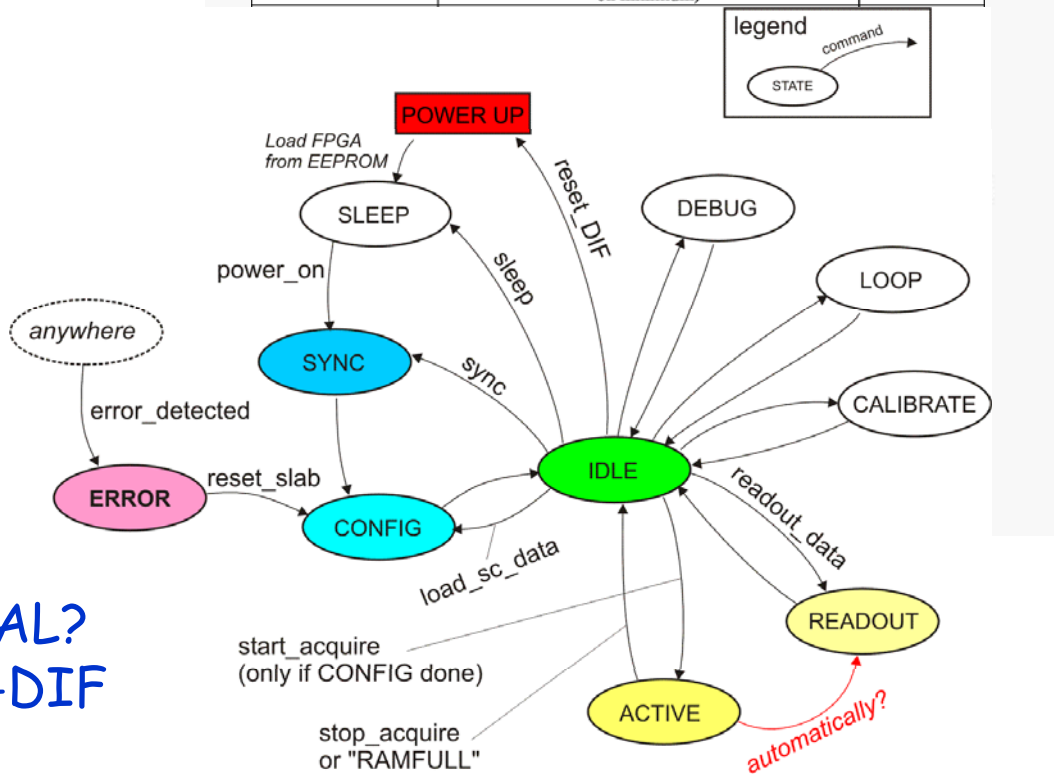
-Based on commercial FPGA (Spartan3-1500) board

-Command list and DIF state diagram in preparation

-VHDL code generation soon (prototype firmware for USB access in 2008)

Command	Function and Parameters	Change DIF State?
power_on	turn slab power on / off (maybe partly?)	no
reset_DIF	reset of DIF electronics (not: slab)	yes
reset_slab	reset of slab (ASICs). Not: DIF	yes
reset_BCID	synchronize data taking by resetting bunch counter	no
sleep	puts DIF and slab into SLEEP state (powered down)	yes
sync	synchronization LDA all DIFs	yes
idle	puts DIF into idle state (DIF power on, slab power on minimum)	yes



DIF state diagram

Firmware status of ECAL/DHCAL?
Reference documents for LDA-DIF interface (also: DAQ group)?
Firmware development needs closer coordination.

CALIB Status

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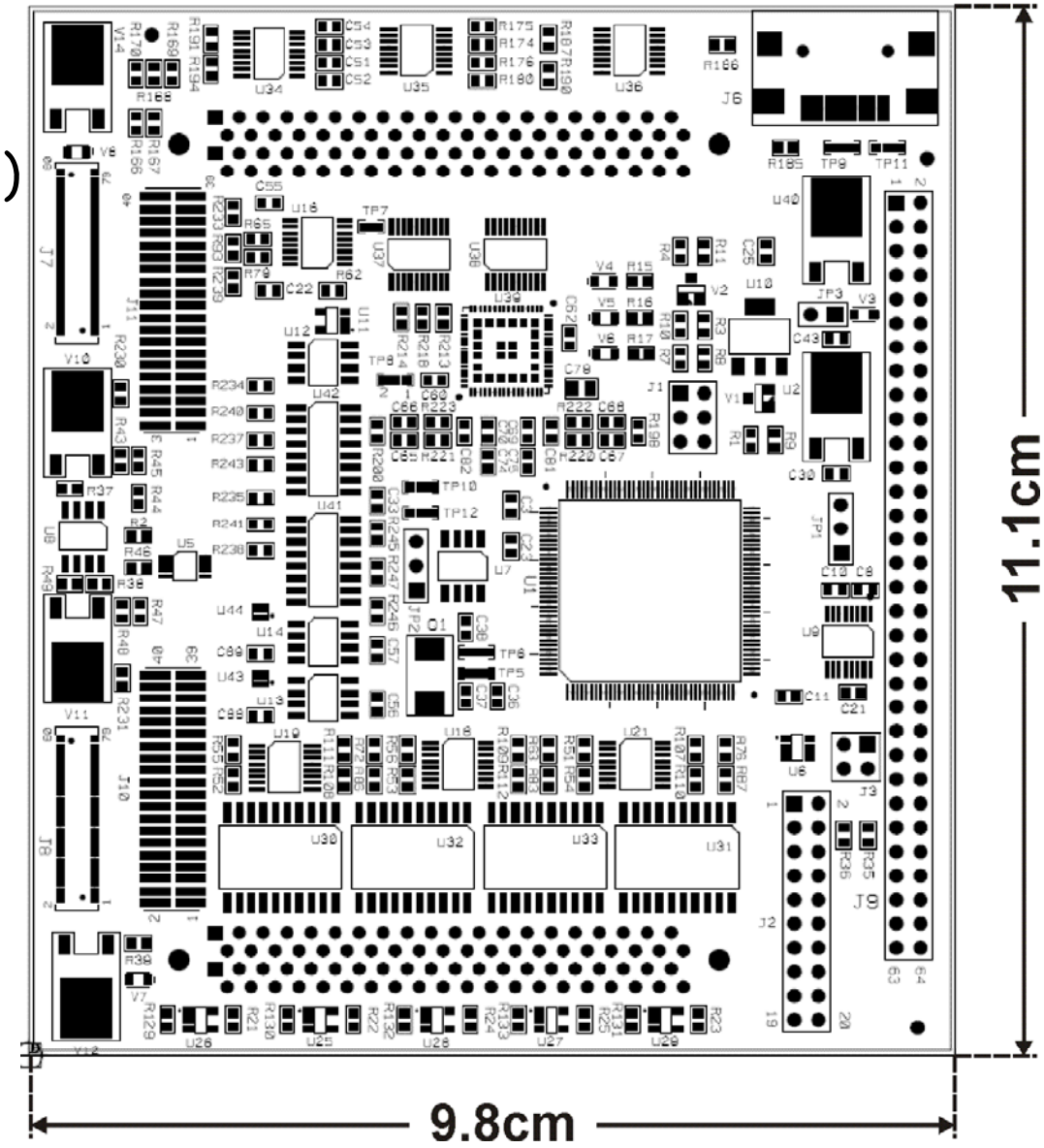
„AHCAL Calibration System“
(UV-LED and Charge Injection)

-Concept fixed, schematic finished

-µController software dev. ongoing (good progress)

-Layout (CAD) ~~starts~~ now, expected ~~to~~ be finished: ~~End of~~ September.

-Module should be available: November/December 08



POWER Status

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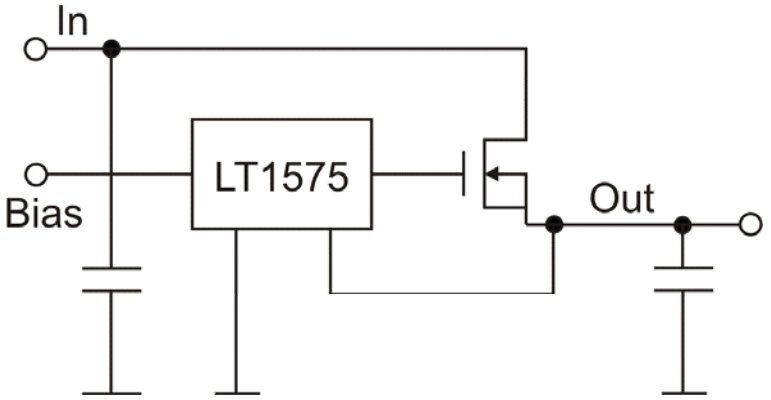
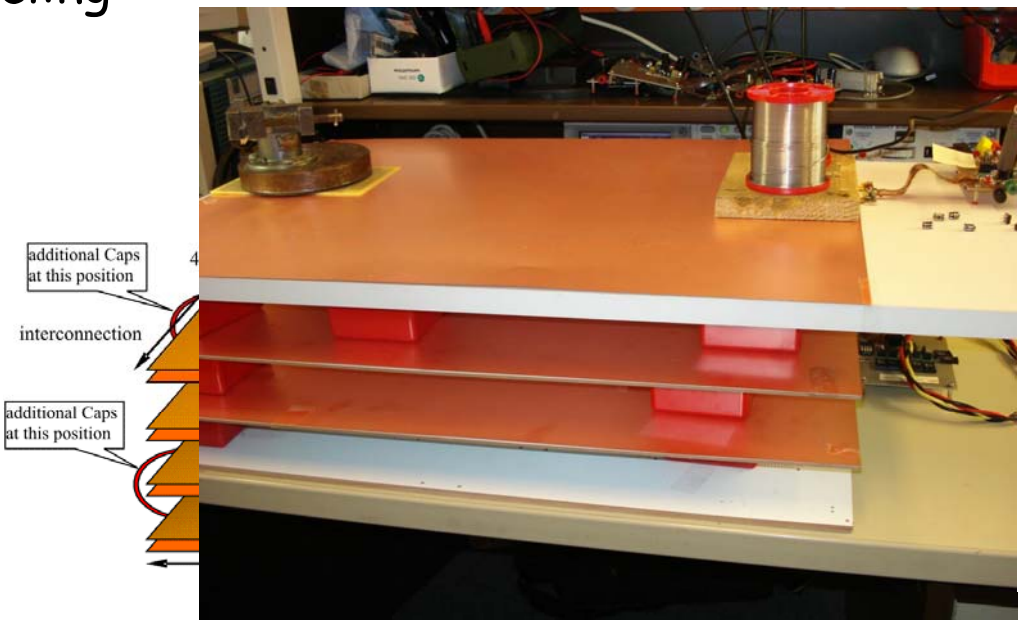
„AHCAL Slab Power Regulators"

-Regulator setup fixed, schematic finished

-Suitable for ILC-like power cycling

-Layout and Production probably in 2009 (module can be replaced initially by bench-top power supplies)





By
H. Wentzlaff

AHCAL Slab Interface (Mech.)

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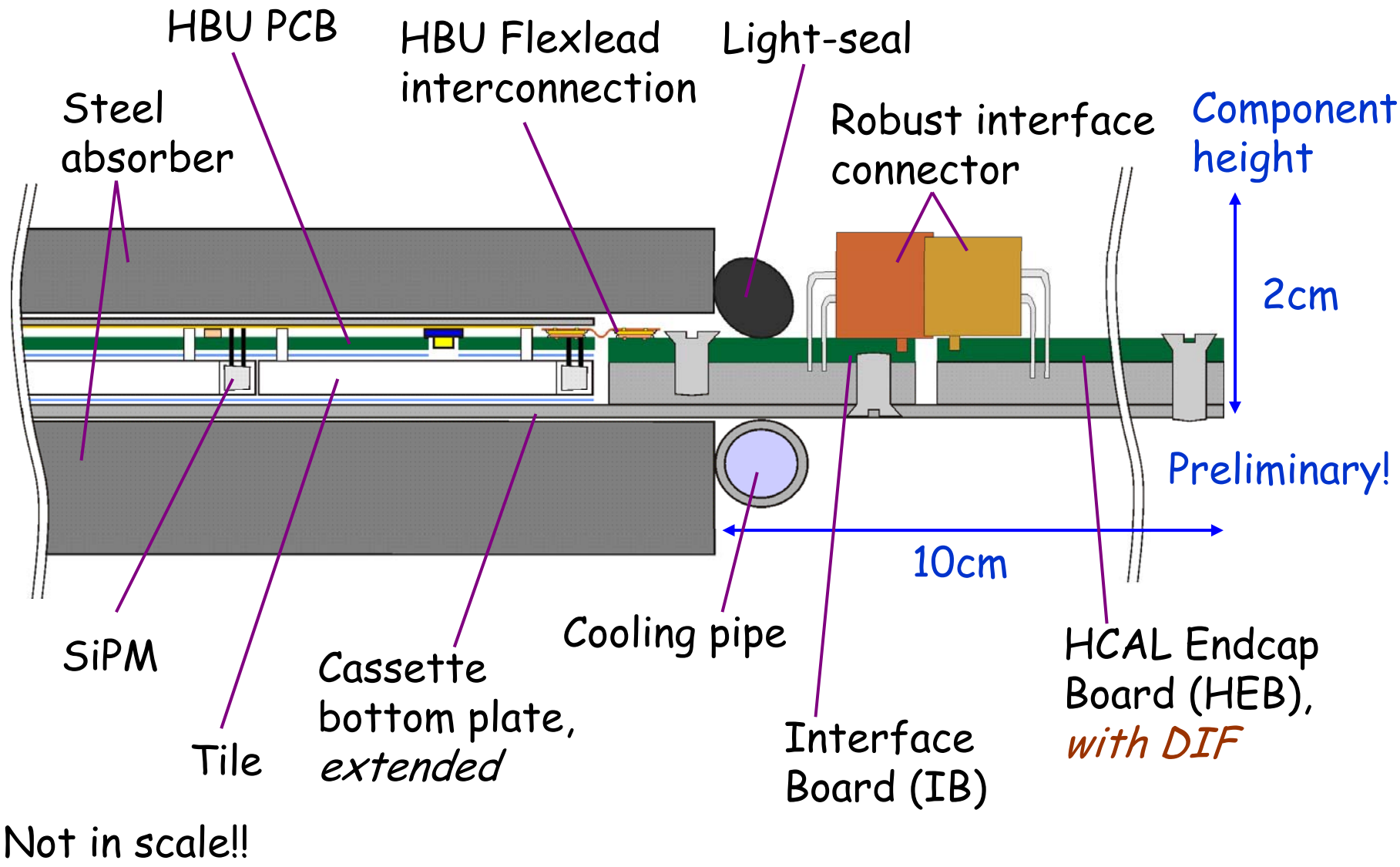

DAQ – Data Rates (Testbeam)

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New tool available (Vincent Boudry) to calculate CALICE DAQ data rates and readout times for the run modes:

- calibration/noise/physics – single event (e.g. ext trigger)
- calibration/noise/physics – burst (internal trigger)
- **testbeam – single event*** (e.g. external trigger?)
- **testbeam – burst*** (e.g. internal trigger)

***Occupancy needed** to estimate the amount of data.

AHCAL – Occupancy in testbeam

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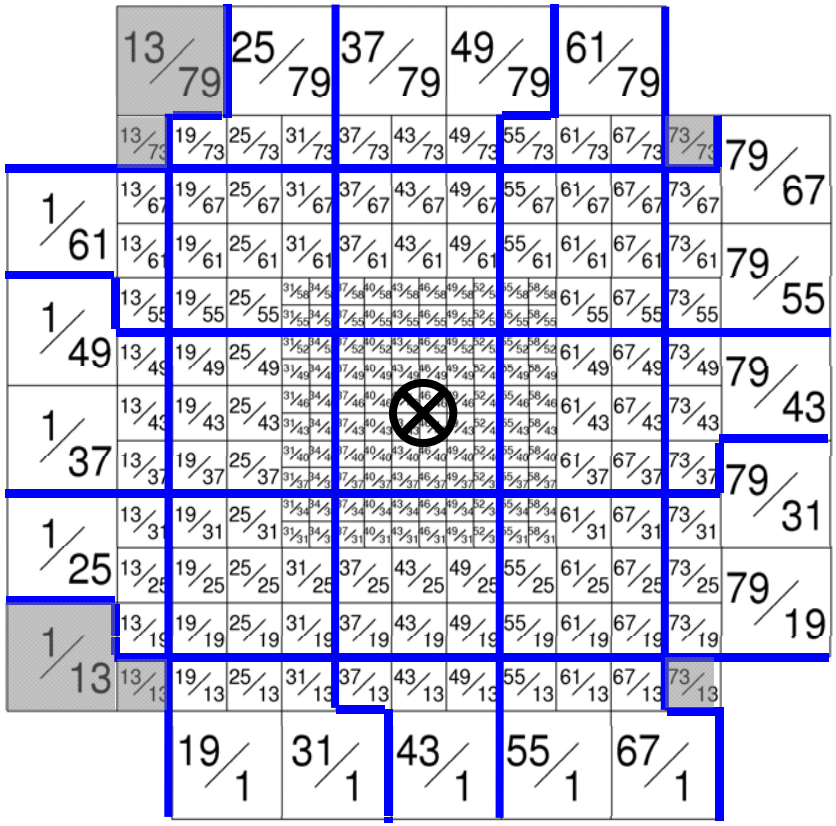
Calculation and Results by B. Lutz (many thanks!!)



- subdivided each layer into 21 sections
- each section corresponds to one virtual chip (36 channels with 3x3 cm cells)
- 798 total virtual chips (38 layers)
- 80 GeV π+ beam hitting centrally
- counting active chips per event

AHCAL – Total Number of ASICS hit

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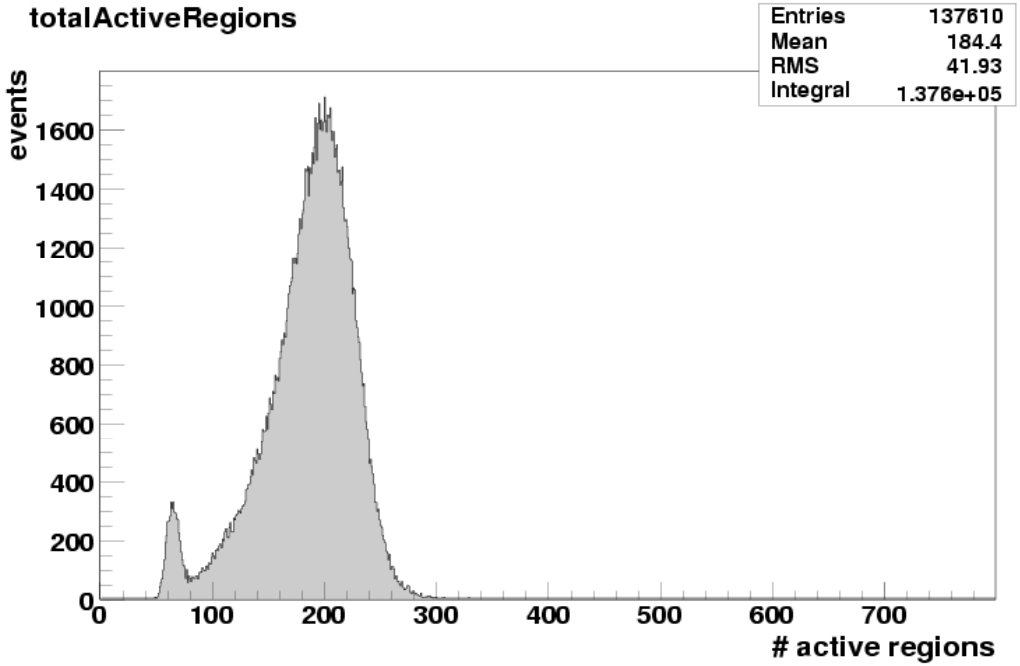

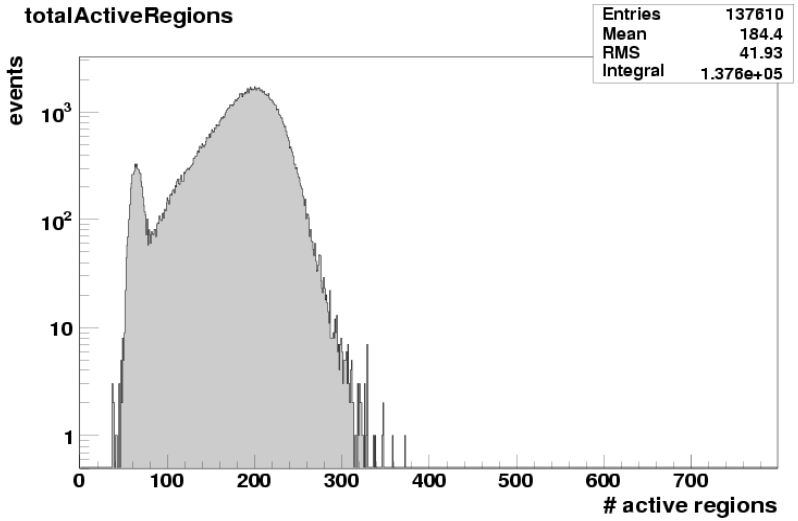

- typically 200 / 798 = ¼ of the chips in 1m^3 are hit

AHCAL – Active ASICs per layer

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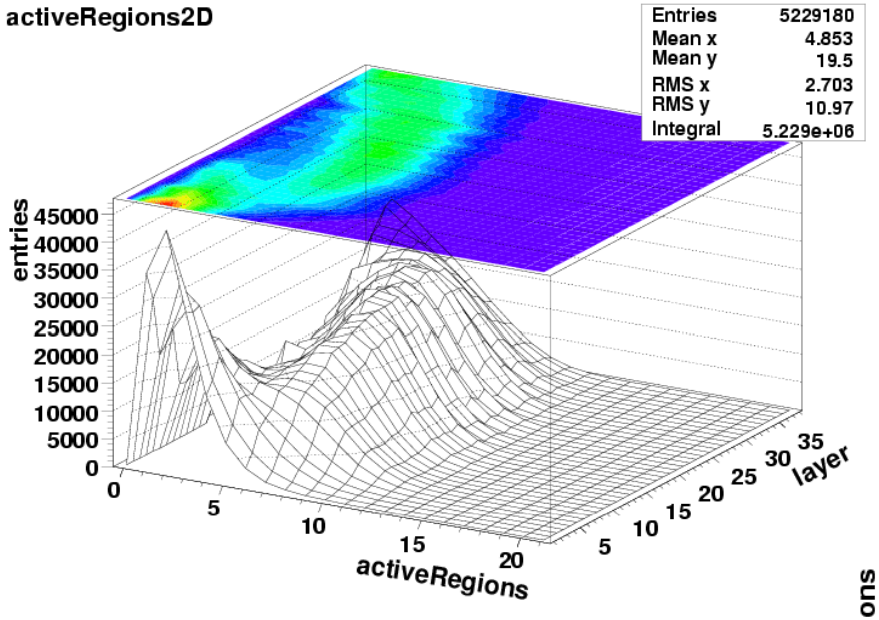
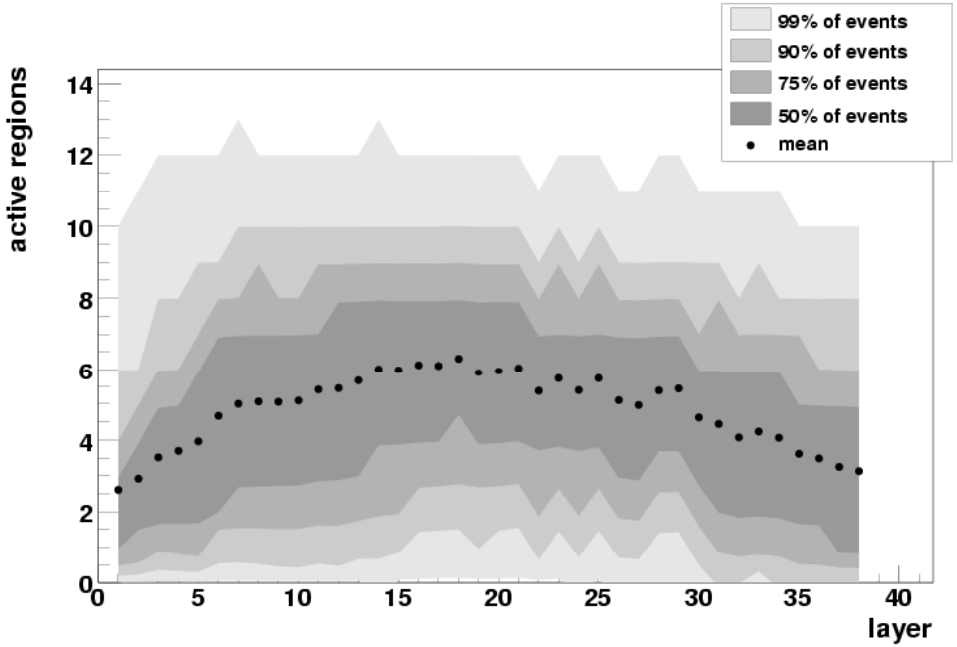


activeRegion: 36tiles (1 virtual ASIC)



Up to 12 ASICs carry data for a single testbeam event per layer. => use this number to estimate DAQ data rate!

Mechanics Status

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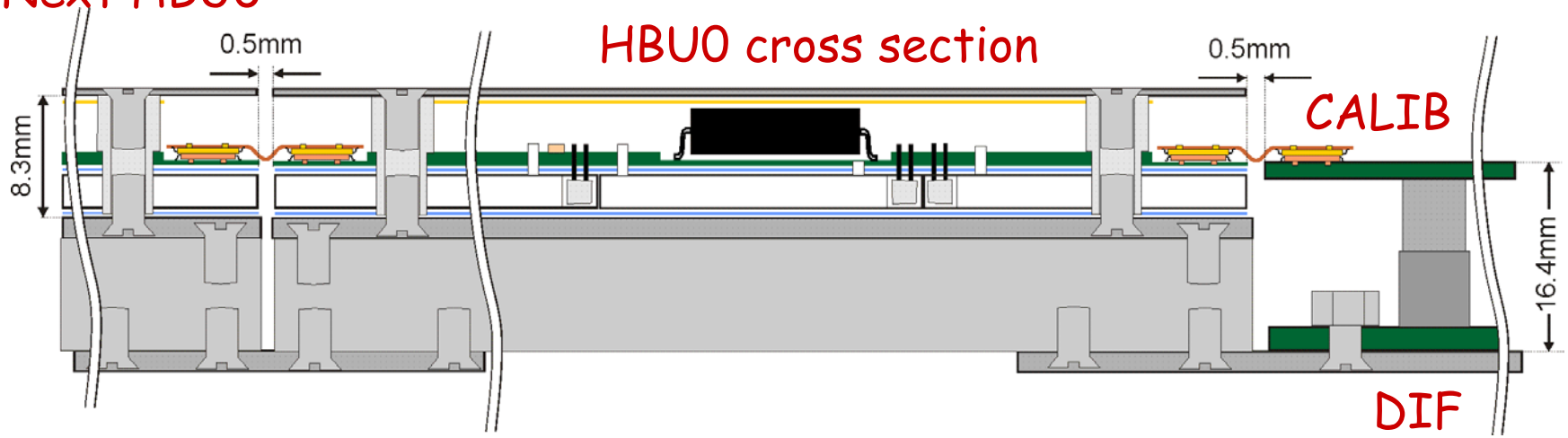
Next HBU0



- Mechanical proposal (cassette, interface to DIF) has been set up for the AHCAL prototype (HBU0, DIF as commercial board).

-The necessary mechanical parts are currently designed within CAD tool => production within 2008

Conclusions

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-AHCAL technical prototype (TP) does not cover a full slab, but ~150 channels (2 HBU0s, tile-prototypes).

-Eudet module (detector layer) requires HBU redesign. A full slab (and detector layer) is expected for summer/autumn 2009.

-timeline for TP is defined by HBU0.

-development of the modules CALIB and DIF (firmware) in 2008 possible.