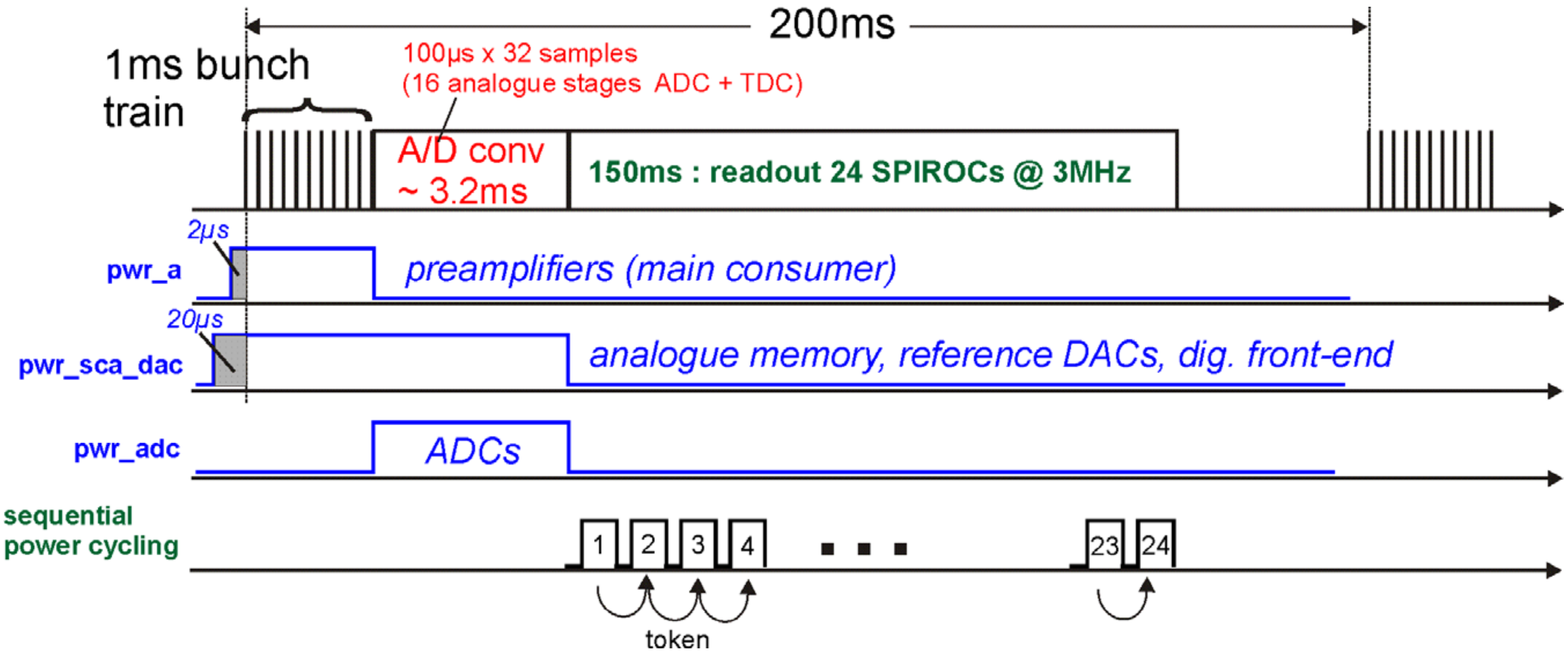
AHCAL Power Aspects

P. Göttlicher, M. Reinecke, H.-J. Wentzlaff

for the AHCAL developers

AHCAL switch-on time



ILC bunch train rate: 5Hz

SPIROC: Main consumer is preamplifier!
=> good approx.: AHCAL switch-on time = ~2ms (1%)

AHCAL: In-Detector Power

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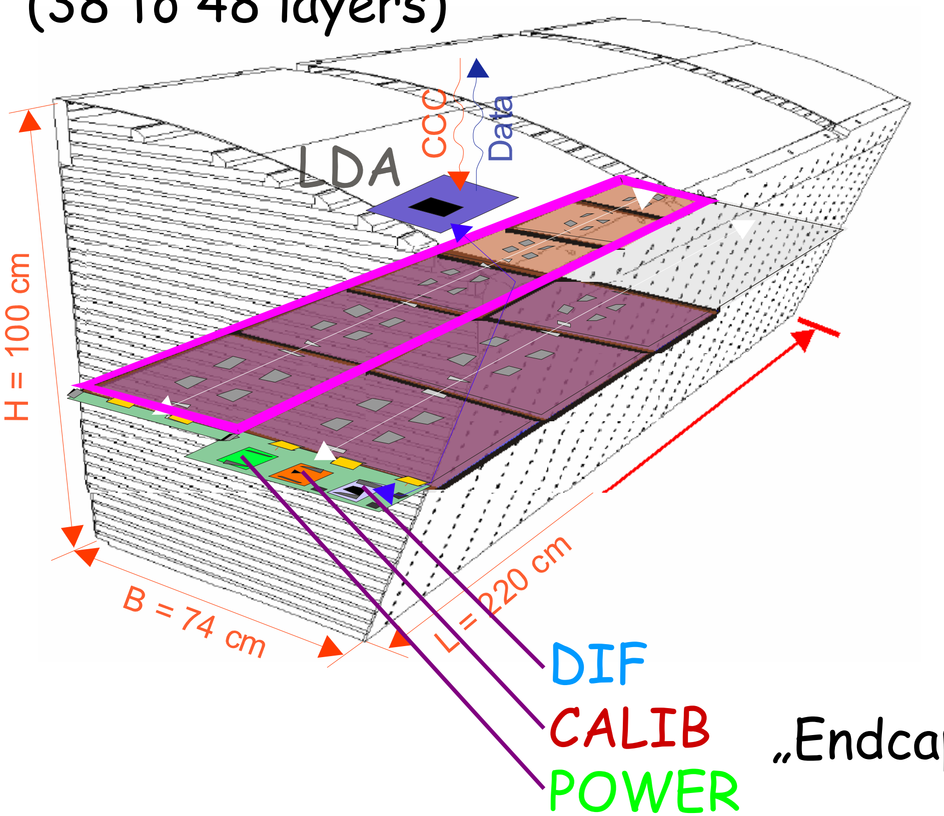
1/16 of half barrel
(38 to 48 layers)



„Endcap Power“

Typical AHCAL layer:

P_{ASIC} = 25µW/chn (1% on-time)
P_{SiPM} = 50V*0.3µA = 15µW/chn
P_{LCS} = 2µW/chn (rather vague)

N_{chn} = 2592 (in 3 full slabs)

=> P_{layer} = ~110mW (1% on-time)

This does not seem to be much, but the power is „trapped“ inside layer (i.e. no „air-flow“).

AHCAL: Endcap Power 1%

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AHCAL input voltages: +6V, +12V, +60V (SiPM bias)

Nr	Baugruppe BG	Anz.	Applikation -Bez.		aus ext. U_e [V]	U_{out1} [V]	U_{out2} [V]	I_{out} [mA]	I_{out} [mA]	Abfall U_{regler} [V]	Abfall U_{regler} [V]	Verlust P_{Regler} [W]	P_{Nutz} [W]	P_{Quelle} [W]
	SLAB													
1		1	VDDA	LP3876ES-ADJ	6,0	3,5		11		2,50		0,0275	0,039	0,066
2		1	VDDD	LP3876ES-ADJ	6,0	3,5		7		2,50		0,0175	0,025	0,042
3		1	VDAC	LP3874ES-ADJ	6,0	5,0		1		1,00		0,001	0,005	0,006
4		1	VREF	REF194ESZ	6,0	4,5		1		1,50		0,0015	0,005	0,006
5	10V/50V	1	HV1	LT3010EMS8E	60,0	10,0	50,0	4	4,00	50,00	10,00	0,2	0,04	0,24
6	10V/50V	1	HV2	LT3010EMS8E	60,0	10,0	50,0	0	0,00	50,00	10,00	0	0	0
7	10V/50V	1	HV3	LT3010EMS8E	60,0	10,0	50,0	0	0,00	50,00	10,00	0	0	0
	CALIB									Sums		0,2475	0,113	0,36
8		1	VCAL11	LT1763CDE	12,0	11,0		20		1,00		0,02	0,22	0,24
9	3,5Volt?	1	VCAL3V3	LT1763CDE	6,0	3,3		300		2,70		0,81	0,99	1,8
	DIF									Sums		0,83	1,21	2,04
10	3,5Volt	1	VDIF3V3	LT1763CDE	6,0	3,3		400		2,70		1,08	1,32	2,4
11		1	VDIF2V5	LT1763CDE	6,0	2,5		100		3,50		0,35	0,25	0,6
12		1	VDIF1V2	LT3021EDH-1.2	6,0	1,2		100		4,80		0,48	0,12	0,6
	POWER									Sums		1,91	1,69	3,6
13	3,5Volt	1	VPWR3V3	LT1763CDE	6,0	3,3		500		2,70		1,35	1,65	3
14	AD1	1	VPREF	REF196GSZ	6,0	3,3		10		2,70		0,027	0,033	0,06
15	AD2	1	VPREF	REF196GSZ	6,0	3,3		10		2,70		0,027	0,033	0,06
16	AD3	1	VPREF	REF196GSZ	6,0	3,3		10		2,70		0,027	0,033	0,06
17	AD4	1	VPREF	REF196GSZ	6,0	3,3		10		2,70		0,027	0,033	0,06
18	AlleADs	1	VPREF	REF192GSZ	6,0	3,3		10		2,70		0,027	0,033	0,06
										Sums		1,485	1,815	3,3
									Total Power			4,4725	4,83	9,30

By H. Wentzlaff

Total Power of 1 AHCAL layer @ 1% switch-on time

AHCAL: Estimated Power

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AHCAL voltages: +6V, +12V (calibration system), +60V (SiPM bias)

1% duty cycle (typical layer):

$P_{total, layer}$ = 9.3W (effective power (**ep**) + power dissipation)
P_{3slabs} = 113mW (in-detector, ep)
P_{calib} = 1.2W (ep)
P_{dif} = 1.7W (ep)
P_{power} = 1.8W (ep)

I_{3slabs} = 1.85A (current into detector when on- 1% of the time)

100% duty cycle (typical layer):

$P_{total, layer}$ = 21W (effective power (**ep**) + power dissipation)
P_{3slabs} = 6.84W (in-detector, ep)
P_{calib} = 1.2W (ep)
P_{dif} = 1.7W (ep)
P_{power} = 1.8W (ep)

I_{3slabs} = 1.85A (current into detector, 100% of the time)

Power Pulsing Tests

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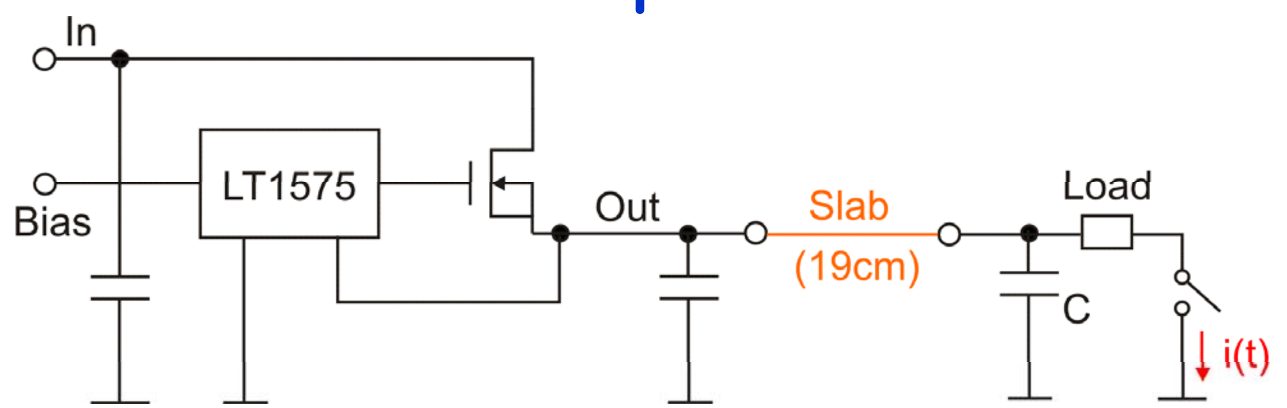
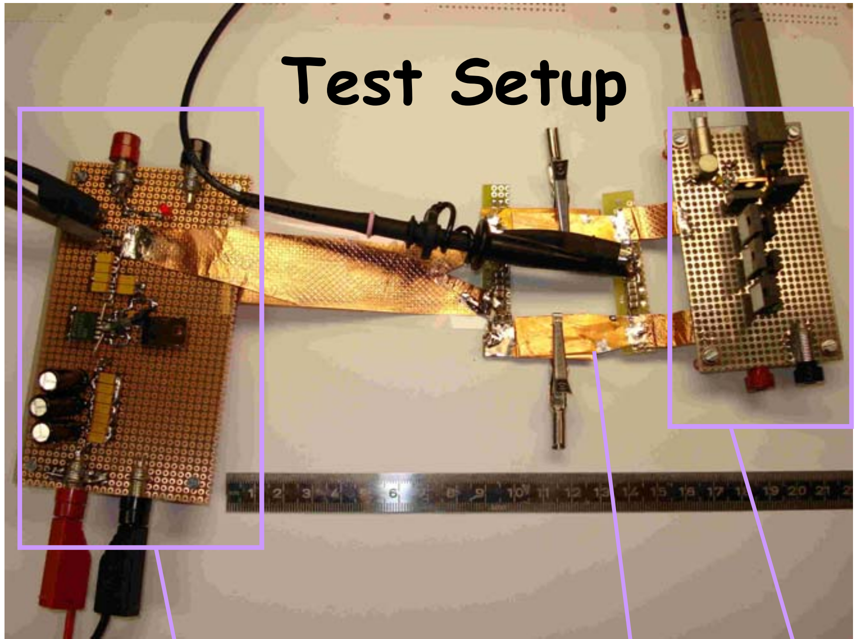
Detector electronics (Load) is switched between „off" (no current) and „on" (full current) with 1% duty cycle.
=> Oscillations on 2.20m-long power-ground system?

Test Setup



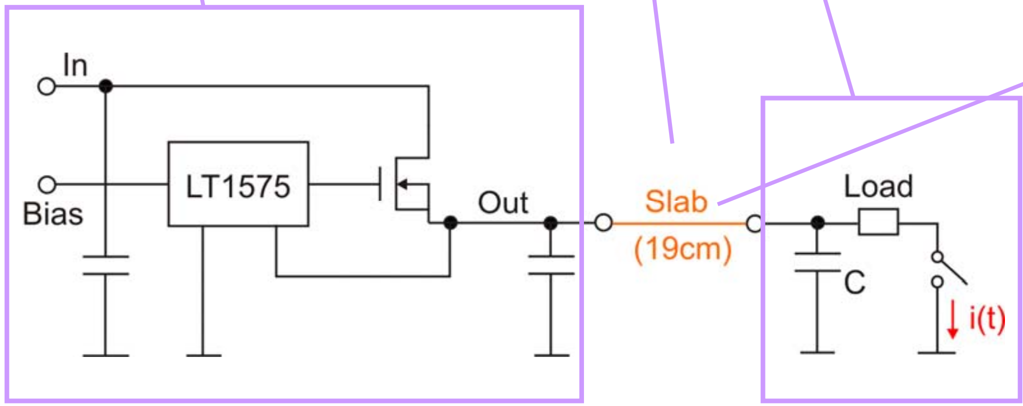
Tested:
Switched Current: 0.7…3A
Load Block Caps : 0…10µF (later: distributed in gap)

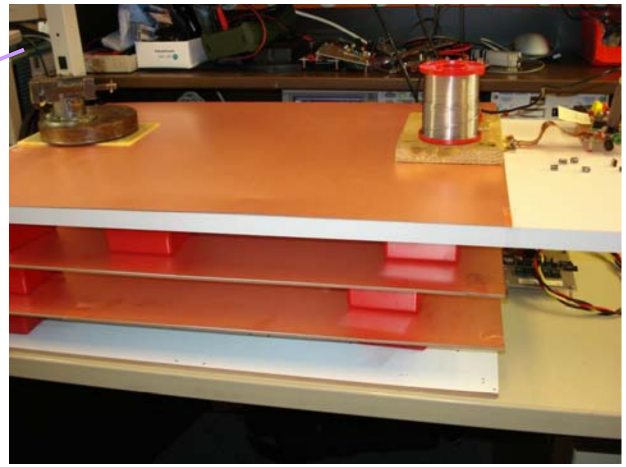
Power cycling test setup



<u>Settling time (Load side):</u>
Voltage within 50mV of final value.
Aim: reasonable values for efficient power cycling (< 50μs)

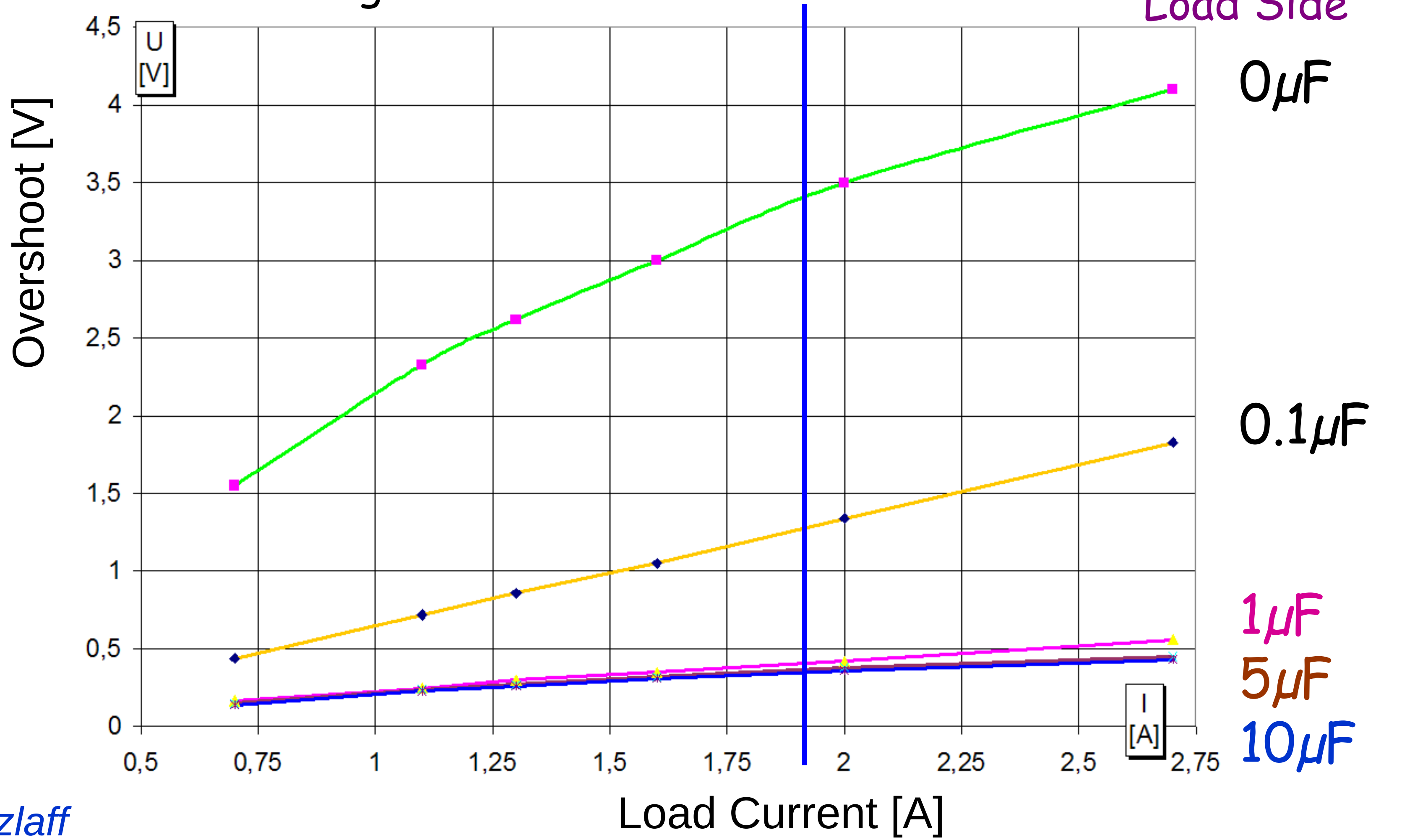
<u>Overshoot</u>
Aim: Protection of devices, stable register settings.





Power Pulsing: Results

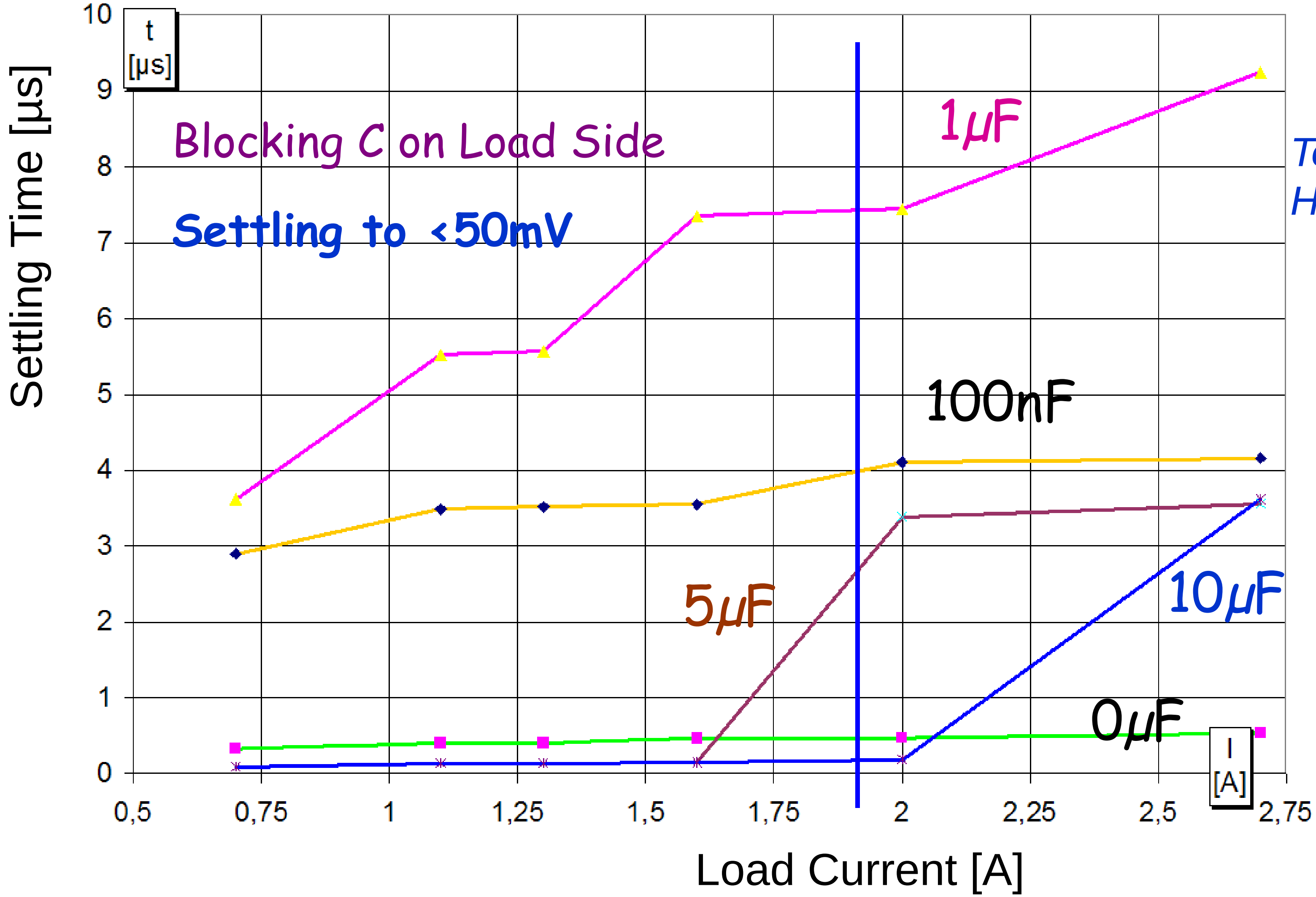
Typical results for overshoot (loadside), shown here for switch-off case (worst-case). Overshoot on regulator side: <150mV.



Test by H. Wentzlaff

Power Pulsing: Results

Typical results for settling time (loadside, **aimed: <50µs**)



Test by H. Wentzlaff

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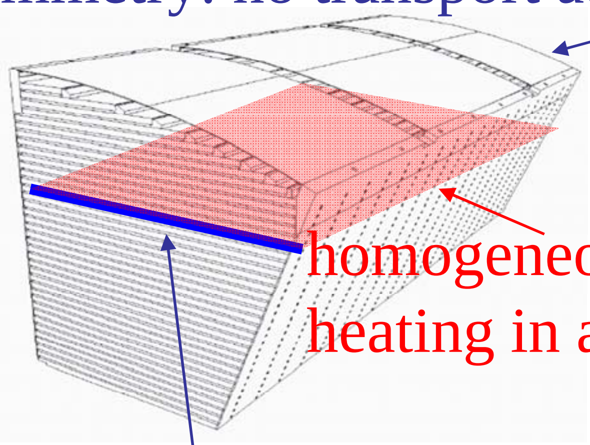
AHCAL: Stack Heating

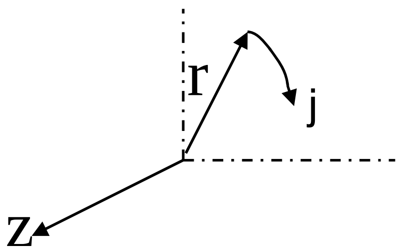
Calculation and Results by P. Göttlicher

symmetry: no transport at z=0m



homogeneous
heating in all gaps

cooling at the ends: z=±2.2m



Heat transport in directions:

j homogeneous heating:
➡ No heat transfer in j

r alternating structure
with air gaps
every air gap is heating
➡ No heat transfer in r

z cooling at end plate
Heat flows in solid material,
air gaps too small, no convection

AHCAL Slab Interface (Mech.)

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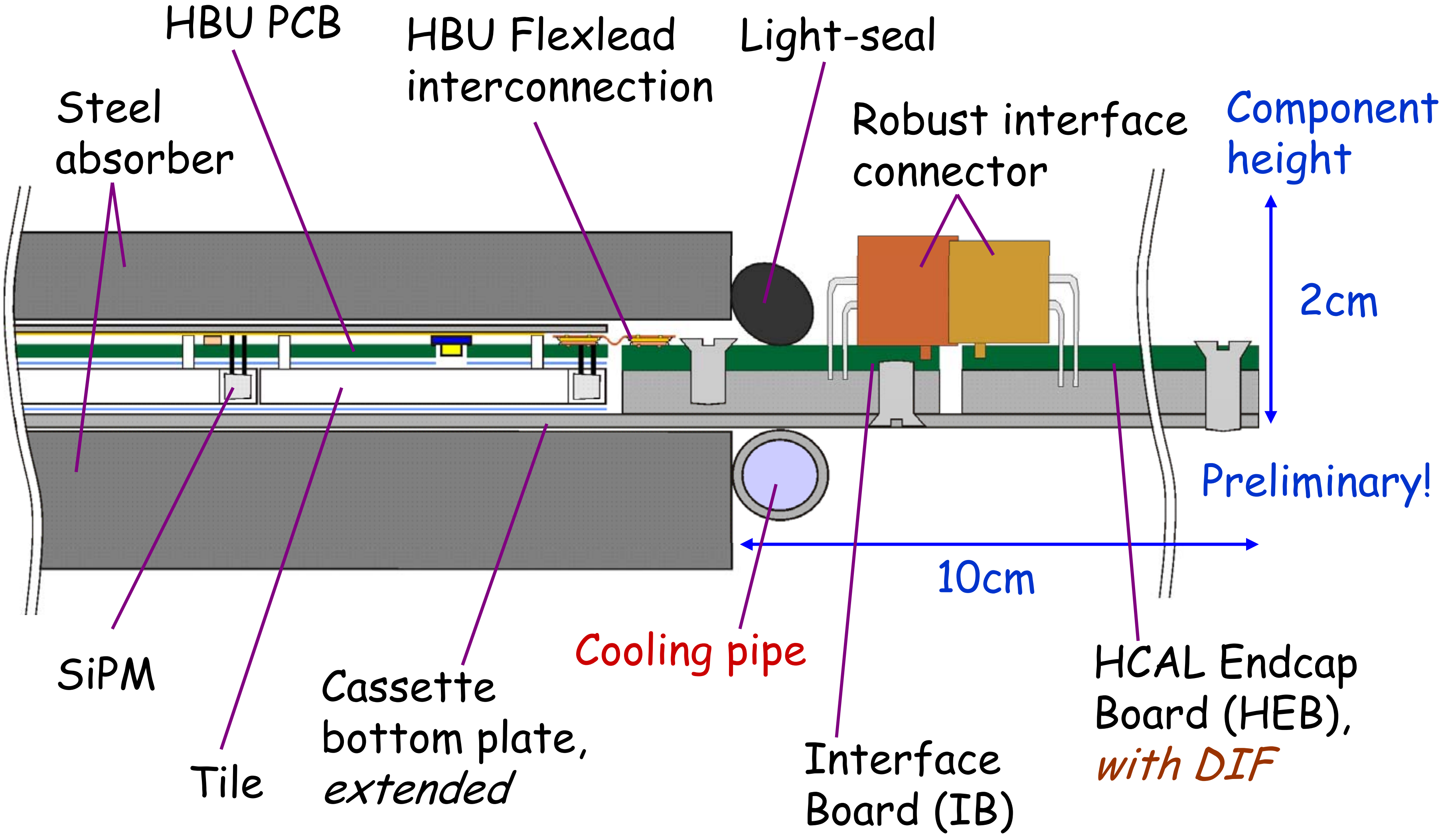

Not in scale!!

Basic Parameters

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Heat production:

Power: P_{chan}=40mW/chan

ASIC: 25mW/chan

HV: +15mW/chan: 50V*0.3mA

Infrastructure: + ??

Geometry:

N_{chan} = 1000/m^2

D_{steel} =2cm (thickness)

L_{heat} = 2.2m (length)

A_{plane} = 2m^2

Material constants:

Stainless steel: Which one?

l_{steel} =15W/Km other publication 15-25W/Km

k_{steel} = 3.7MJ/m^{3}K

In detail see: P. Göttlicher „System aspects of the ILC-electronics and power-pulsing", Topical Workshop on electronics for Particle Physics (TWEPP-07), pp. 355-364, Prague, Oct. 2007

AHCAL heating: Results

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Temperature T for $\frac{\partial T}{\partial t} = 0$:

$$T \quad = \quad -(z^2 - L_{heat}^2)\,\frac{P_{chan} N_{chan}}{2\lambda_{steel} d_{steel}}$$

δT (z=0) = 0.33K

Time dependence (Fourier transformation with components parameterized by τ, α(τ)),

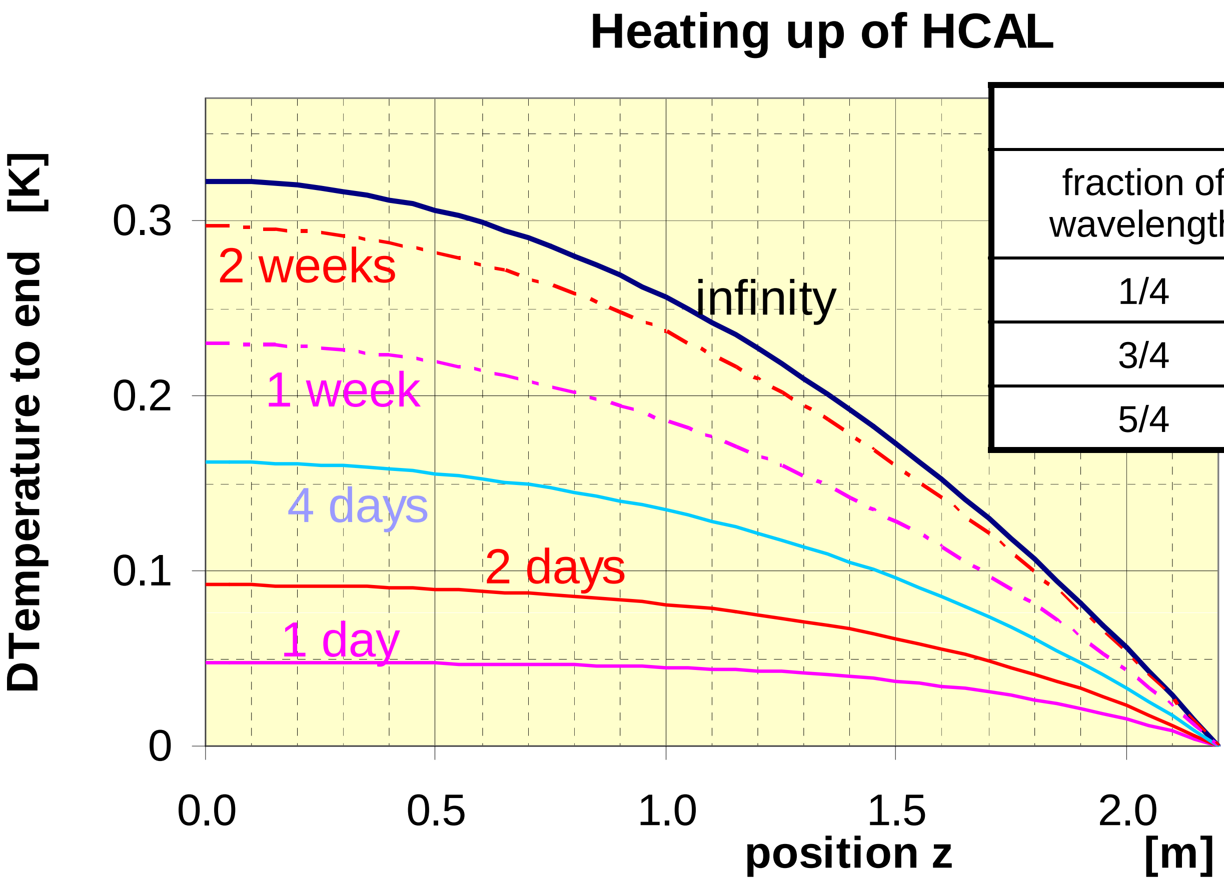
elements: A e-(t/τ) cos(2pα(x/L_{heat}))

One cooled end, and one with to heat flow: α= (1/4, 3/4, 5/4,....)

$$\tau \quad = \quad \frac{\kappa_{steel} L_{heat}^2}{4\pi^2 \lambda_{steel} \alpha^2}$$

Slowest component (α=1/4) : τ = 5.6days

AHCAL heating: Results



fourier components		
fraction of wavelength	time constant	relative amplitude
1/4	5.6 days	+ 103%
3/4	0.6 days	- 4%
5/4	0.2 days	+1%

Conclusions

-Heating of AHCAL stack is small (0.33K @ z=0), but cooling is needed at the end-cap (liquid cooling), external heating (e.g. ECAL) is not included in this calculation. Assumptions for the power dissipation correct?

-Time constant of heating is large (several days)

-Regulator setup enables small settling times (<10μs) and overshoots (<1V for 1μF blocking caps) for the ILC power pulsing.

-Power of one layer is small (1% duty cycle): 110mW per in-detector layer, 10W in total for one layer (preliminary).