	CALICE Electronics short meeting : minutes **DAQ and CCC** **Detector running modes** **Signals and synchronization**	Draft 0

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CALICE Electronics short meeting: minutes

DAQ and CCC

Detector running modes

Signals and synchronization

Held on Tuesday June 24

The purpose of this meeting was to have a first thought on the way the data would be acquired on the detector (EUDET test beam) and to agree on common definitions. Various consequences about clocking and commands have then be discussed.

The meeting started at 14:05 CEST.

List of the participants: Julie Prast (LAPP), Christophe Combaret (IPNL), Mathias Reineke (DESY), Bart Hommels (Cambridge), Matt Warren (UCL) , Franck Gastaldi (LLR), Remi Cornat (LLR), David Bailey, Marc Kelly, Adrian Vogel (DESY), Antoine Mathieu (LLR)

Agenda on Indico : http://ilcagenda.linearcollider.org/conferenceDisplay.py?confId=2817

1) LDA and CCC status (Matt and Marc)

Firmware has not evolved so much since the last collaboration meeting but work is ongoing.

The LDA board is being redesigned (bug found on the commercial board).

CCC and backplane: only a few CCC required so no need to be put on a backplane.

2) Running modes

Proposal of running modes definitions (Remi&Vincent) were made in order to clarify what we would like to do with the detector (see slides attached to the agenda).

2 major modes:

- Demonstrator (technological studies : power pulsing, thermal behavior,…) with ILC like conditions. This mode is probably required for EUDET but is not clear enough to be discussed in details (next CALICE week?).
- TestBeam/Physics : should allow to take as much (interesting) data as possible. 2 sub modes :
    - ⇨ Single event : interesting data are selected thanks to an external trigger then acquisition is stopped and chip read-out before to restart a new cycle (beam spill not finished). 2 options :

        - Only triggered channels (or chips) are stored (Physics)
        - The whole chips/detector ? is read-out (Noise and calibration)
    - ⇨ Burst : The ROCs acquire data in auto-trigger mode. Acquisition is stopped when a chip becomes full (ChipFULL signal) or with a command from DAQ.

Pending questions :

- Start of spill (Remi) ?
- Sensitivity to the noise level (Julie)? Internal trigger threshold settings ?
- Burst sub-mode : Do we really need to broadcast ChipFULL to the whole detector (Bart) to stop chips acquiring data ? (Read-out time is long compared to acquisition and the gain in the number of acquired events is not obvious)

Summary of the open discussion for the following points:

3) Clocks
   2 clocks for the ROCs : SlowClock and FastClock. The Fast clock is not necessarily the same as the one coming from LDA.
   The SlowClock is functionally the most important: shaping time, BXid, R/W in ROCs buffers. Its frequency is a sub multiple of the machine clock. The constraint is on stability not really on the jitter : 1 ns seem OK.

   The slow clock could be generated from a counter or from the LDA-DIF data link (comma characters are periodically sent to synchronize the link). This way have been tested (Marc). It allows to phase the clock according to the link (time steps corresponding to one bit).

4) Commands
   Need to clarify fast commands/very fast commands/commands (Bart) and a common vocabulary has to be found.
   - Very Fast commands : signals to be received on the DIFs or ROCs at the same slow clock edge everywhere with absolute time requirements. Typically the TRIGext signal. "Trigger and Fast Control"="TFC" ?
   - Commands : encoded signals to be received within the same slow clock period with no stringent requirements on the clock period number. "Commands"

   This definition of "command" constraints the clock frequency of the LDA-DIF link which have to be (the number of bit send for a command) times the slow clock frequency.
   E.G. : command on 20 bits (2 bytes + encoding) would need a link clock of 5 MHz*20 = 100 MHz.

   Need to establish the number of VFCommands and commands
   - ⇨ number of bytes to encode commands could have an impact on required clock frequency for the link)
   - ⇨ Number of dedicated wires for VFCommands onto the HDMI connector.

Questions about how to ensure the time alignment all over the detector.

- ⇨ Depends on the firmware (not written yet) but some confidence to have a spread of about 5 ns for VFcommands (data sheet of the LDA fpga)

Questions about the capability of ODR to generate VFcommands (or commands).

- ⇨ VFCommands are handled by CCC.

5) Busy

Busy signal (ChipFULL) is useful for the "burst" sub mode of the "TestBeam" running mode. It would allow the "detector" to stop acquisition everywhere and optimize the recorded event rate (quick restart of acquisition)

- ⇨ Feedback of busy state of a particular chip at the level of the detector

Inputs for this kind of signal foreseen at the CCC level.

Questions on how to transmit "Busy" from DIF to LDA : dedicated line or encoded commands?

- ⇨ Background question is the actual timing requirements to distribute "Busy" on the detector. No clear answer yet.
- ⇨ Need to have another VFCommand (Busy feedback to other chips !)

Question about the usefulness of a "quick restart" for the Burst sub-mode.

- ⇨ See point 2)

The meeting ended at 15:45.

Conclusion running modes and signaling: An attempt to define and have a common definition about running modes. Demonstrator mode will have to be defined and discussed. Common definition for commands and fast commands is required as well as the number of commands (list).
A lot of questions about timing and clocks (some ideas expressed during the meeting) would need another meeting soon.