EDAQ meeting: DAQ signals

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TB DAQ modes

Modes:

- **Physics**
  - as fast as possible IN SPILL, poissonian stat
  - “low occupancy” (particle type & E dependant)
- **Calibration / noise**
  - *a priori*: off spill, fixed rate
  - all cells
  -

- **Single Event**
- **Burst**

Analogue: Single Event only

- **centralised readout**
- **External trigger** (from hodoscope or calibration system)
  - Stop Acq, **Hold analog data** + sampling, Start Acq
- **Data sync** for Event building
  - sync of ADC cards

TB DAQ modes: single event with auto-trig

Using ROC chips: auto trigger, buffer (Hardroc: 256, Spiroc: 16)

Single Event + auto-Trig

- **External trigger** (hodoscope) → DIF
  - Stop Acq, Read chips, Start Acq
- **Data sync** (for Event building)
  - On synchronized BC ID → **need for a SYNC @ MClk (100– 400 ns)**
  - On trigger timestamp (e.g. On DIF Timecounter on last internal trigger to ext. trigger)
  - **BUT: for the AHCAL/Spiroc:** the TDC signal needs a SYNC of the clocks **±1ns**

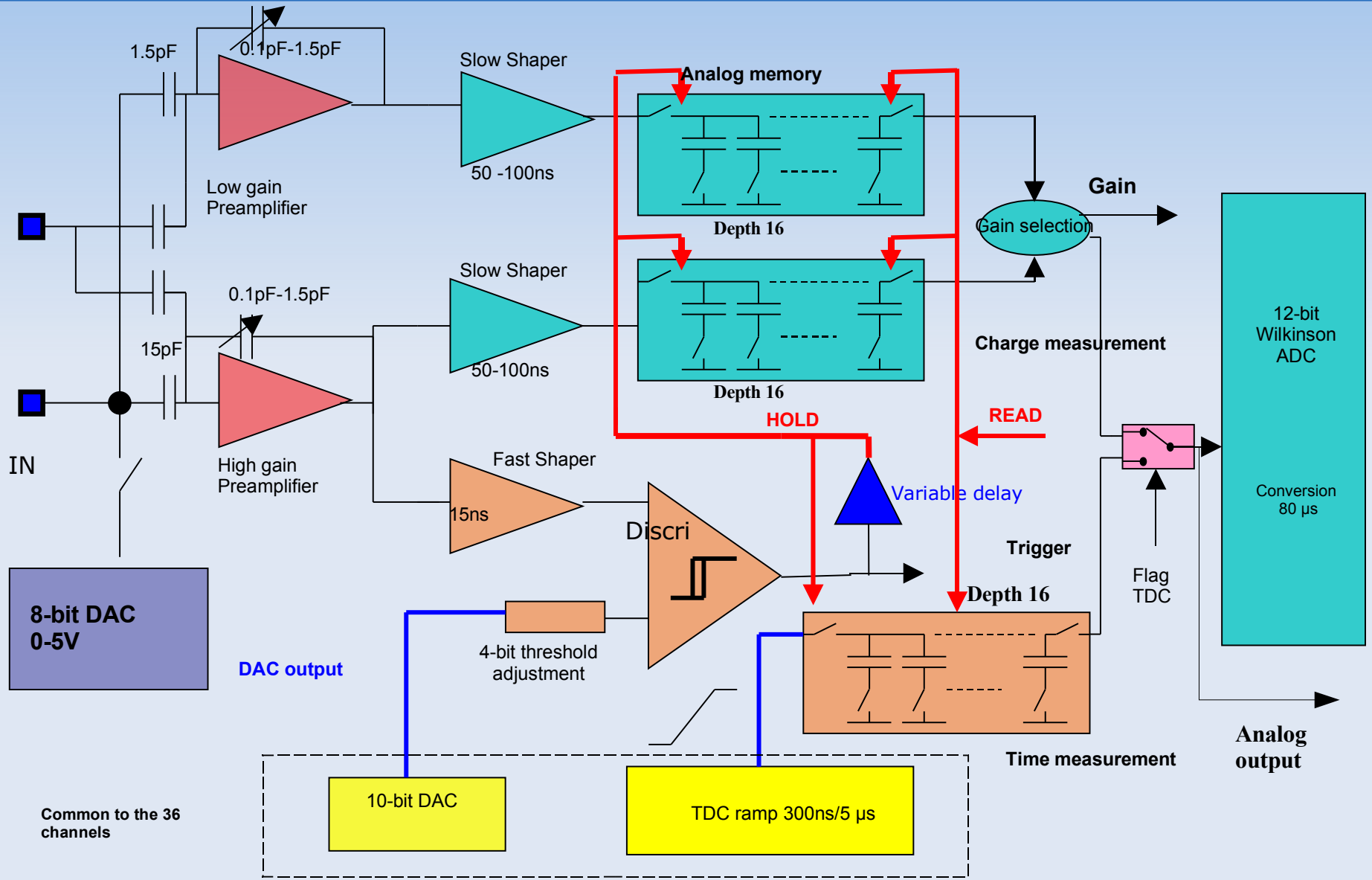
Single events “in phase” : Noise runs

- need a fast trigger (δ<1ns ???? TBC)

Rems:

- Fine if no RAM full
  e.g. # rejected triggers + noise event per chip < 128 [16 for the ECAL/AHCAL!]
- Sync can be x-check by a BC counter in the DIF's

SPIROC diagram



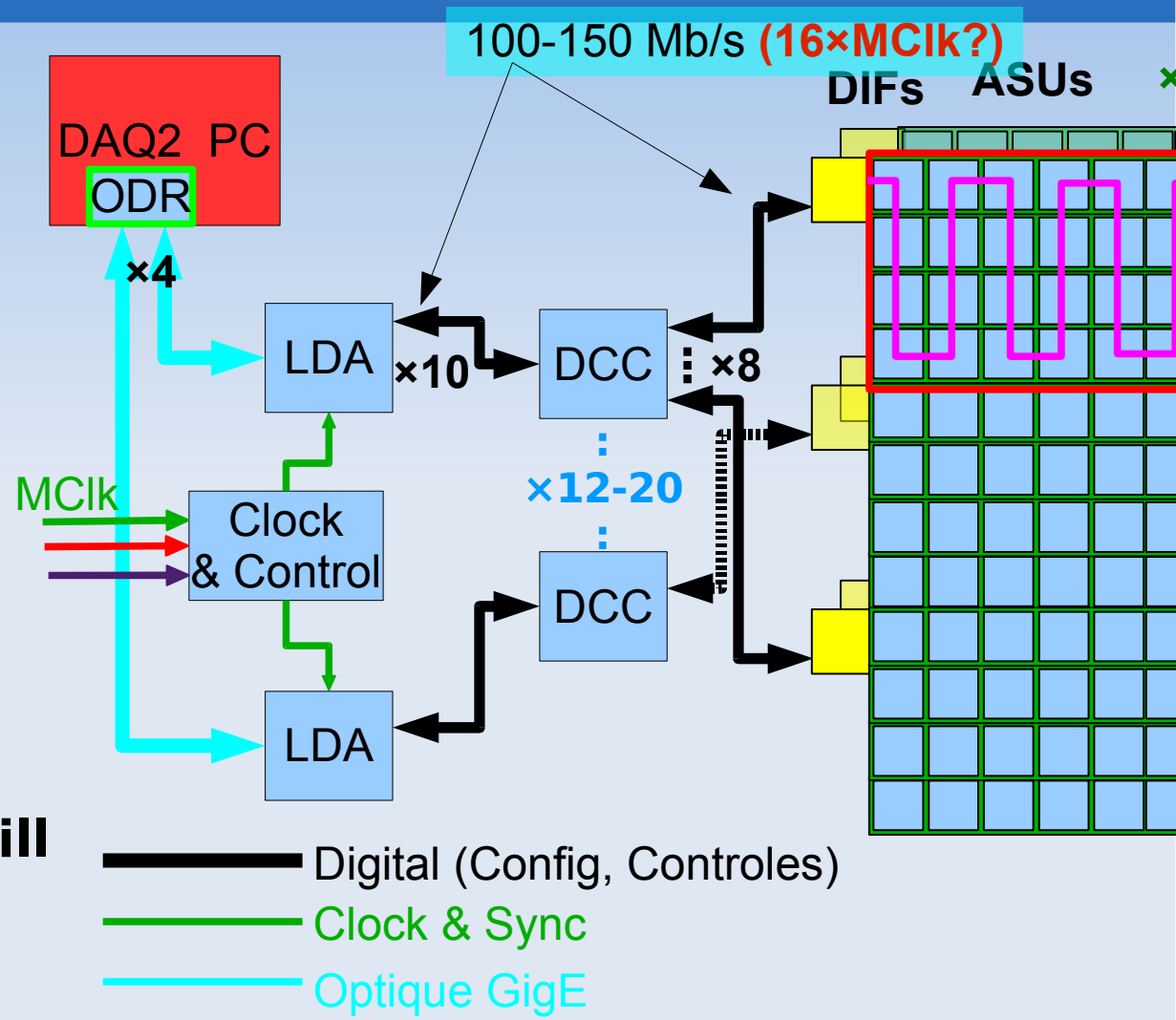
TB DAQ modes

Burst mode (≤128 FOR DHCAL): *TB data, Calibration, ILC*

- **No external trigger** but independent recording of trigger mode (⊃ Timestamp)
  (could be 1 HR recording Trigger bits)
- Data sync internal [synchronisation on reset of BC ID on all HR], at the Beg of A LF
- Internal «RAM full» management needed
  Every 128 DHCAL [ECAL: 16] events
  - **LOCAL**: in DIF with immediate RO of SLAB
    - 4 ms for 100 GeV π's without Reset (avoid loss of sync)
    - **Indiv DT**: might be hard too handle.
    - ~~Local storage of data ????~~
  - **Global**
    - fast Ramfull → DAQ (stop of Acq, RO of all chips, and restart)
    - periodic interruptions
    - counting of part: for example one Hardroc for the Hodoscope → RAMfull

Signals

- **Clock**
  - Machine Clock (Mclk) ×16 on data (?)
  - MClk rebuild in DIF's from Data clock (?)
- **fast sync**
  - ≤ 1 MClk (≤1 ns if TDC's)
  - SpillSTART ?
- **External trigger**
  - δ ≤ 1 MClk
- **StartAcq/StopAcq/EndSpill**
  - from ODR
- **BUSY**
  - RamFull: DIF→LDA→C&C→trig
  - LDA → ODR (⇒ End of RO)



Propositions

Trigger

- have a simple logic in the C&C card:
  - OR(trigger inputs) AND !OR(BUSY)
  - could go to the DIF as a *fast command*

Fast signals

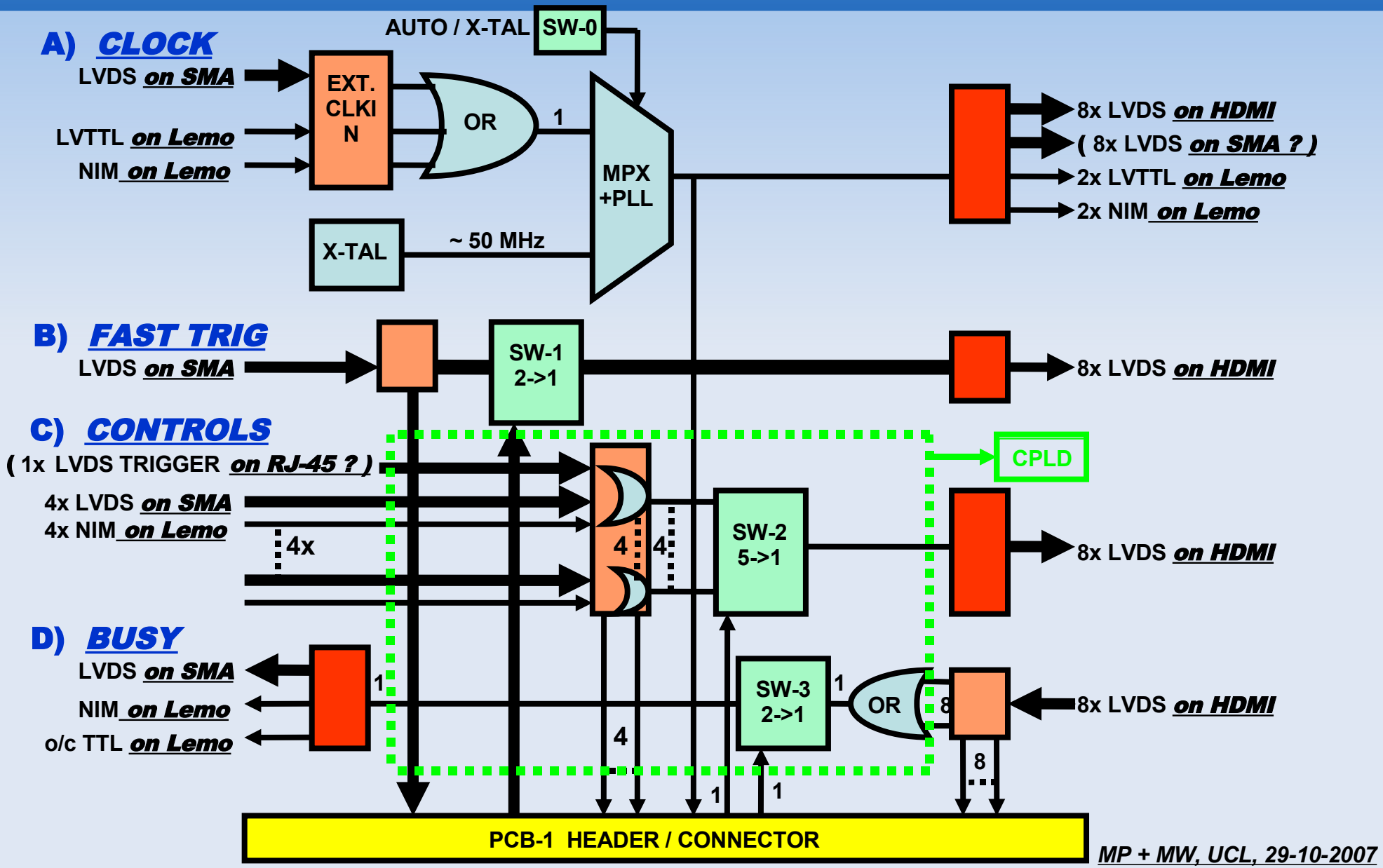
- = sync signal @ beg. of spill
- needs a special treat[t] in LDA & DCC and a **dedicated line to the DIFs** (reason: a *fast command* has (10 bits/100MHz = 100ns jitter)

BUSY

- Generated by the DCC/LDA and released as soon as the data from all DIF is in memory.
- Option if needed: a RAMfull could be also generate a BUSY (via a status word DIF→LDA), propagated to the C&C card and generating a trigger to stop all the DAQ.

Back-up

Clock & Control Card [reminder]



DAQ2 DHCAL M³ Test Beam contingencies

- ASIC's in auto trig
- DHCAL Data rates in TB
  - Expected from 100 GeV π (J-C. Brient's note)
    - 5 ASIC's touched in average (max 18) / plane
    - All on the central DIF
  - 1 evt = 160bits
    - Readout time 1 ASIC @ 5Mb/s = 0.032ms
    - RO 1 plane ~ 0.16ms [6 kHz]
  - 1 full HR (128 events) = 20480 bits
    - Readout time 1 full HR @ 5Mb/s = 4ms
- see Remi's talk for ECAL
- TB rates: 10^4 (10^8 at FNAL ???) part/s during 10s/min (SPS mode).
- RPC limitation: ~100Hz/cm²
  µMegas: basically not limited...