DAQ and CCC
Running modes of the detector
Signals and synchronization

http://ilcagenda.linearcollider.org/conferenceDisplay.py?confId= 2817

CALICE technical meeting on EVO

Tuesday, June 24

14:00 CEST

Duration : 1h

EUDET : 2 aims = 2 major modes ?

- Calibration / Noise / Test beam

The aim of the calibration mode is data taking in order to perform the calibration of the detector and physics studies about properties and performance of the detector. The detector and the electronic systems are configured to ensure the highest rate for the data tacking.

- Demonstrator (=EUDET)

The demonstrator mode is intended to run the detector as close as possible to ILC functioning in order to perform engineering studies on power pulsing, power supply, thermal dissipation. It is under the scope of the EUDET contract for which technical solutions must be tested and engineering feasibility must be proven.

Demonstrator mode

- Would need low power
  - Particular configuration for the electronics (degraded mode w.r.t. calibration mode)
- Would need beam structure like ILD
  - Can be emulated setting the trigger threshold high in ROCs (avoid noise)
  - Stop acquisition from time to time to reach a duty cycle of about 1%
- Not obvious…

Demonstrator mode

- EUDET questions to answer
  - Mechanical structure
    - Robustness
    - Compactness
      - Cabling
      - services
  - Overall power consumption
    - Current
    - Thermal dissipation
  - Signal integrity

Test beam submodes

- Single event

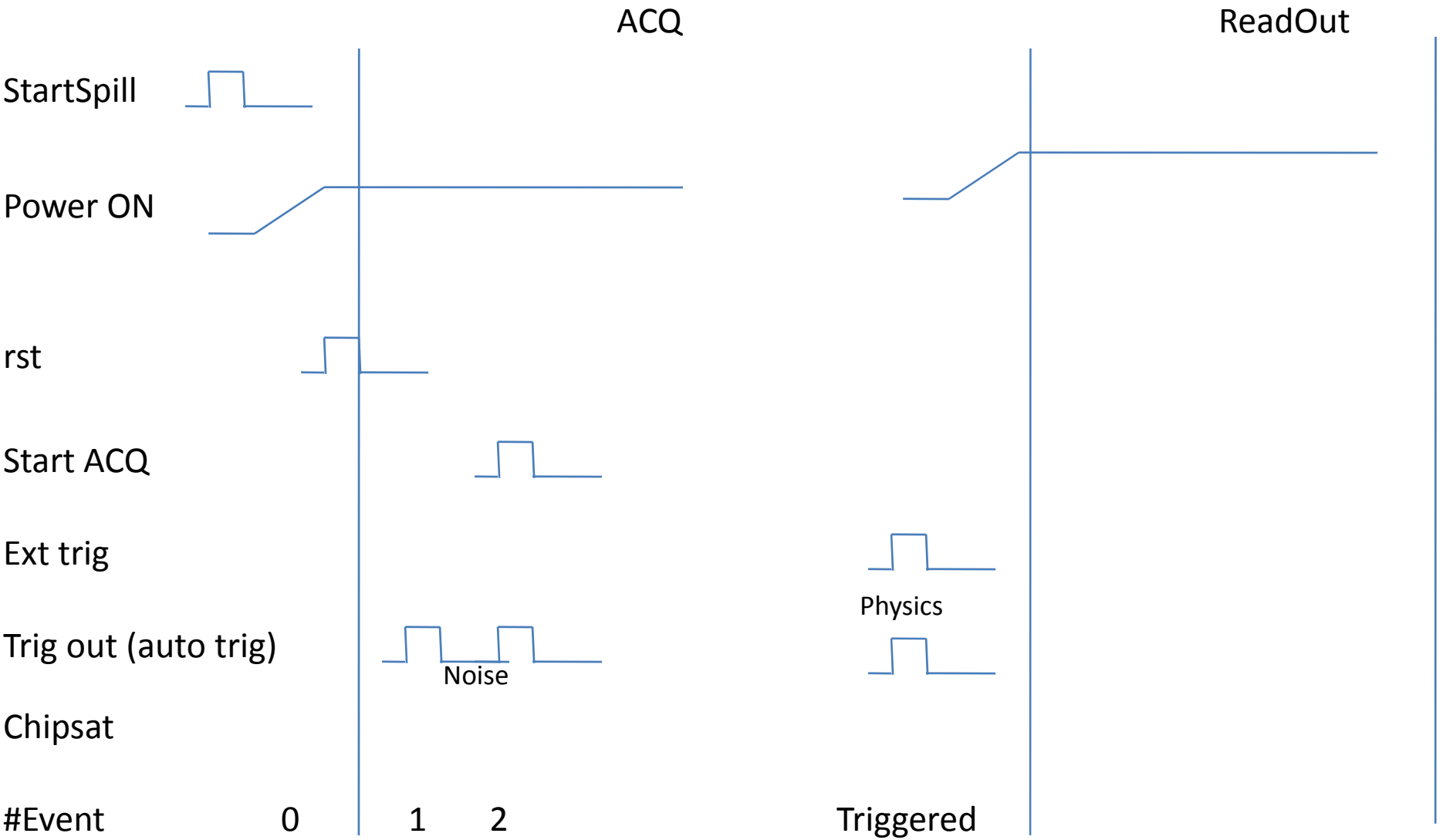
In this mode, a single interesting event is selected by a trigger. This trigger is external to the front end chips and must be distributed in a isochronous way all over the detector.
This event is the last stored event in the front-end chip buffers. These buffers may contain previously acquired events thanks to the auto-trigger capability of the front-end chips (noise or not triggered particles). These previous events are not synchronized in time from chip to chip. Chips are read_out immediately after the trigger and the acquisition process is quickly restarted

For calibration/noise : All the detector channels are forced to acquire the selected event.

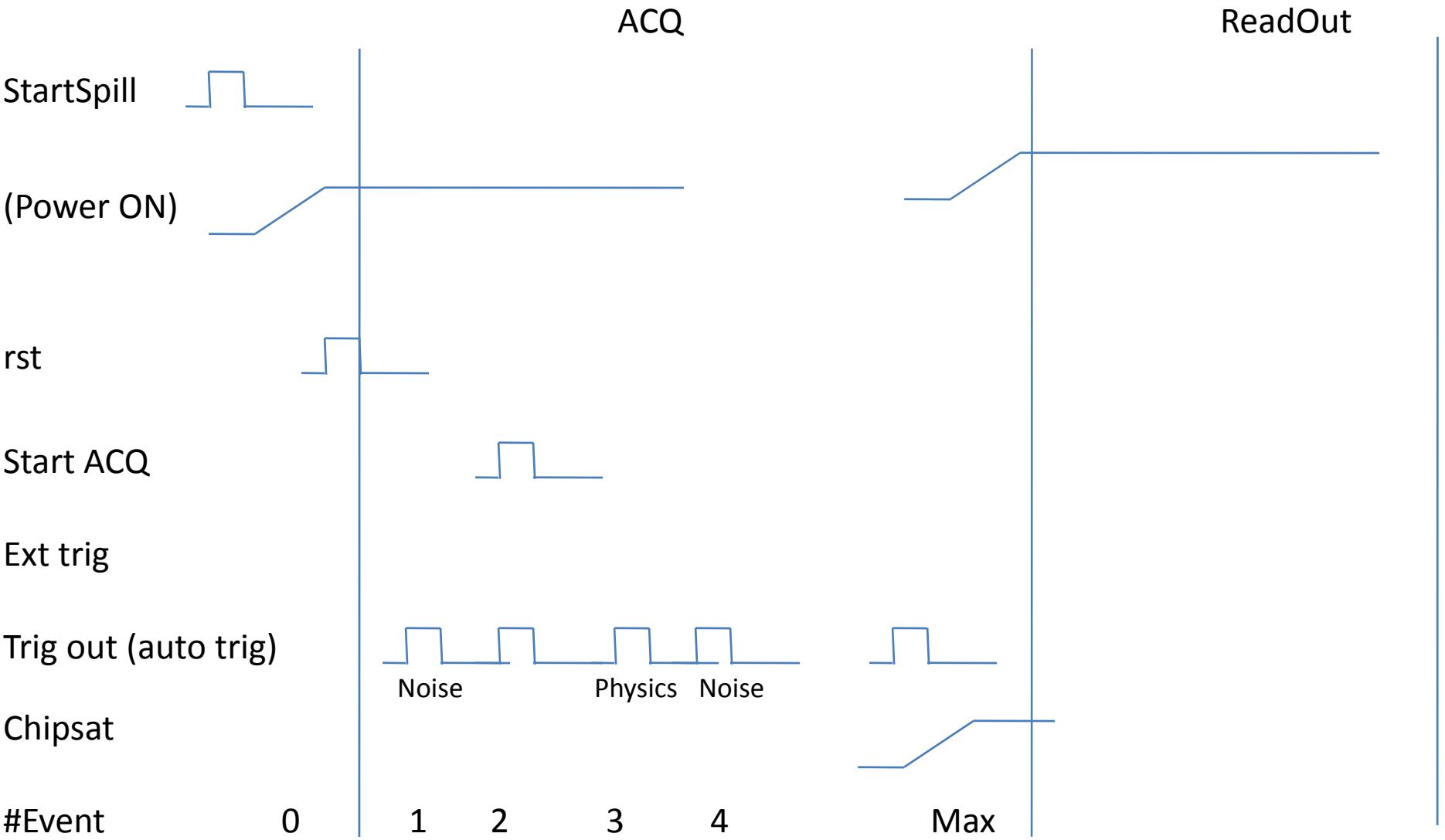
- Burst

Similar to the TB single event mode: the ASIC are put into their standard acquisition mode at the beginning of a spill, right after a synchronisation signal (Reset of BC counters on ASICs and DIF's).
There is no external trigger: the acquisition is stopped either: ChipFULL (local), RamFULL (Global), STOP by DAQ (e.g. at a given frequency)

Typical cycle (single event)



Typical cycle (burst)



Acquisition Signals (HardROC V2)
DIF-SLAB side

- Ck_5 (slow clock)
- Start_Acq
- Raz_ch
- Val_evt
- Trig_ext
- Rst_counter
- Chipsat
- (out_trig)
- (Hold)

Readout Signals (HardROC V2)
DIF-SLAB side

- Ck_5 (slow clock) (ck_40 for ADCs)
- Start_readout
- End_readout
- transmiton
- Dout