Running modes of the detector (update)
Demonstrator mode
DHCAL concentrator board
DIF&Signal integrity

http://ilcagenda.linearcollider.org/conferenceDisplay.py?confId= 2839

CALICE technical meeting on EVO

Friday, July 4

14:00 CEST

Duration : 1h

EUDET : 2 aims = 2 major modes ?

- Calibration / Noise / Test beam

The aim of the calibration mode is data taking in order to perform the calibration of the detector and physics studies about properties and performance of the detector. The detector and the electronic systems are configured to ensure the highest rate for the data tacking.

- Demonstrator (=EUDET)

The demonstrator mode is intended to run the detector as close as possible to ILC functioning in order to perform engineering studies on power pulsing, power supply, thermal dissipation. It is under the scope of the EUDET contract for which technical solutions must be tested and engineering feasibility must be proven.

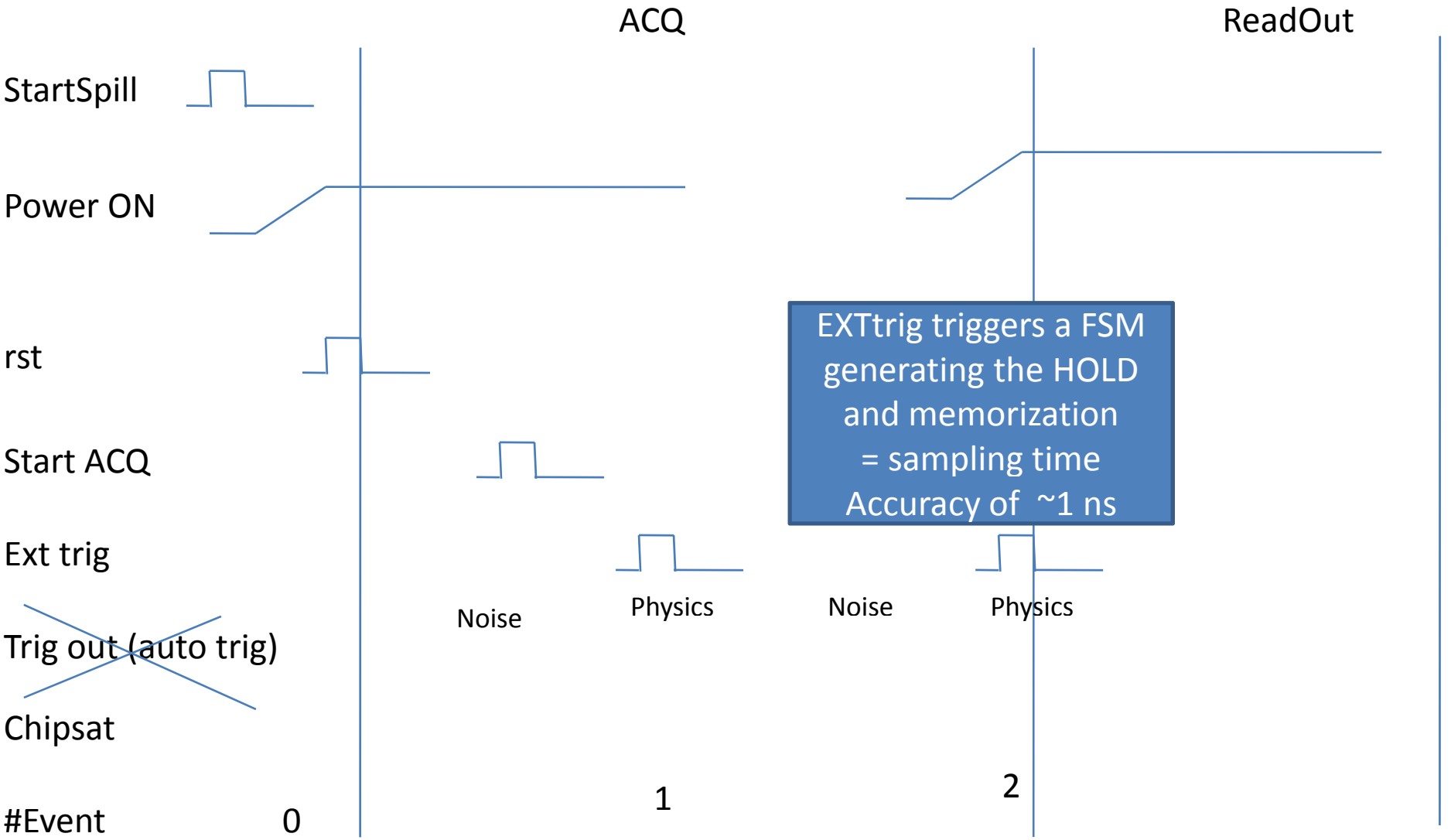
Test beam structure

- Structure inside the SPILL

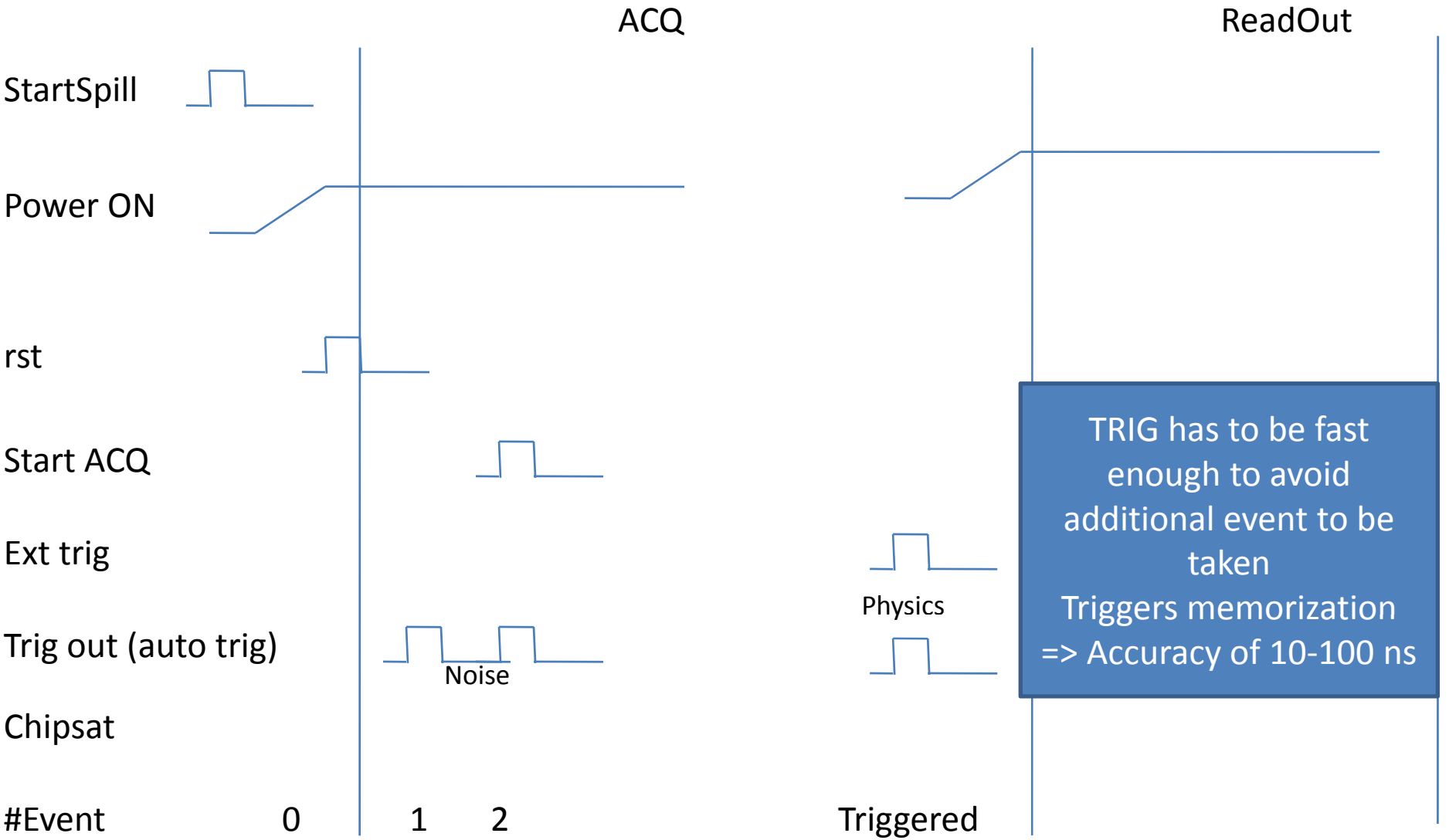
"The structure we see is that the beam particles are not spread completely randomly in time, but are bunched at the O(10-100us) level." (FNAL=11 us)

- Few particles within the micro-spill
- SINGLE evt mode = Study of Noise = acquire all the channel over the detector
- BURST mode = physics

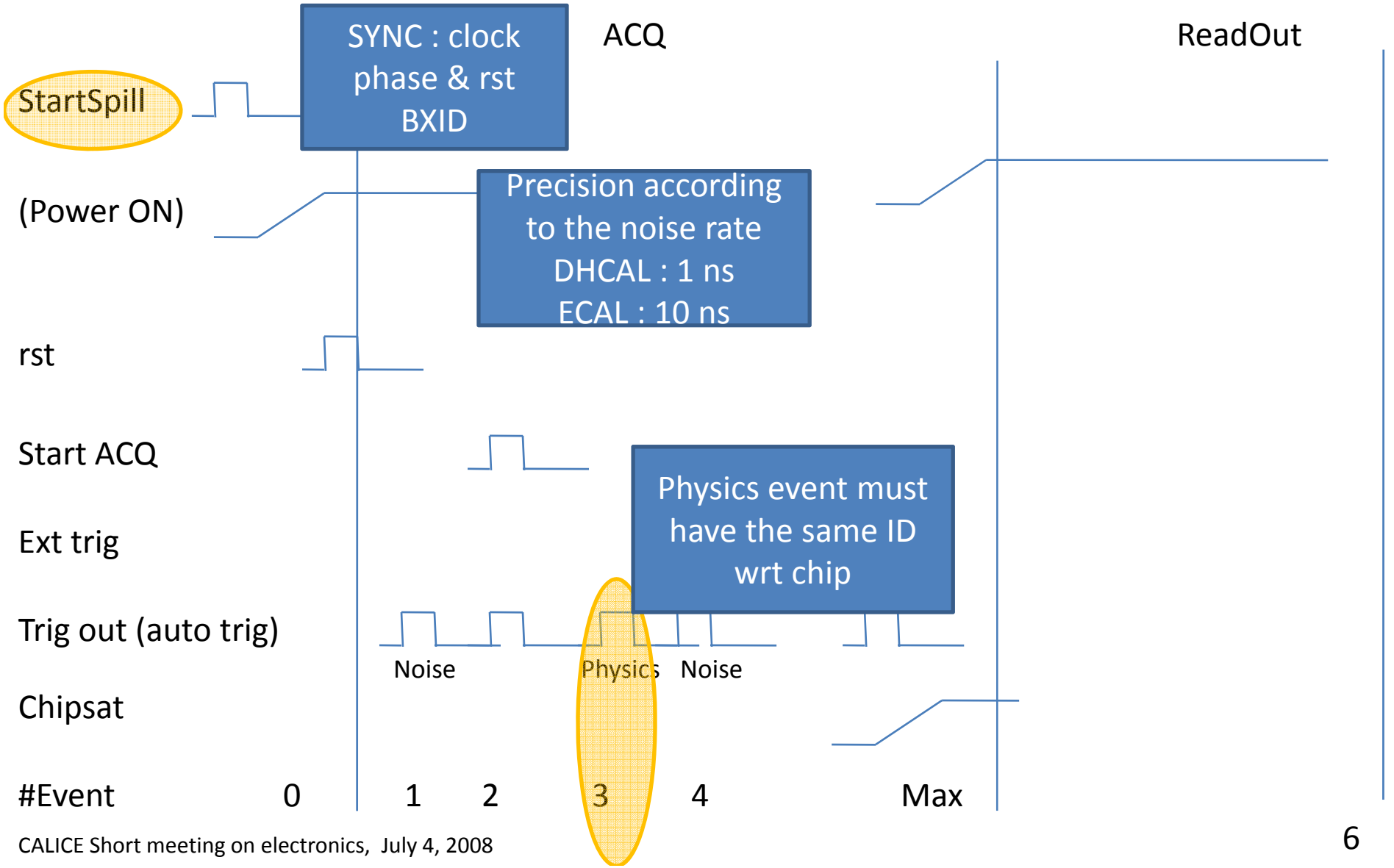
Typical cycle (triggered event)



Typical cycle (single event)



Typical cycle (burst)



Demonstrator mode

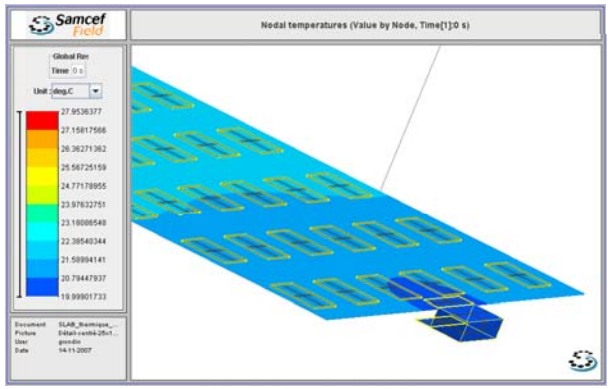
- Would need low power
  - Particular configuration for the electronics (degraded mode w.r.t. calibration mode)
- Would need beam structure like ILD
  - Can be emulated setting the trigger threshold high in ROCs (avoid noise)
  - Stop acquisition from time to time to reach a duty cycle of about 1%
- Not obvious…

Demonstrator mode

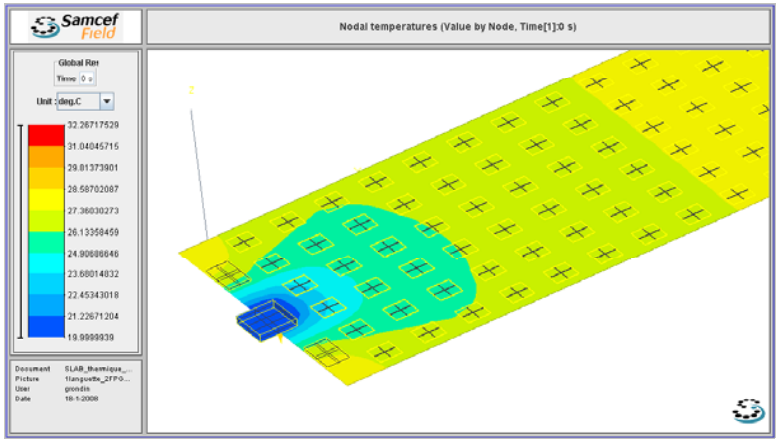
- EUDET questions to answer
  - Mechanical structure
    - Robustness
    - Compactness
      - Cabling
      - Services
  - power
    - Current (power) consumption
    - Thermal dissipation
  - Signal integrity

Demonstrator mode : Thermal studies

- DIF components have a strong impact on the cooling of the SLAB



Without fpga

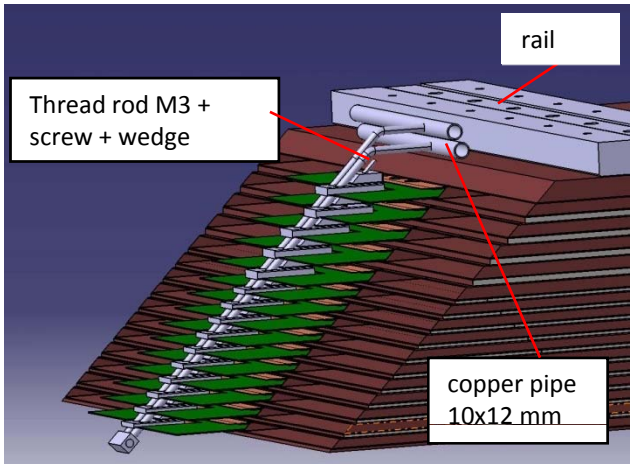


With fpga

- Depends on : power dissipation, location on the DIF board
- To be realistic : power down unnecessary features (those not needed if it were ILC), low power firmware

Cooling (ECAL)

- EUDET ECAL will be build as if it were an ILD module
- Place to connect DIF to the cooling pipe
- Location of FPGA
  - Move the DIF outside the detector ?
  - Warming resistor to “emulate” the fpga on adapter board ?
- Thermal probes



Demonstrator mode : Power

- Power pulsing to be tested at ~ILC duty cycle
- Low current output capability of power supplies
  - Need HUGE (few mF !) capacitance to store power at the DIF level
  - Capability to monitor power supplies
- HV switch on/off
  - HV stability
  - Detector capacitance can discharge in the electronics

Demonstrator mode : conclusion

- Run the detector similarly to ILD
  - With or without beam
  - Not intended to acquire physics data but should have a minimum activity to show that the detector is still working
- Disable features to avoid power cons. And thermal dissipation
  - Minimize clock frequency, realistic data rate
  - No pll, SER/DES, and heating parts
- Enable V(t), HV(t), T(t), power switching

Next topics

- Franck : DHCAL concentrator board
  - links
  - Synchronisation
- Maurice & Bart : ECAL Slab & Signal integrity
- Next meeting ?
  - EVO or @LLR or @CERN : http://www.doodle.ch/qxb3q7xvvhf3zxhh
  - Agenda ?