DCC (Data Concentrator Card)

Goal: decrease the number of LDA

This card is between the DIF and LDA

Remember : 3 DIF x 40 planes

Without DCC: needs of 12 LDA

With DCC (9 DIF per DCC) : needs of 2 LDA

Our schedule:

First : works with an XILINX evaluation board to show a feasibilities

Goal : Design a card to read 9 DIF

Open questions

- ID for each DIF
  - To send commands
  - To read the data on each DIF
- Protocol
  - IDLE to synchronize the link
  - SOF,EOF for Data delimiter
  - CMD characters to send commands
  - Others

Questions

- Protocol

DIF to LDA ????

To Be Define : Organisation of DATA and DATA COMMANDS

LDA to DIF ????

- Link specification
  - Rate for the serial link is 100 Mb/s (8b/10b) (parallel data on 16 bits)
  - Needs of 100 MHz clock on each cards.
  - Others signals on HDMI connector :
    - On same pin : Ext_trig and Sync ?
    - Busy signal : to be define (example RAM Full, DCC busy)