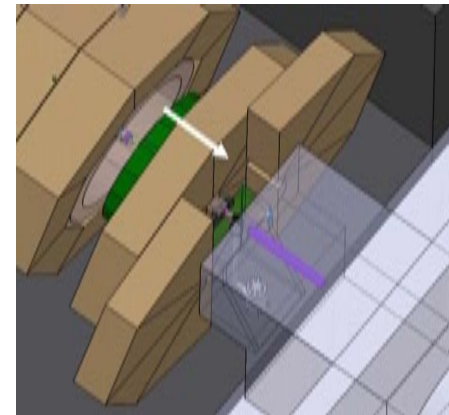


SLAB COOLING

- *DEMONSTRATOR*
- *EUDET*



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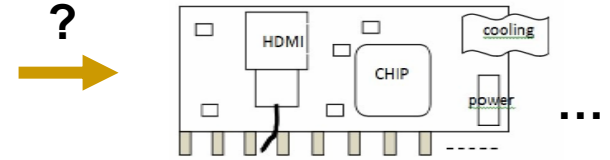
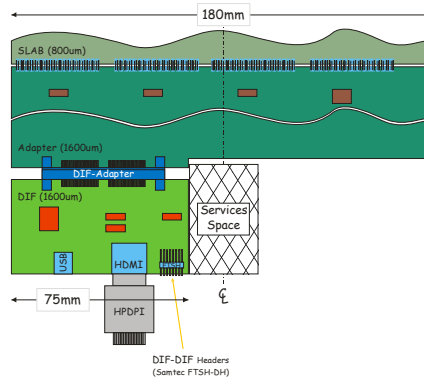


- Goal of experimental tests:
 - a real thermal test to be compared to numerical simulation,
 - In order to answer to simplification of slab's model,
 - To know more precisely transfert coefficients,
 - To verify the behaviour of the cooling system in EUDET's configuration.

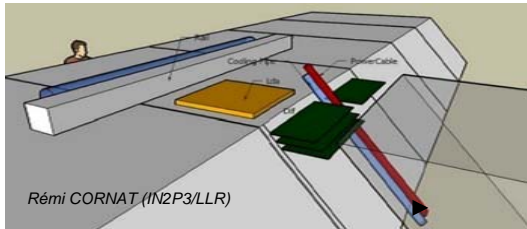
So, dimensions of structures of the demonstrator (124mm) have to be defined, with all parameters for these first thermal tests (dimensions, nb of resistances, captors....)

- To reproduce as precisely as possible these tests in simulations.

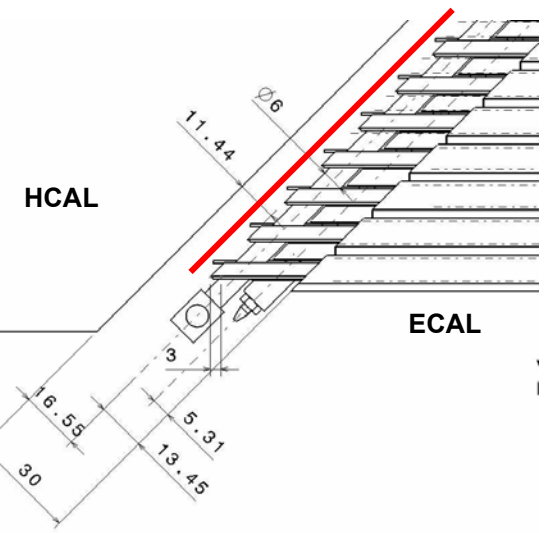
Mechanical constraints on ECAL electronics:



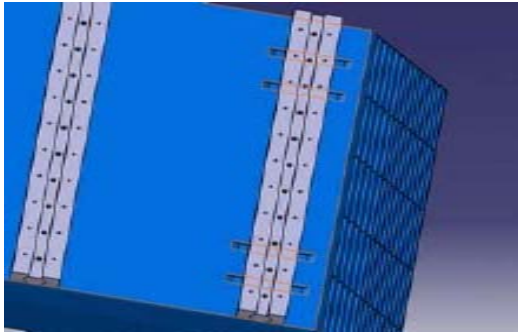
DIF is part of last ASU of the SLAB
Minimum Space for cooling necessary



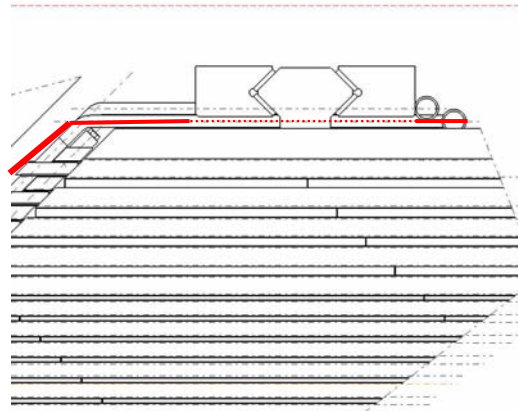
Place for cabling : DAQ + HV + GND
Service space between cooling and HCAL > 1cm



Space for HV and GND



Former solution: in thick composite plate



Passing through the rail: OK

SLAB COOLING - DEMONSTRATOR

Boundary condition:

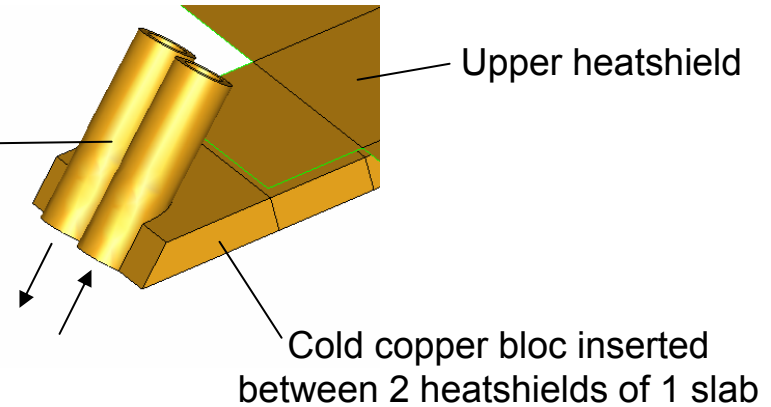
Convective flux into pipe with fluid at 20°C ($h = 3445 \text{ W/m}^2\cdot\text{K}$)

Load (for 1 half slab = 1 side)

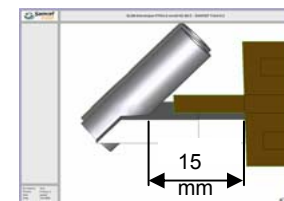
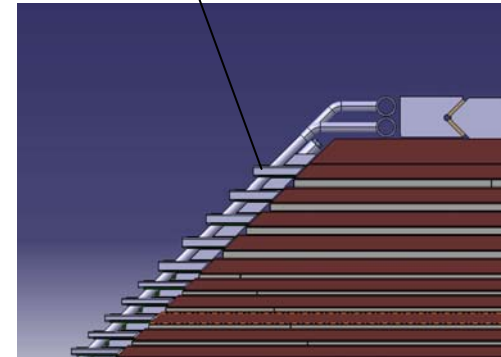
Total wafer power (EUDET) : **0.205 W**

With 11 ASU 124.5 x 124.5

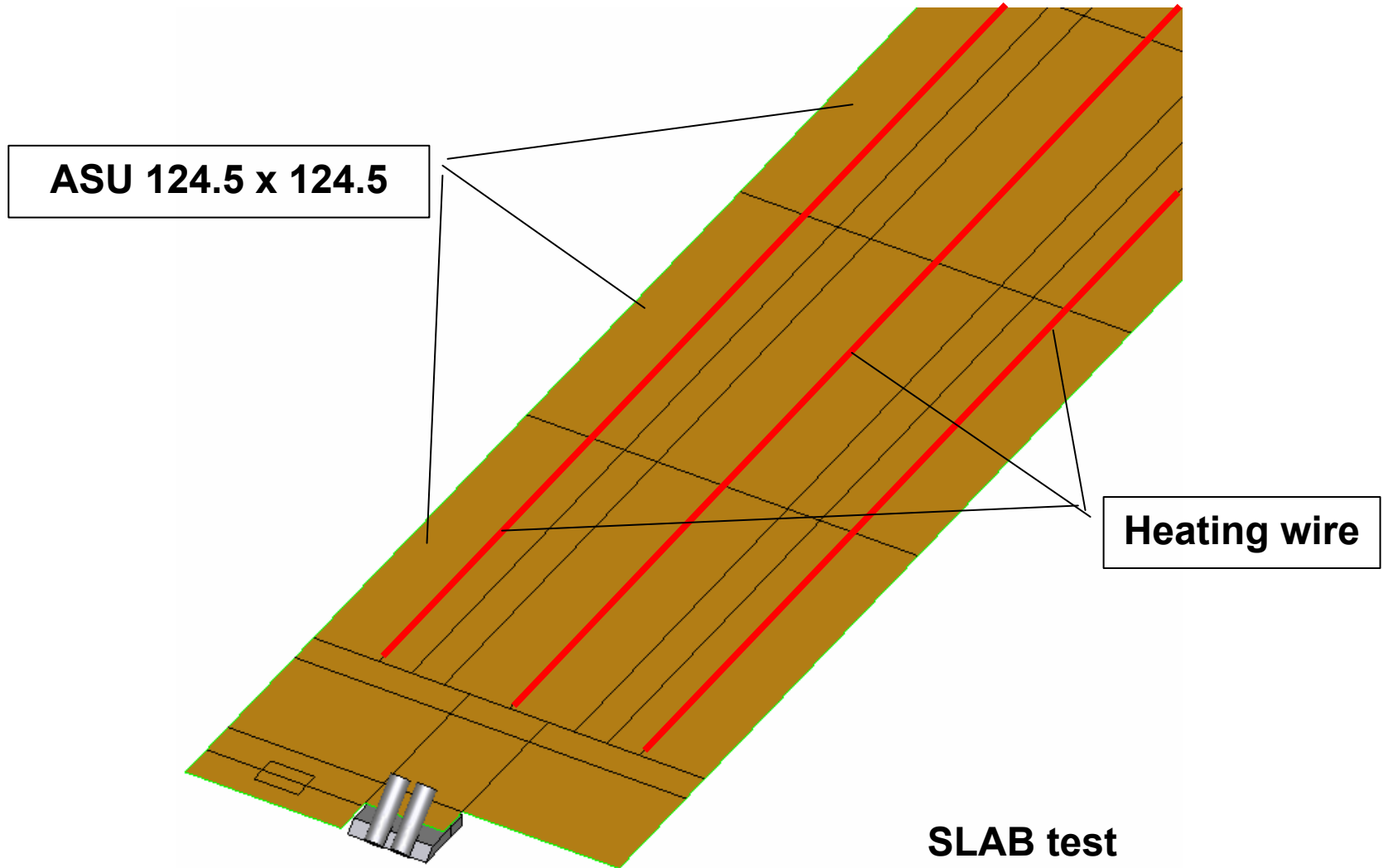
=> $0.205 / 11 = 0.018636 \text{ W / ASU}$



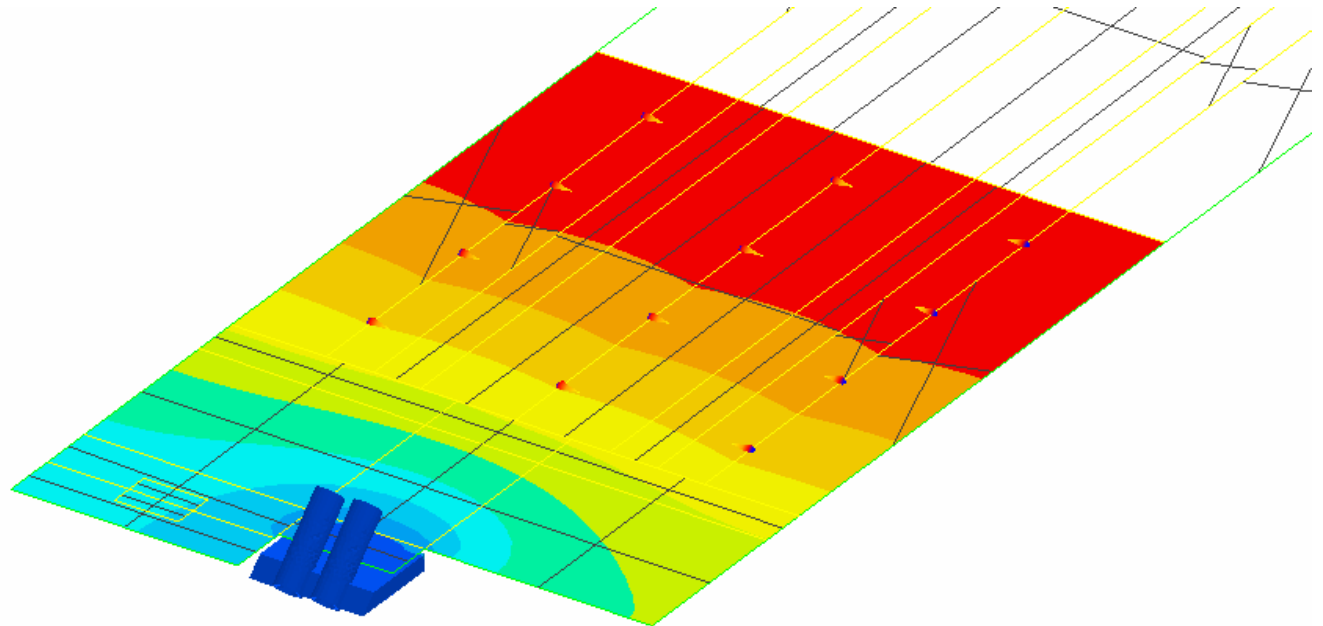
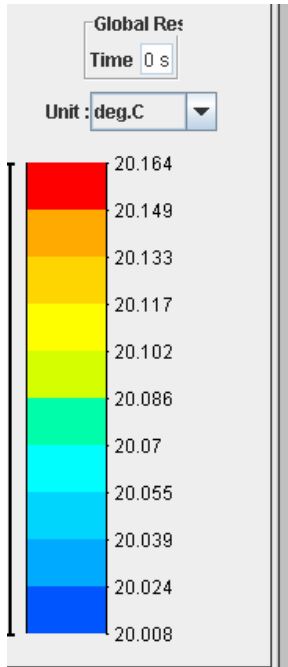
ASU 124,5 x 124,5	Power (w)	Lenght (mm)	If 3 Heat wire : Power / Heat wire (w)
1	0,0186	124,5	0,0062
2	0,0373	249	0,0124
3	0,0559	373,5	0,0186
4	0,0745	498	0,0248
5	0,0932	622,5	0,0311
6	0,1118	747	0,0373
7	0,1305	871,5	0,0435
8	0,1491	996	0,0497
9	0,1677	1120,5	0,0559
10	0,1864	1245	0,0621
11	0,2050	1369,5	0,0683



Model presentation:

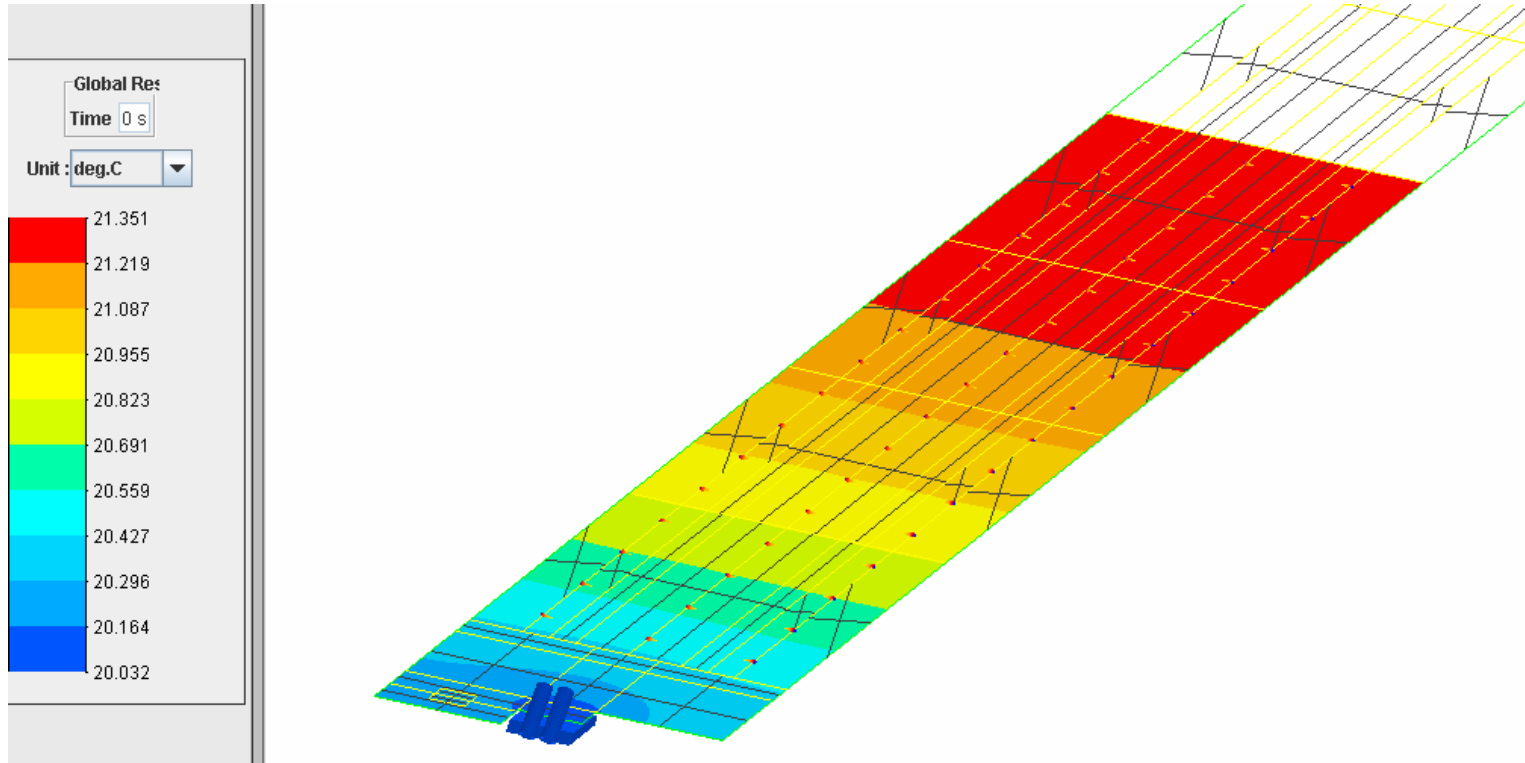


Load case A : 1 ASU (power 0.0186 W)



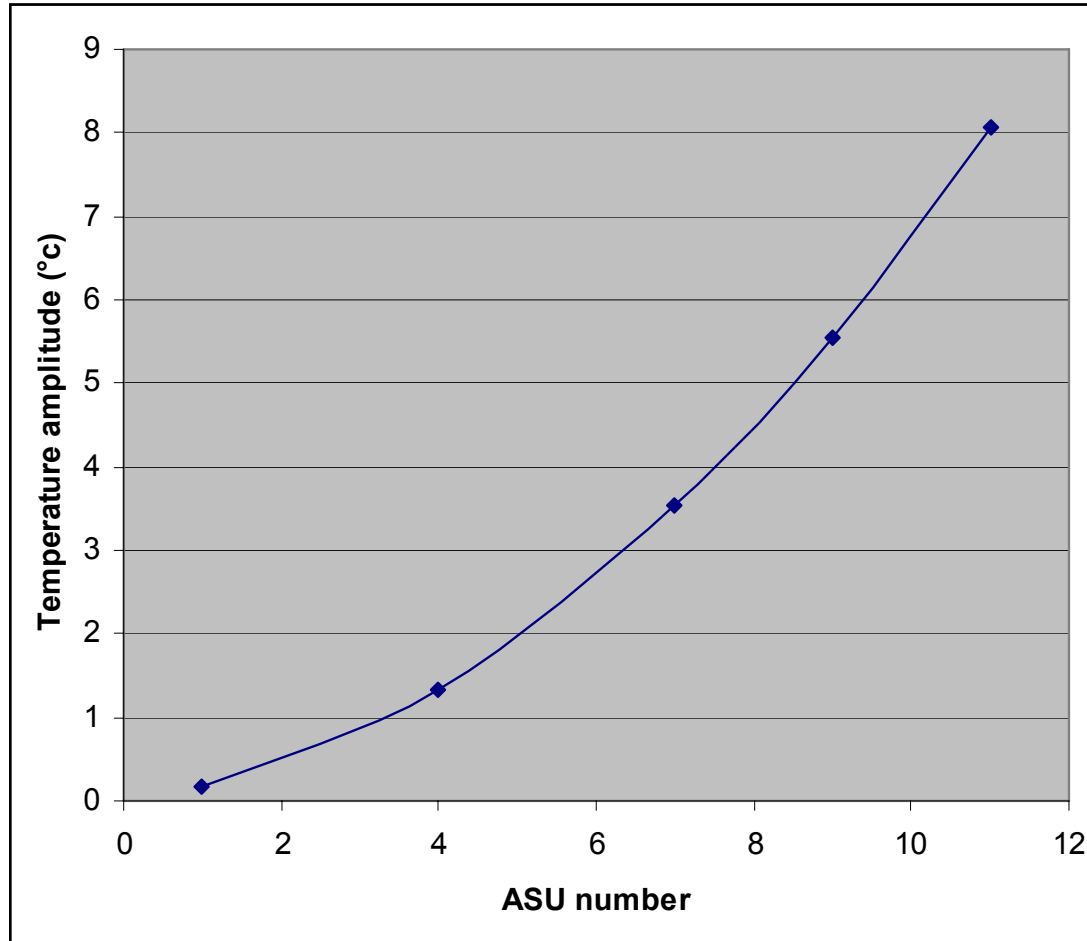
Temperature amplitude : 0.156°C => Small temperature variation => hard to measure

Load case B : 4 ASU (power 0.0745 W)



Temperature amplitude : 1.32°c...not enough

Temperature amplitude / ASU number

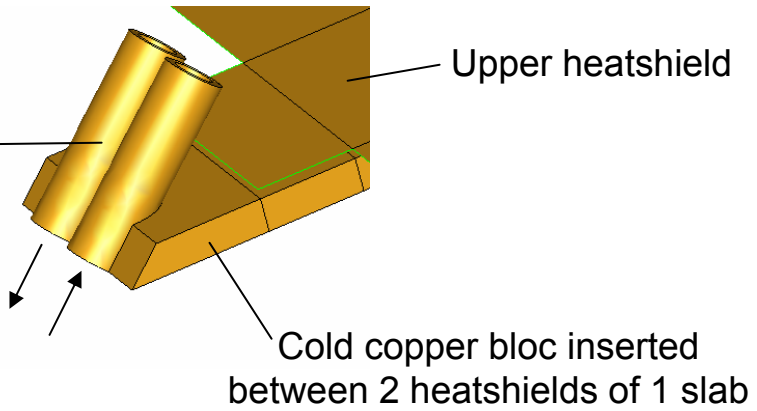


At least, ~5 or 6 ASU necessary to have convenient results

SLAB COOLING - EUDET

Boundary condition:

Convective flux into pipe with fluid at 20°C ($h = 3445 \text{ W/m}^2\cdot\text{K}$)

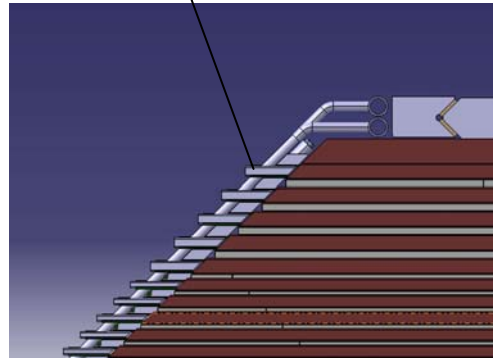


Load (for 1 half slab = 1 side)

- Channel heat flux : 25 μW
- Number of channel / chip : 64 (Hardroc)
- Number of chip / wafer : 4
- Number of wafer on 1/2 SLAB : 32

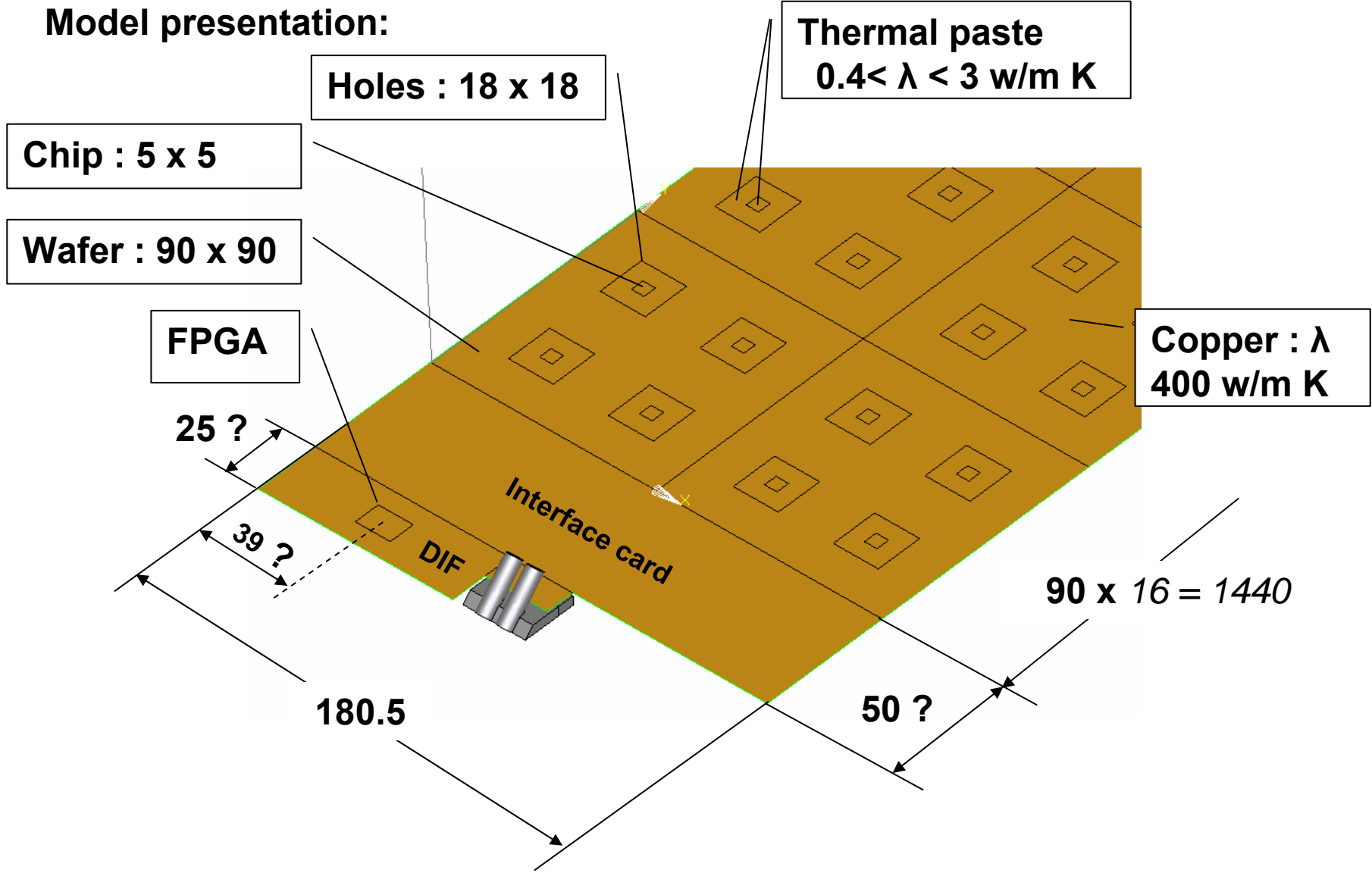
Total wafer power : $25 \times 10^{-6} \times 64 \times 4 \times 32 = \mathbf{0.205 \text{ W}}$

FPGA power : **3 W**



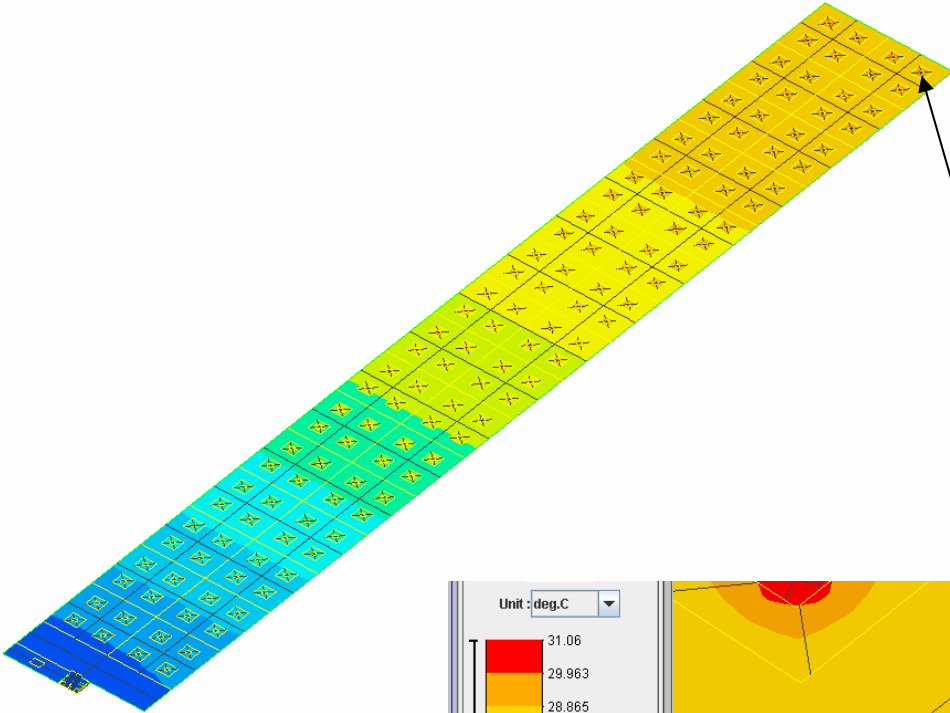
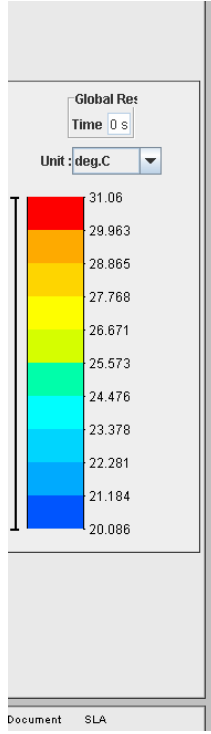
SLAB COOLING - EUDET

Model presentation:

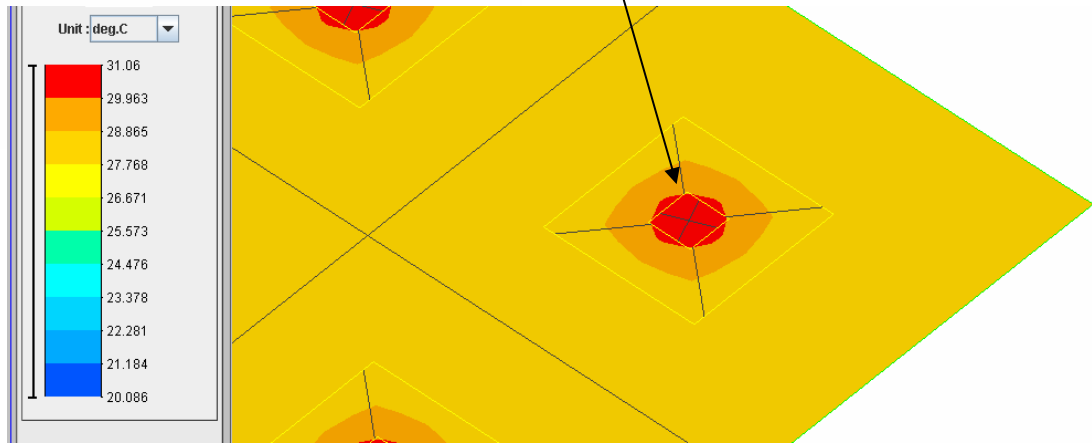


SLAB COOLING - EUDET

Load case 1 : Without FPGA, Thermic paste $\lambda = 0.4 \text{ W/m } ^\circ\text{K}$, Copper thickness : 0.4 mm

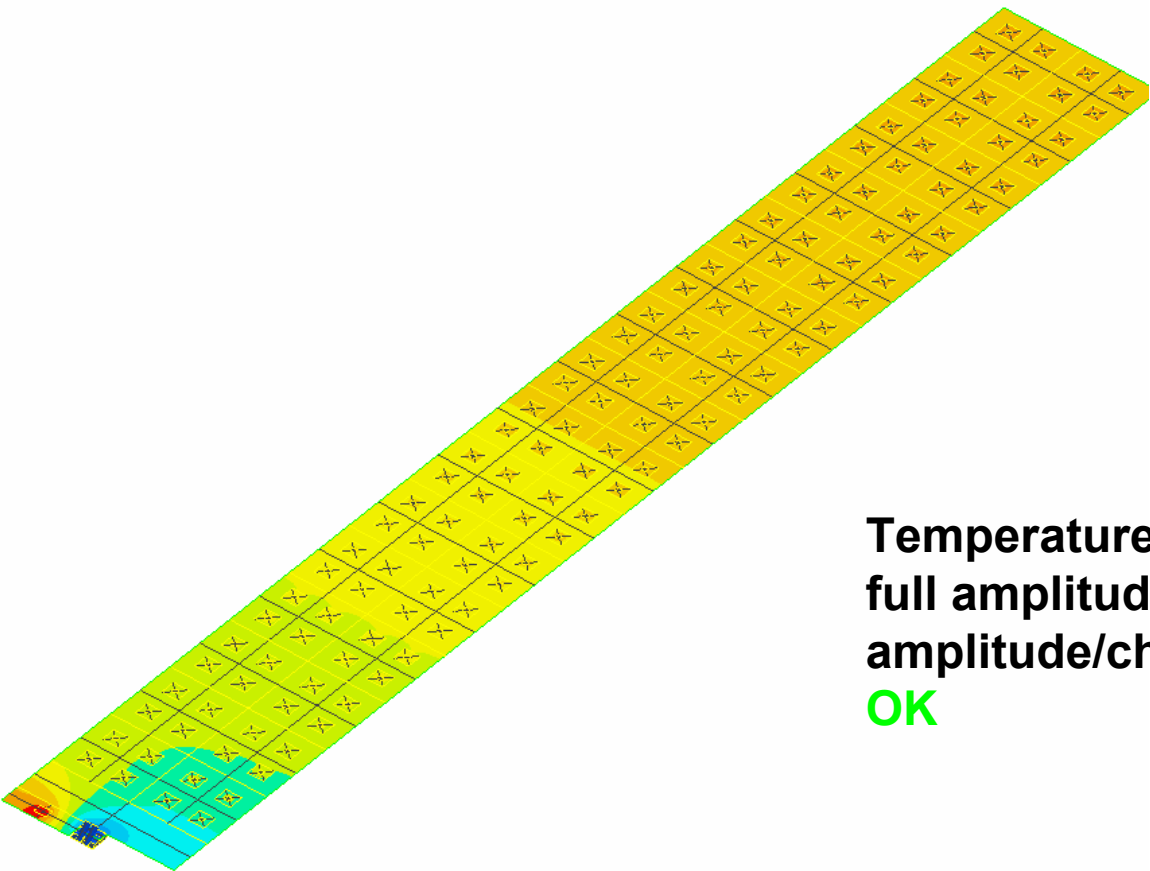
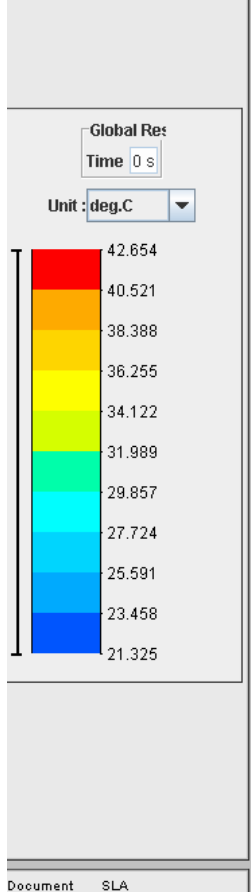


Temperature amplitude : 11 °c
OK



SLAB COOLING - EUDET

Load case 2 : With FPGA, Thermic paste $\lambda = 0.4 \text{ W/m } ^\circ\text{K}$, Copper thickness : 0.4 mm

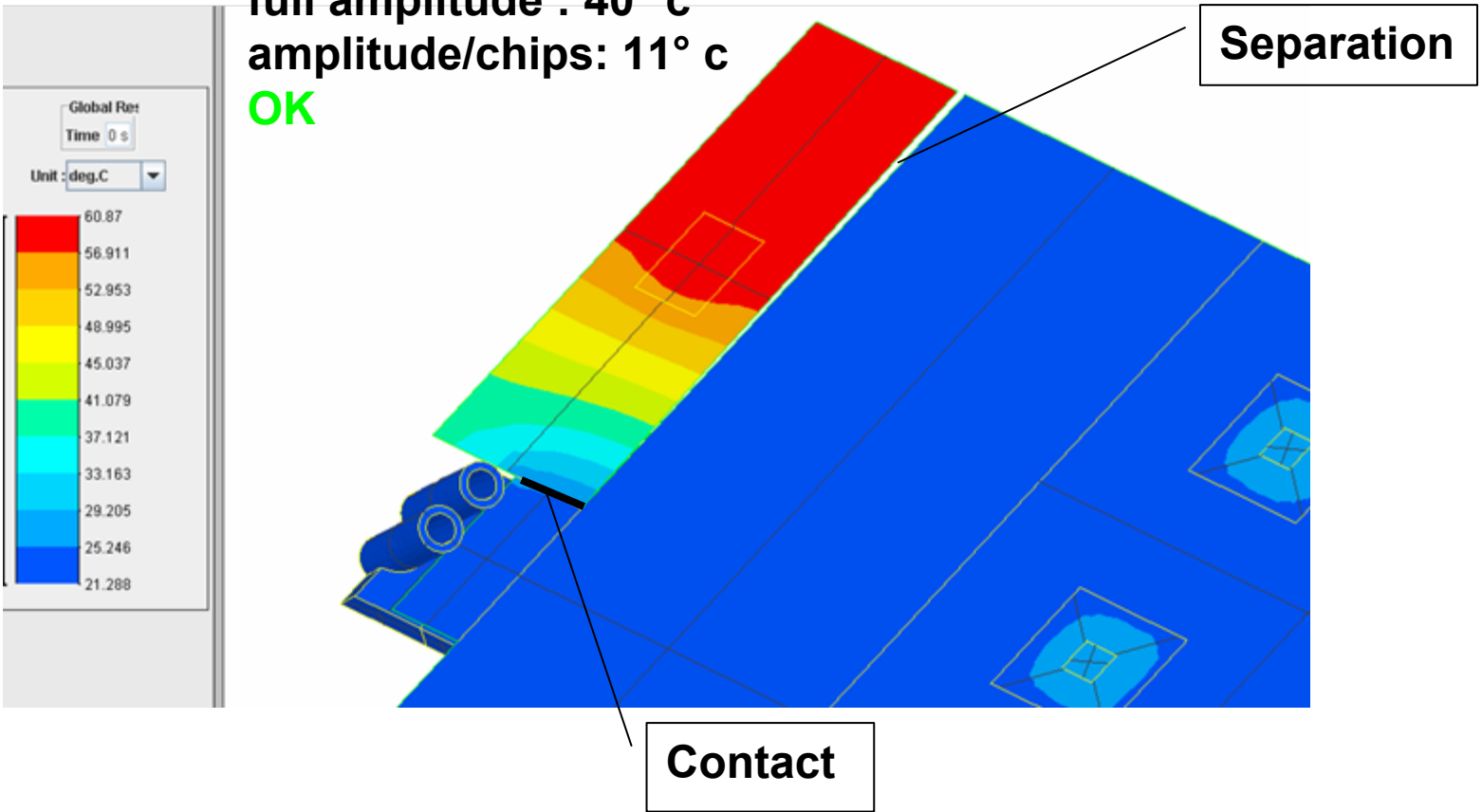


Temperature :
full amplitude : 21.3 °c
amplitude/chips: 11° c
OK

SLAB COOLING - EUDET

Load case 3 : With FPGA separate from the copper plate, Thermic paste $\lambda = 0.4 \text{ W/m } ^\circ\text{K}$, Copper thickness : 0.4 mm

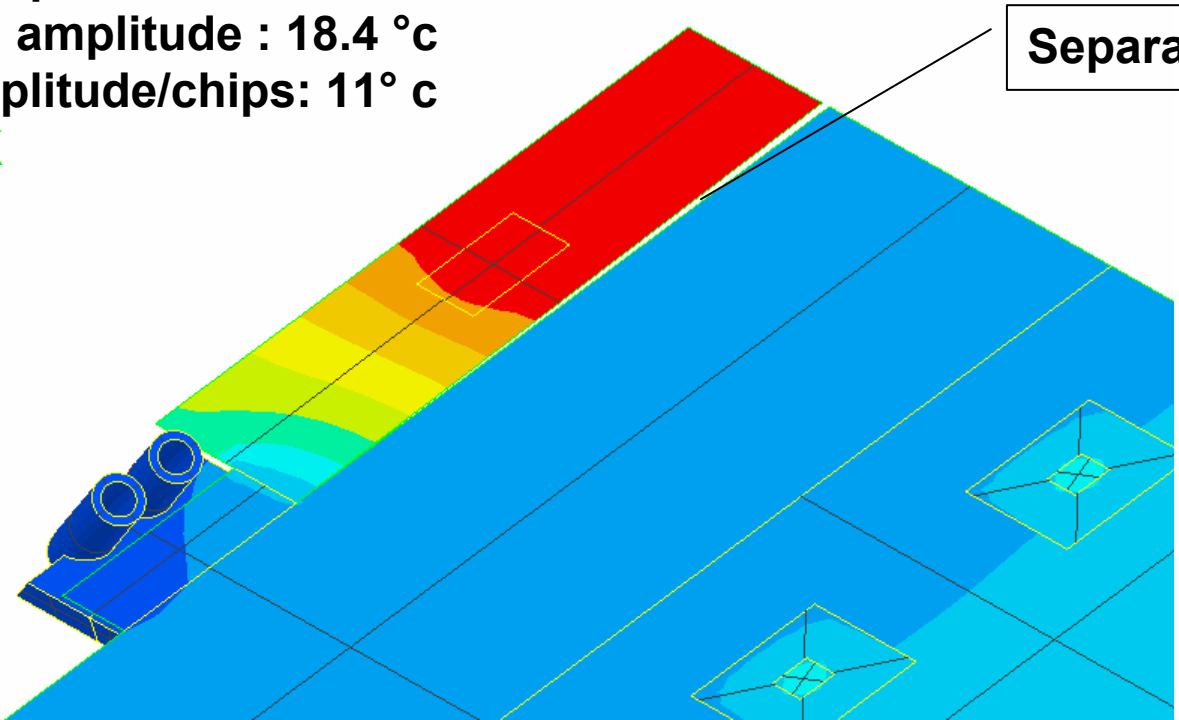
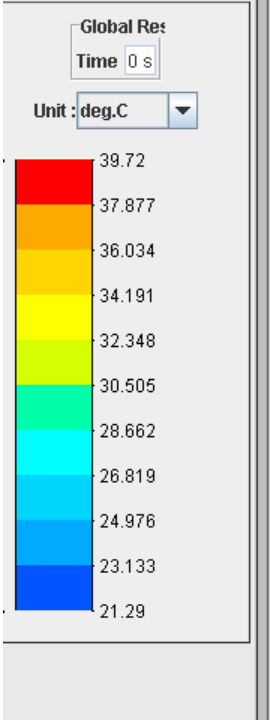
Temperature :
full amplitude : 40 °c
amplitude/chips: 11° c
OK



SLAB COOLING - EUDET

Load case 4 : With FPGA separate from the copper plate, Thermic paste $\lambda = 0.4 \text{ W/m } ^\circ\text{K}$, Copper thickness : 0.4 mm and **1 mm** near FPGA

Temperature :
full amplitude : 18.4 °c
amplitude/chips: 11° c
OK



Demonstrator

- *3 layers – 124.5mm - 1300 long ?*
- *Thermal simulation with 1 ASU ? (4 better): PCB dimensions (total length) to be confirmed*
- *Number of heating resistances: 3 rows corresponding to chips rows : power/surface*
- *Heat shield Geometry / Thermal insulation of slab for tests*
- *Optimization of composite sheets : studies of best parameters for thick plates*

Goal:

- **Test of cooling system: mechanical aspect and performances**
- **Optimization of simulation: conductivities, materials, geometries**

EUDET

MANCHESTER
1824

Backend system (DIF support): **Confirmation of FPGA consumption and position...**

LM

EUDET module: structures to be assembled and tested with cooling system.

CC

Detector slabs **integration for thermal tests** with tuned power, copper shields with specific geometry and temperature probes.

- Interface card ? Dimensions and specificities ?
- DIF: integrated or not

Goal:

- **Simulations to be performed with demonstrator's approved values to validate the whole cooling of EUDET.**