IN2P3

Omega

EUDET FEE status

C. de LA TAILLE

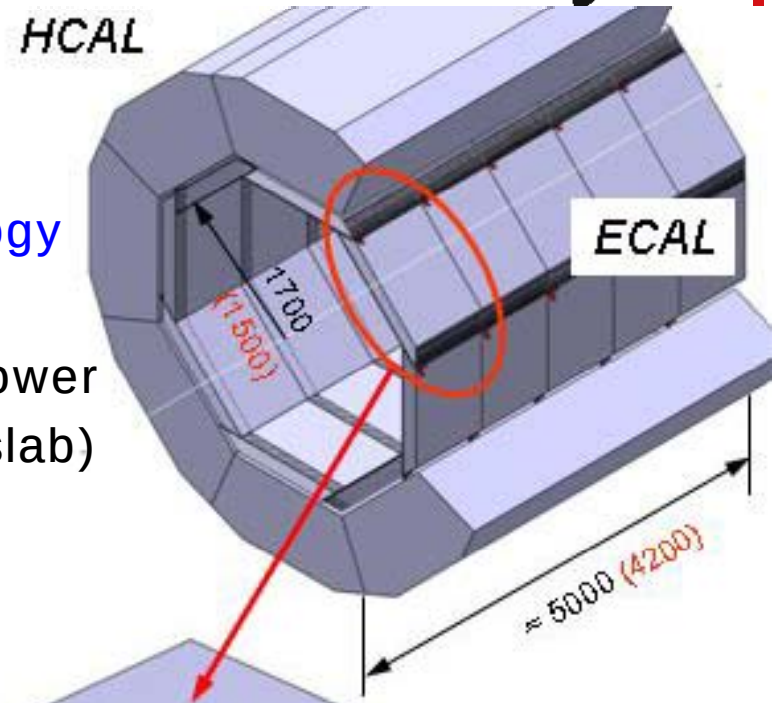
CALICE Calorimeter for ILC

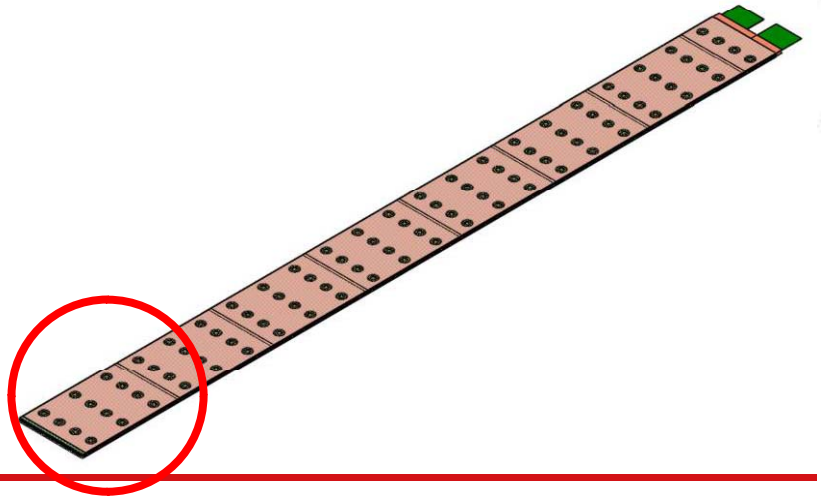
EUDET

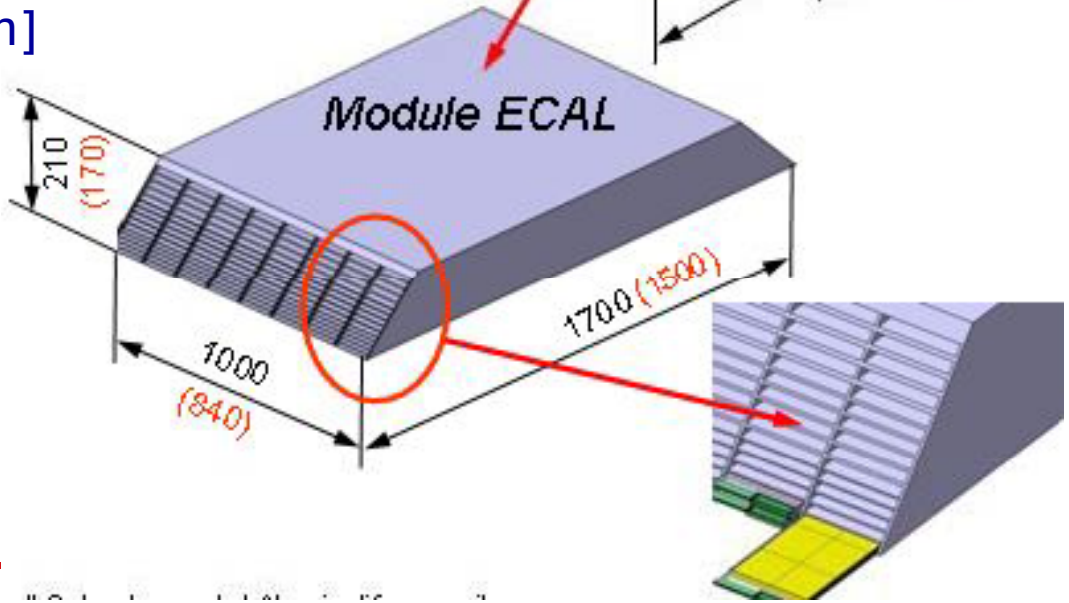
Orsay MicroElectronic Group Associated

Technological prototypes : “EUDET module”

- Front-end ASICs embedded in detector
  - Very high level of integration
  - Ultra-low power with pulsed mode
  - Target « analog friendly » SiGe technology
- All communications via edge
  - 4,000 ch/slab, minimal room, access, power
  - small data volume (~ few 100 kbyte/s/slab)
- EUDET funding for fab in 2009
- [AHCAL : see talk by F. Sefkow]
- [DHCAL : see talk by I. Laktineh]

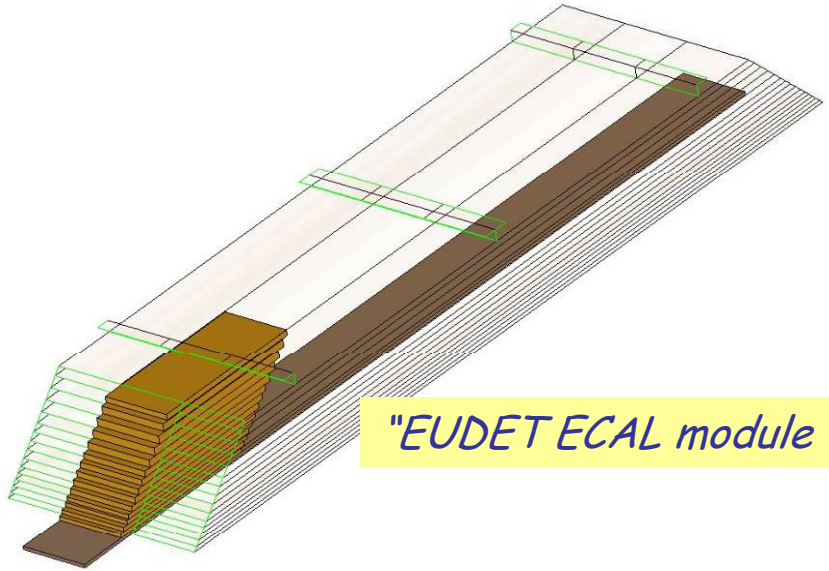




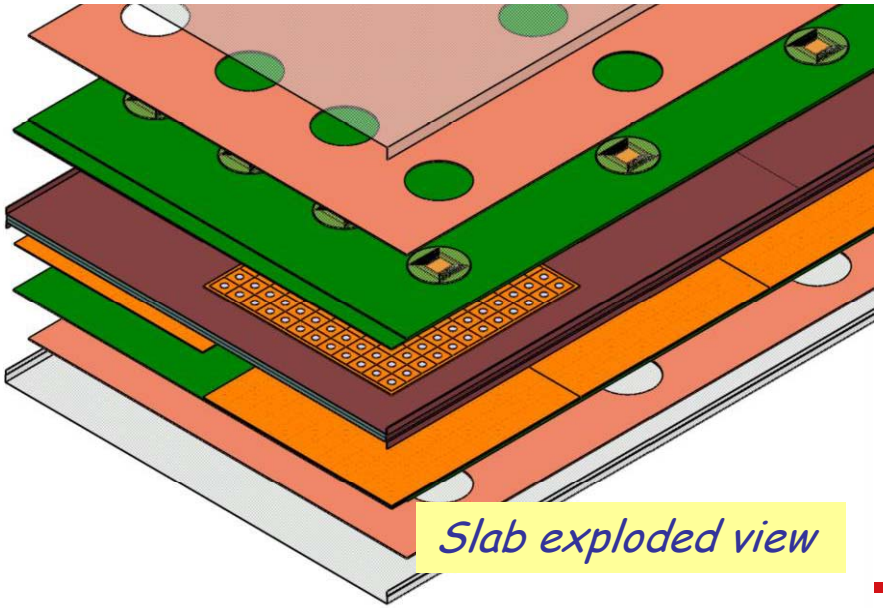


EUDET module FEE : main issues

- "stictchable" motherboards
  - Minimize connections between boards
- No (few) external components
  - Reduce PCB thickness to <800µm
  - Mixed signal issues
  - Digital activity with sensistive analog front-end
- Pulsed power issues
  - Electronics stability
  - Thermal effects
  - To be tested in beam a.s.a.p
- Interface to new DAQ
  - DIF boards, detector
- <u>Low cost and industrialization are the major goal</u>



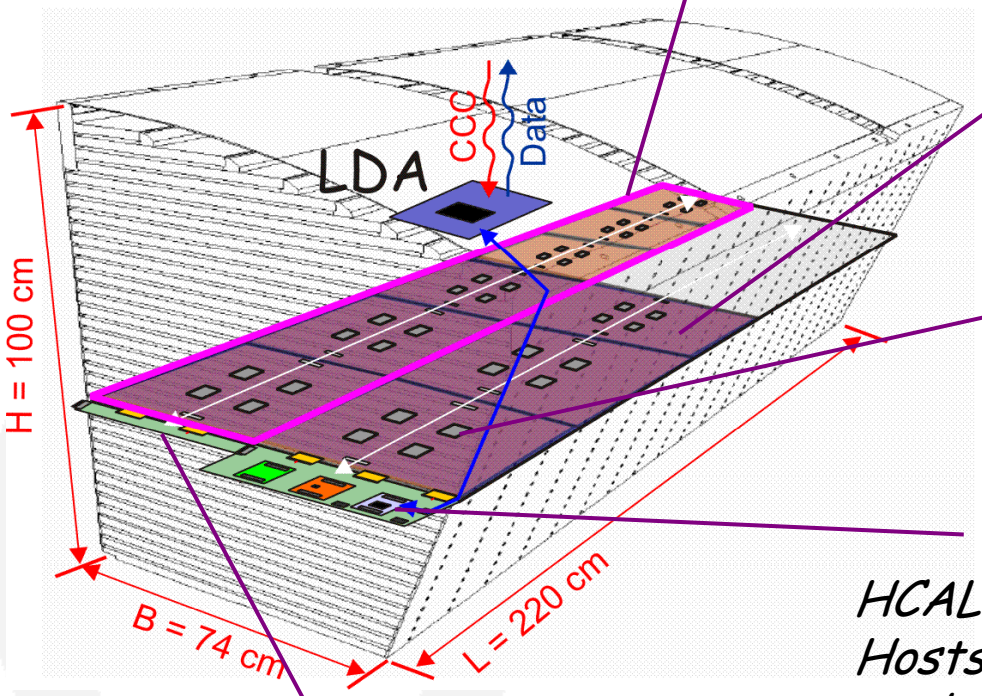
"EUDET ECAL module



Slab exploded view

Barrel HCAL architecture

1/16 of barrel half



AHCAL Slab
6 HBUs in a row

Front end ASICs embedded
Interfaces accessible

HBU
HCAL Base Unit
12 x 12 tiles

SPIROC
4 on a HBU

HEB
HCAL Endcap Board
Hosts mezzanine modules:
DIF, **CALIB** and **POWER**

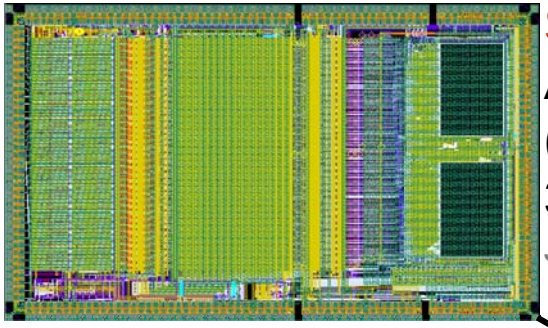
HLD
HCAL Layer Distributor

Power:
40 µW / channel

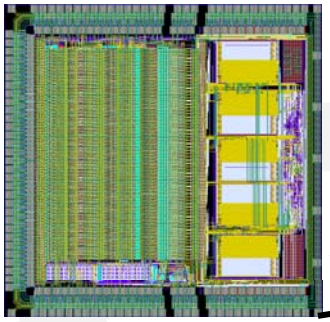
Heat:
T grad. 0.3K/2m
Time constant: 6 d

P.Goettlicher (DESY)

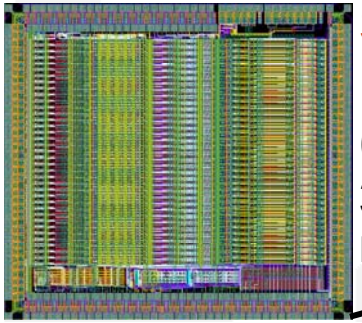
The front-end ASICs : the ROC chips



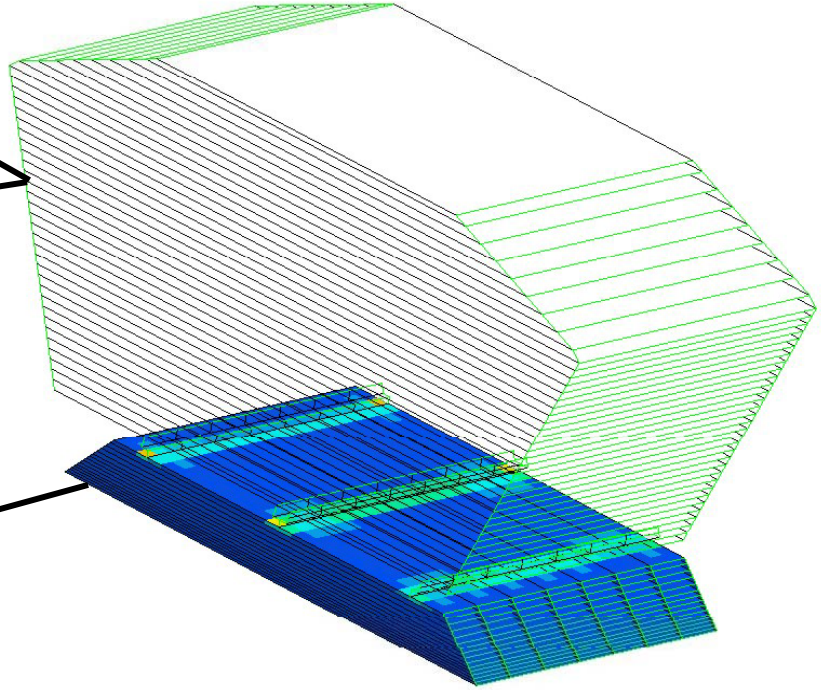
SPIROC
Analog HCAL
(SiPM)
36 ch. 32mm²
June 07



HARDROC
Digital HCAL
(RPC, µmegas or GEMs)
64 ch. 16mm²
Sept 06

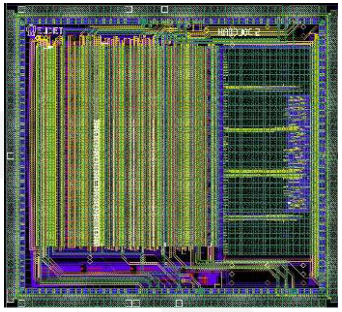


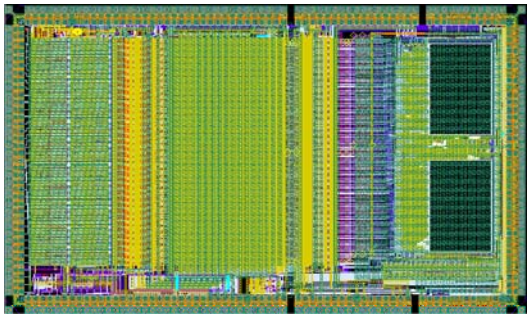
SKIROC
ECAL
(Si PIN diode)
36 ch. 20mm²
Nov 06



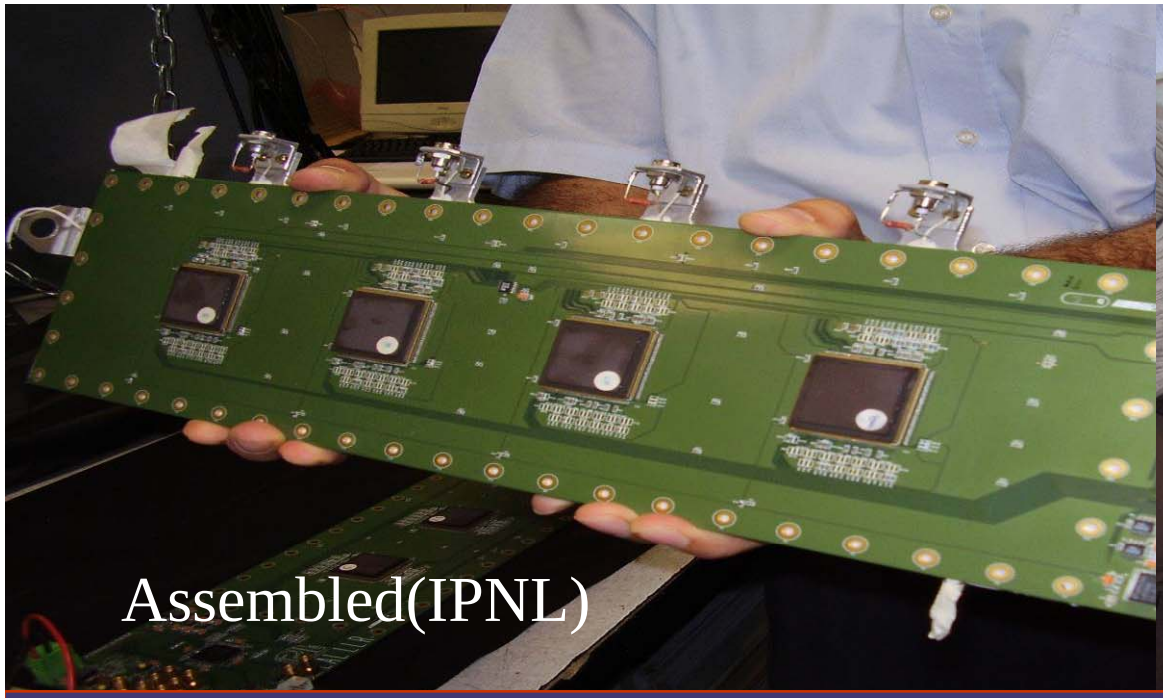
Activities in 2008 (1)

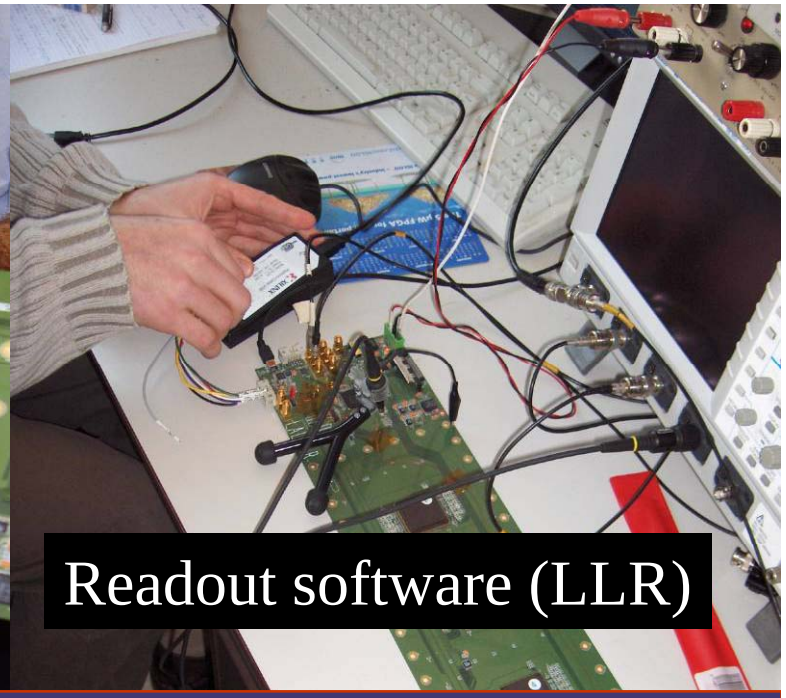
- 2 chips submissions
  - HaRDROC2 (june 08) final prototype before production
  - SPIROC2 (june 08) : fixed ADC and slow control bug
  - Financed by CALICE
  - EUDET money reserved for engineering run in 2009

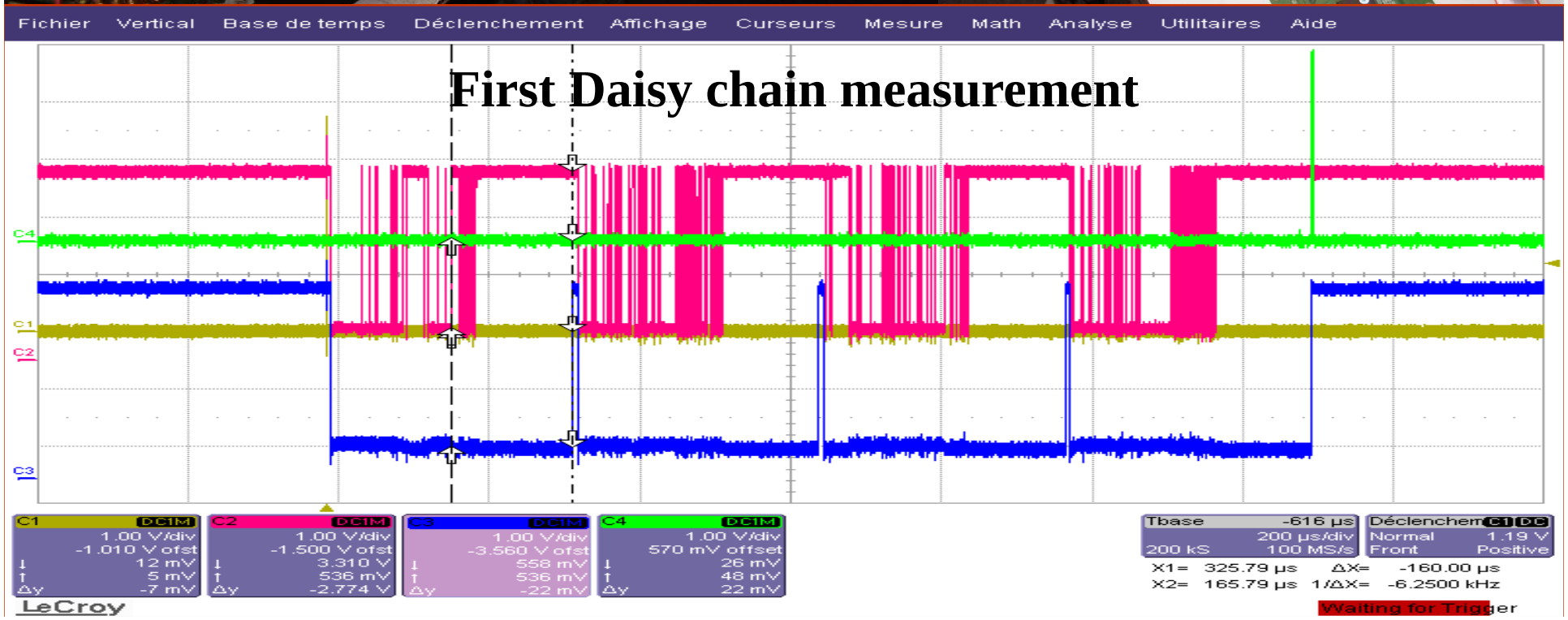




- Large activity on ASIC measurements
  - Validation of readout scheme with HaRDROC (Lyon, LLR, Orsay)
  - Analog characterization of SPIROC (DESY+Orsay)
  - ADC characterization on SKIROC1 (Clermont,Orsay)


Assembled(IPNL)


Readout software (LLR)


First Daisy chain measurement
Fichier Vertical Base de temps Déclenchement Affichage Curseurs Mesure Math Analyse Utilitaires Aide
C4
C1
C2
C3
C1 DC1M 1.00 V/div -1.010 V ofst 12 mV 5 mV Δy -7 mV
C2 DC1M 1.00 V/div -1.500 V ofst 3.310 V 536 mV Δy -2.774 V
C3 DC1M 1.00 V/div -3.560 V ofst 558 mV 536 mV Δy -22 mV
C4 DC1M 1.00 V/div 570 mV offset 26 mV 48 mV Δy 22 mV
Tbase -616 µs 200 µs/div 200 kS 100 MS/s
Déclenchem C1 DC Normal 1.19 V Front Positive
X1= 325.79 µs ΔX= -160.00 µs
X2= 165.79 µs 1/ΔX= -6.2500 kHz
LeCroy
Waiting for Trigger

Beam test [I. Laktineh CALOR 08]

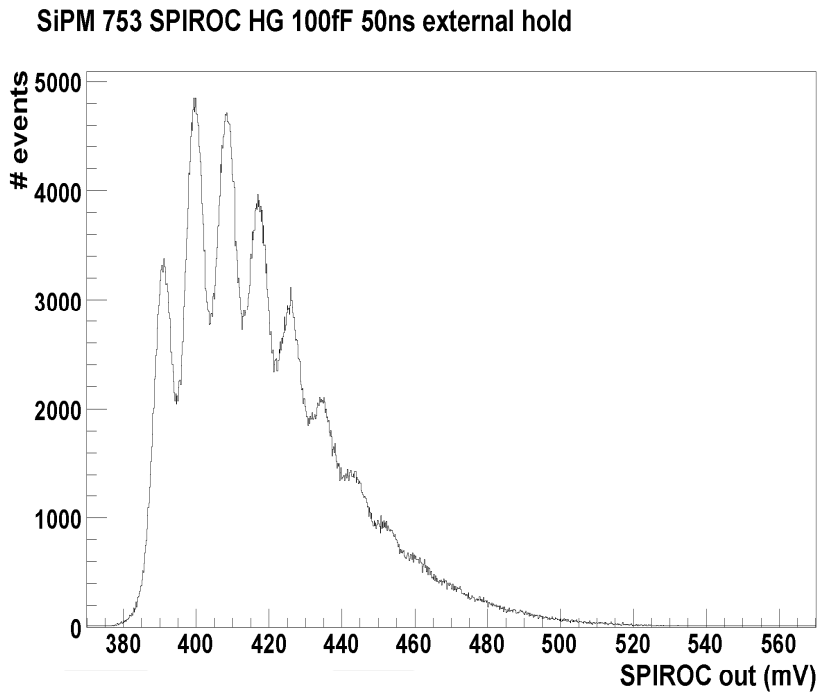
Final confirmation of the success of our electronic readout system will be coming soon with the beam tests with 5 fully equipped detectors (32×8 pads each):

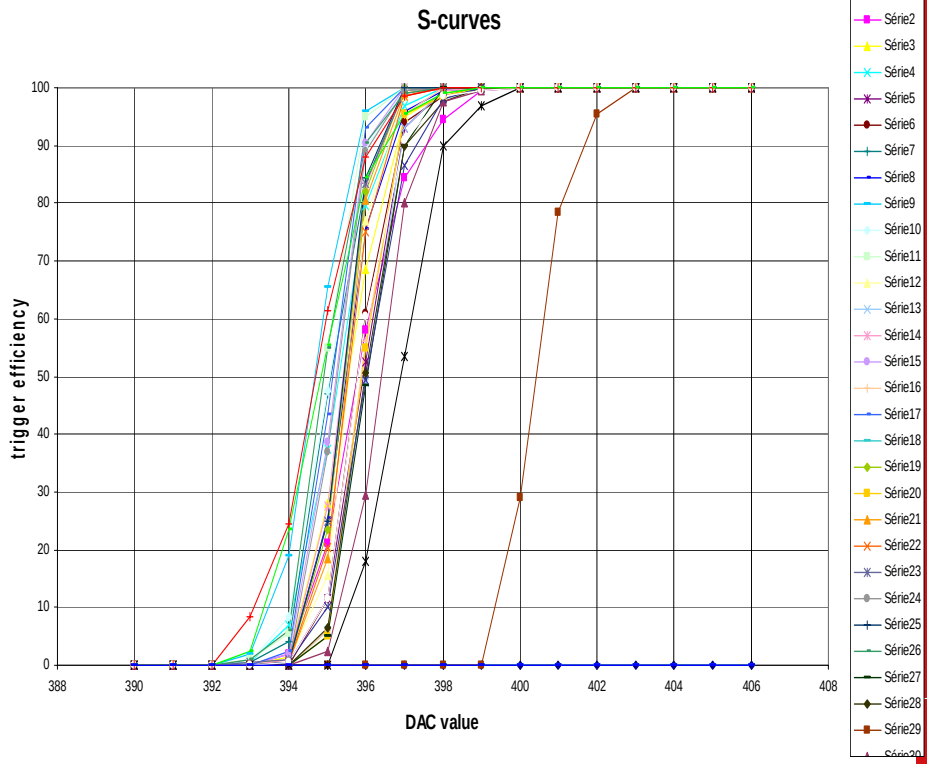
10-17 July :
beam test@ps-cern
3-11 August :
beam test@sps-cern

To study:
* Efficiency and multiplicity
vs:angle, position, particle multiplicity
* but also the first phase of the Hadronic shower

SPIROC performance

- Good analog performance
  - Single photo-electron/noise = 8
  - Auto-trigger with good uniformity
  - Complex chip : many more measurements needed
- bug in the ADC necessitates an iteration

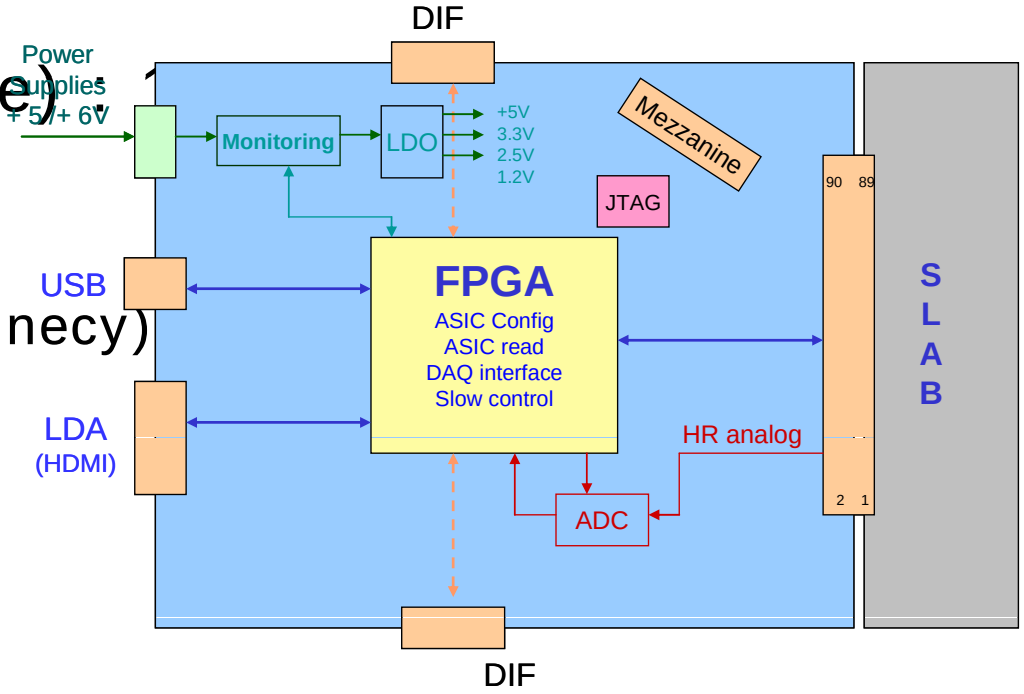




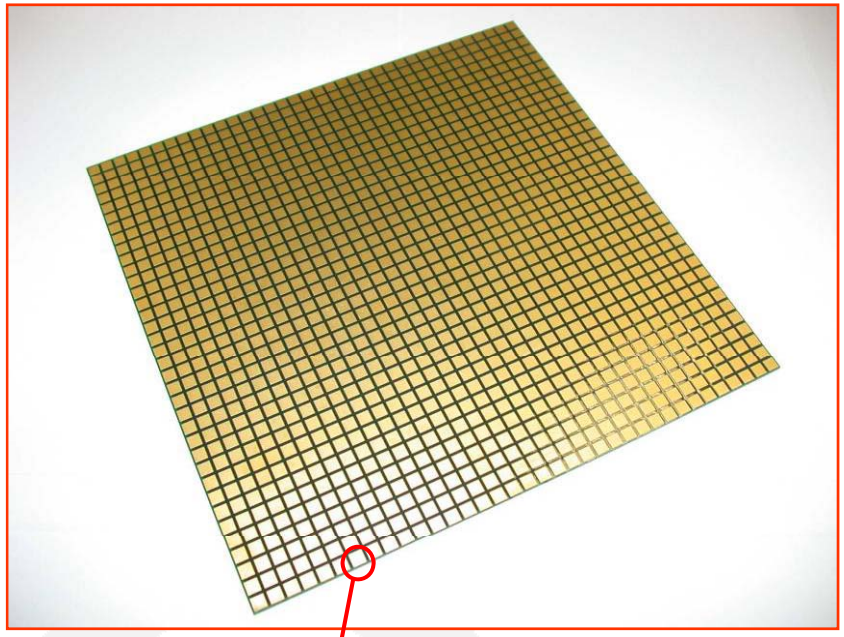
Activities in 2008 (2)

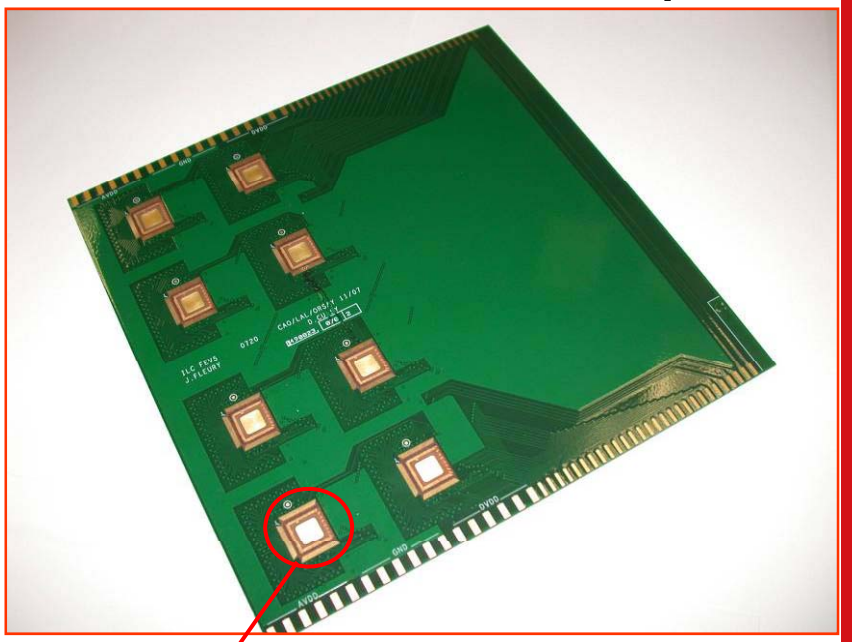
- Front End boards
  - ECAL, DHCAL & AHCAL (shown in detector subtasks)
  - Essential for detector mechanics finalization
  - Difficulties with ECAL prototype FEV5 (chip on board, minimal thickness...) => ~6 months delay experienced by present manufacturer

- DIF (detector InterFace) :
  - ECAL : UK
  - AHCAL : DESY
  - (not EUDET DHCAL : Annecy)

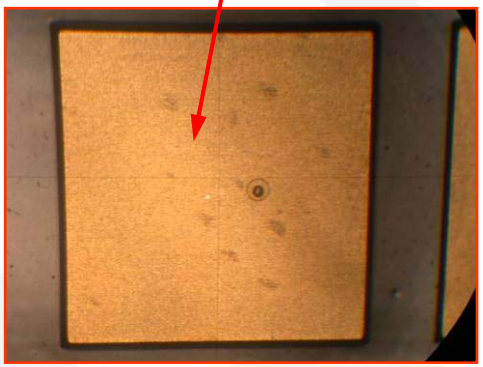


FEV5 : new PCB for ECAL

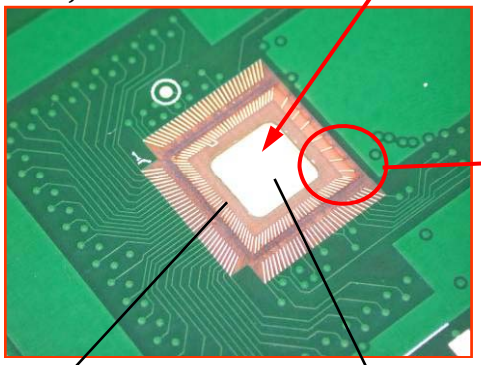


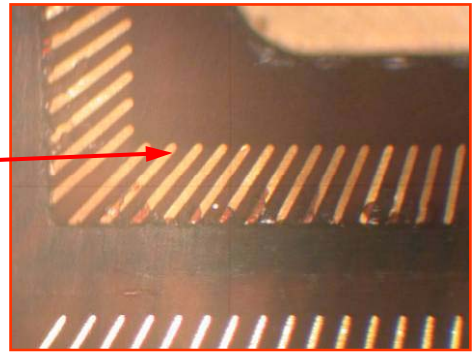


Global dimensions :
*180*180 mm, thickness 1.2mm*



*pixel dimensions : 4*4 mm*





0.15mm <depth<0.17mm

0.6mm< depth<0.7mm

Next steps

- ASICs
  - One engineering run with HARDROC2, SPIROC2 and SKIROC2 spring 2009
  - Same digital part and interface to DAQ2
  - Change of package -> smaller size
  - Should allow first prototype of EUDET ECAL and AHCAL modules mid 2009
- Front-End boards
  - Difficult for ECAL Difficult to keep milestone of dec 08 for final prototype
- Readout
  - First DIFs coming now. Tests starting.

EUDET FEE meetings

- London 8 jan 08
  - ~ 40 participants
- Orsay 2 jun 08

- Also CALICE meetings :
  - Argonne march 08
  - Manchester sept 08

Summary

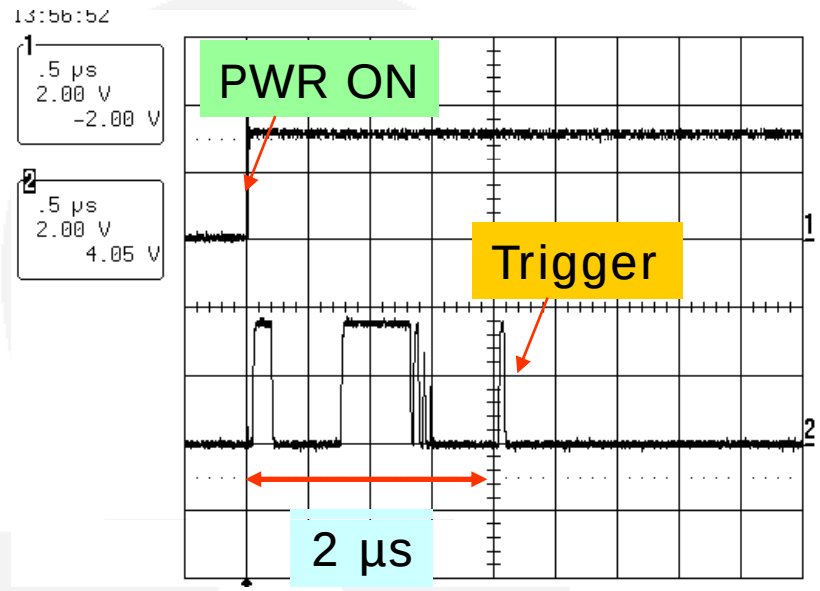
- 2nd prototypes of HARDROC (DHCAL) and SPIROC (AHCAL) submitted in june 08
- DAQ part validated with HaRDROC
- Power pulsing tests
- Front-end boards first prototypes
  - Difficulties with ECAL boards
- DAQ interface (DIF boards) prototyped

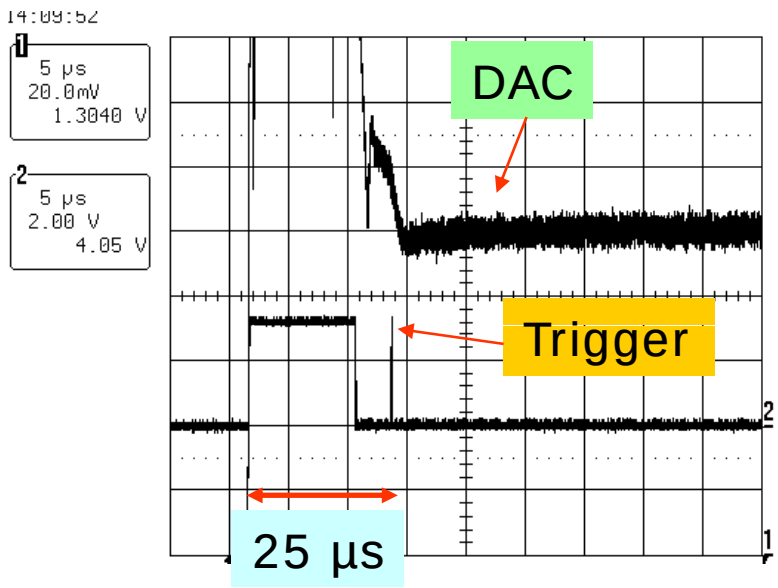
- One engineering run with all 3 chips (ECAL, DHCAL and AHCAL) spring 2009 : can be used as « production run »
- Expect busy period end 08- beg 09

Backup slides

Power pulsing : « Awake » time

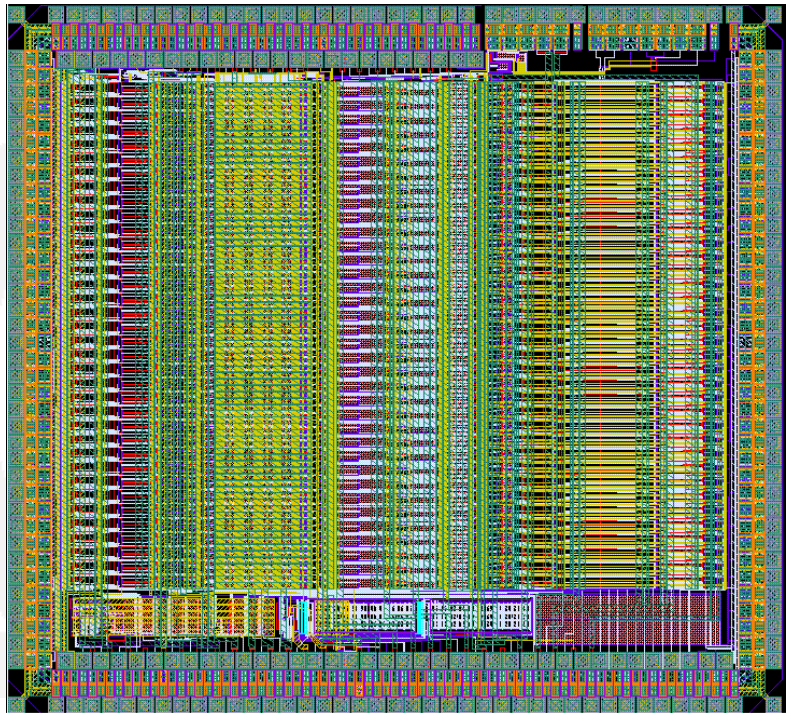
- PWR ON: ILC like (1ms,199ms)
- All decoupling capacitors removed : difficult compromise between noise filtering and fast awake time
- Awake time :
  - Anaog part = 2 us
  - DAC part = 25 us
- 0.5 % duty cycle achieved, now to be tested at system level



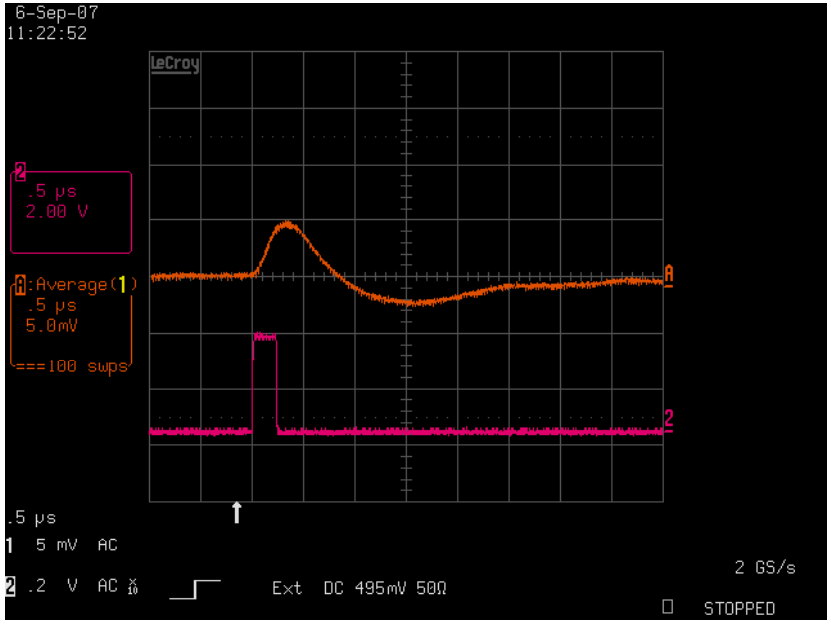


SKIROC for W-Si ECAL

- Silicon Kalorimeter Integrated Read Out Chip (Nov 06)
  - 36 channels with 15 bits Preamp + bi-gain shaper + autotrigger + analog memory + Wilkinson ADC
  - Digital part outside in a FPGA for lack of time and increased flexibility
  - Technology SiGe 0.35µm AMS. Chip received may 07

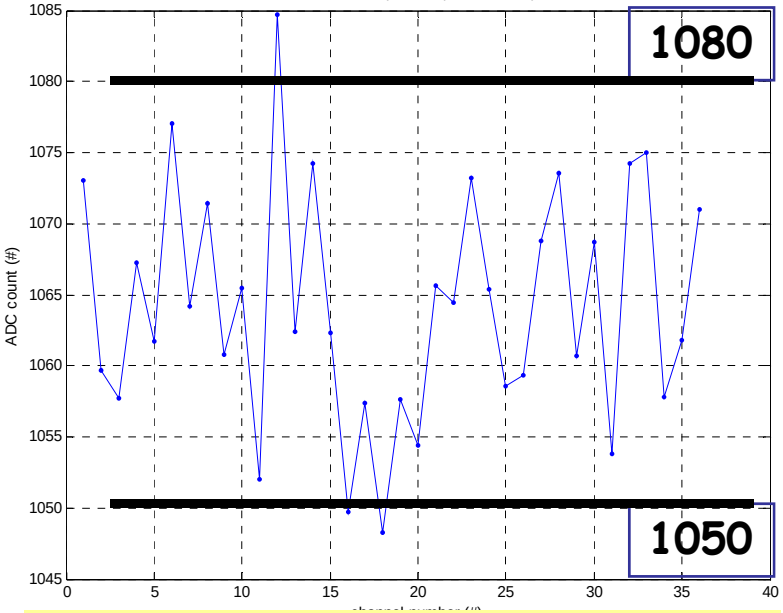


1 MIP in SKIROC

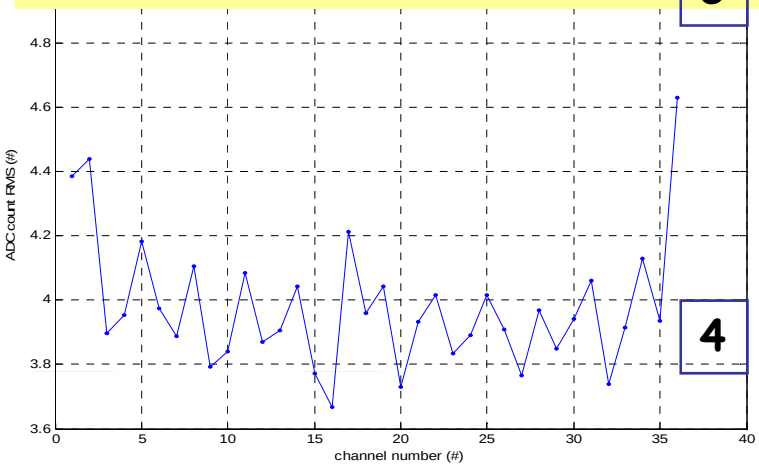


12 bit Wilkinson ADC performance

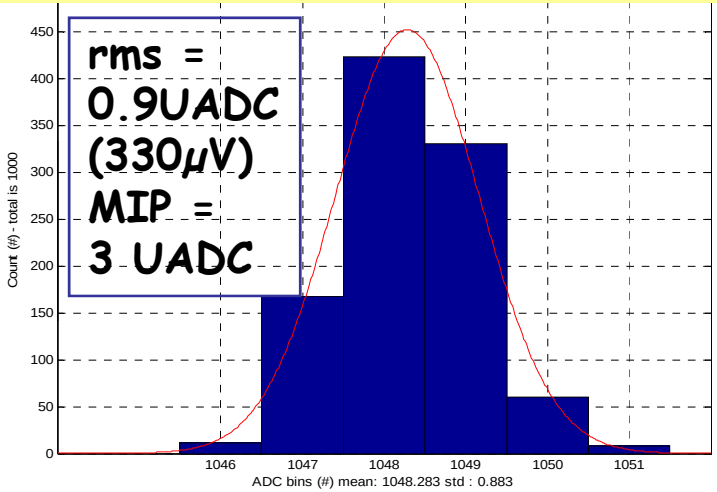
Pedestal value vs Channel number



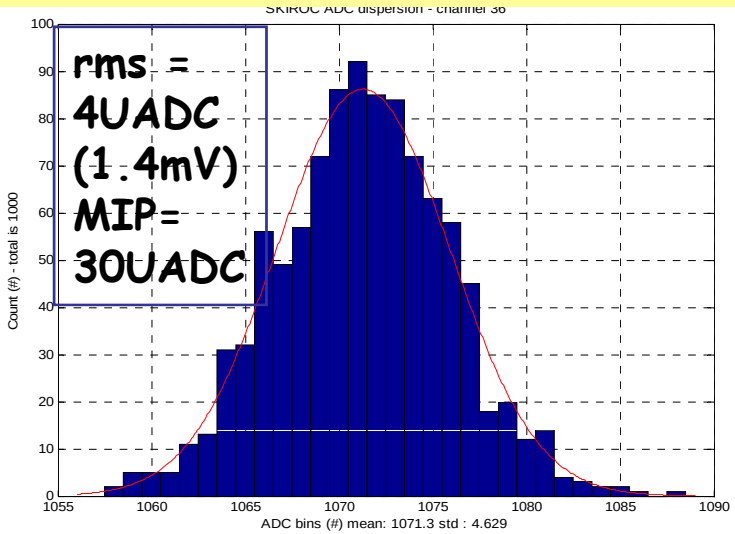
Noise vs Channel number



Noise in low gain shaper

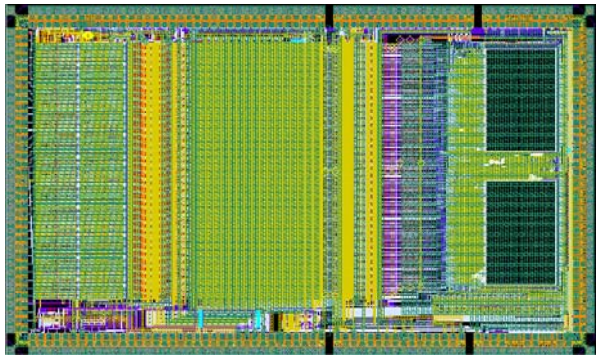


Noise in high gain shaper

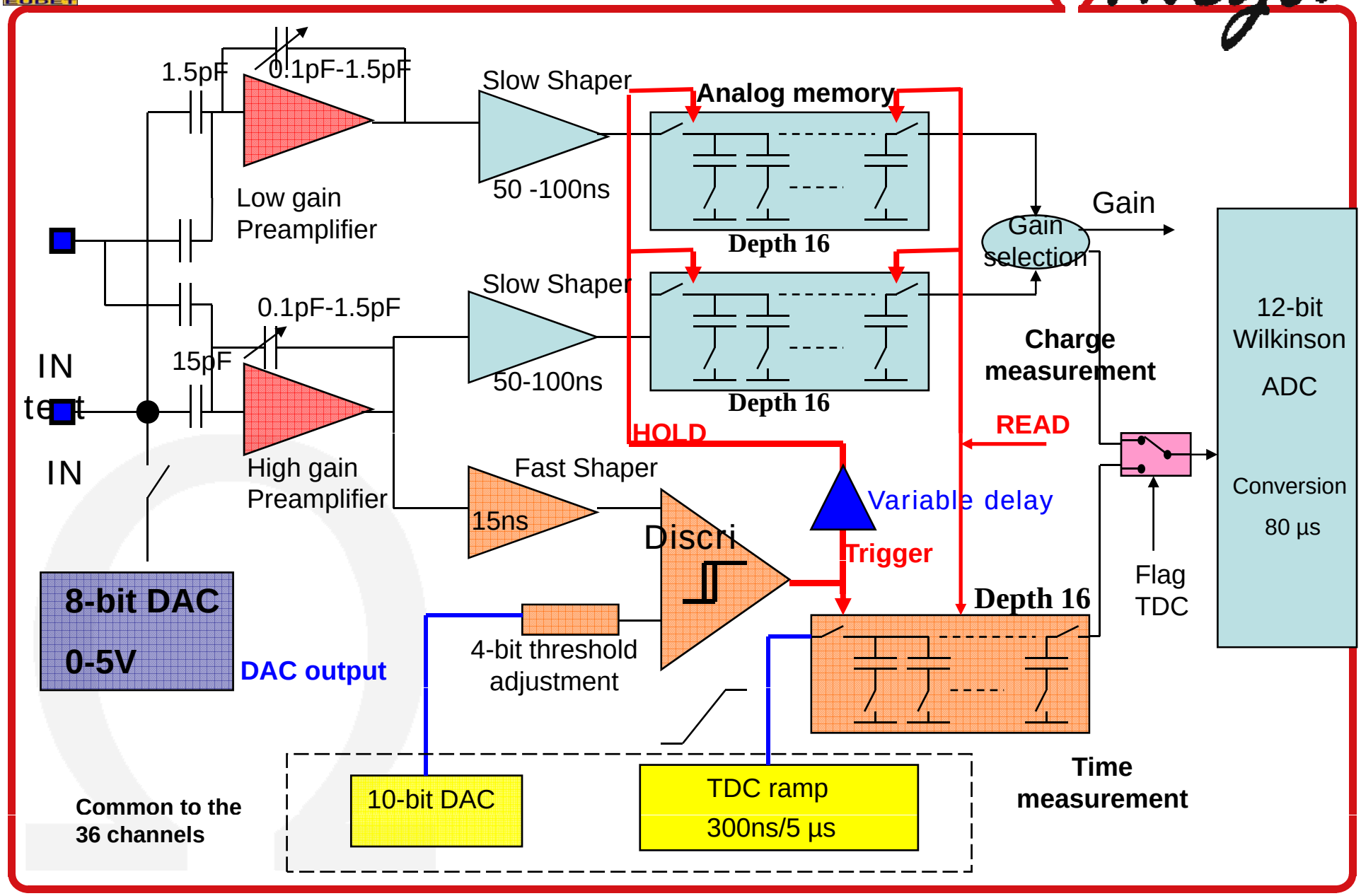


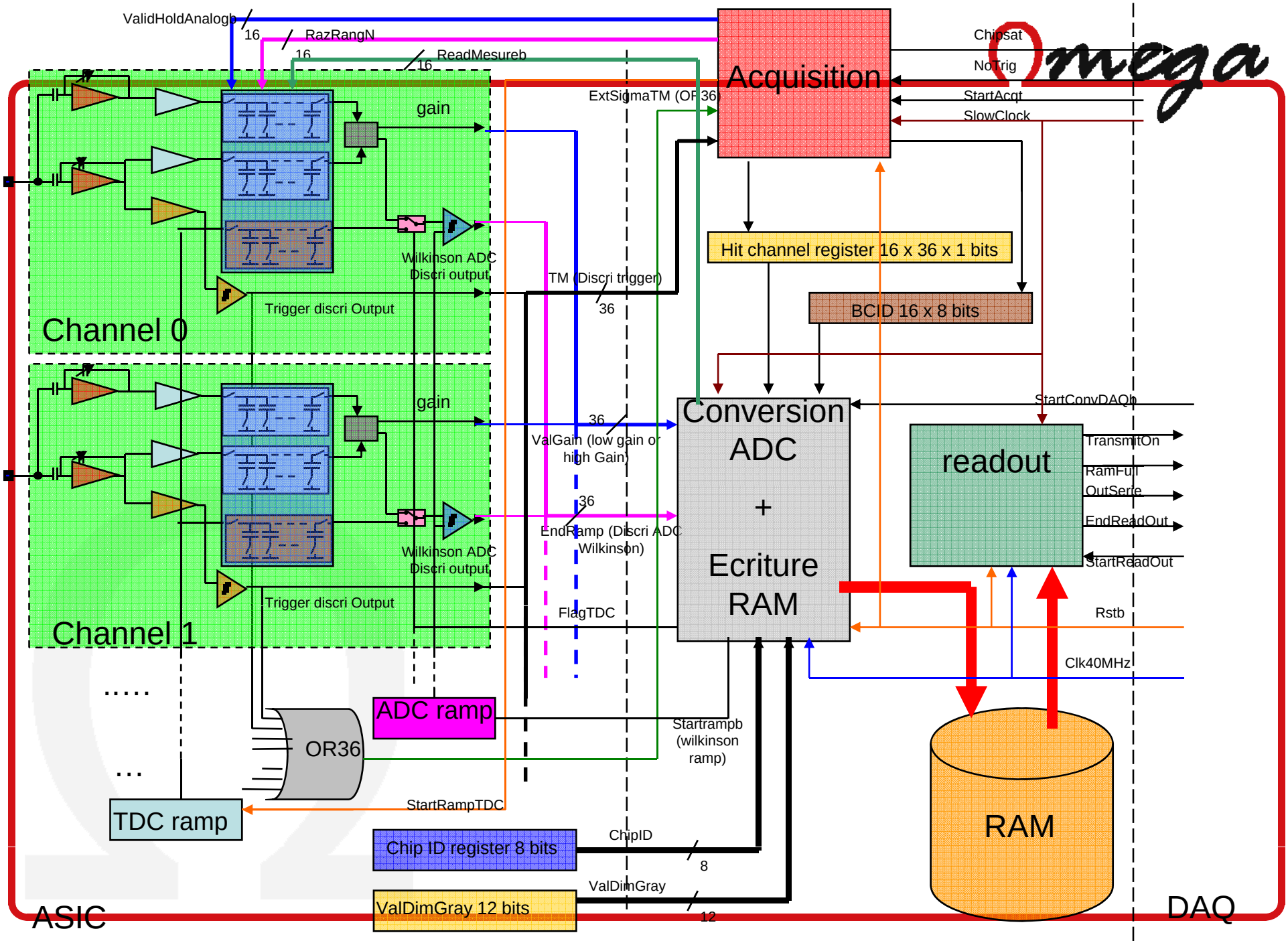
SPIROC main features

- Internal input 8-bit DAC (0-5V) for individual SiPM gain adjustment
- Energy measurement : 14 bits
  - 2 gains (1-10) + 12 bit ADC 1 pe → 2000 pe
  - Variable shaping time from 50ns to 100ns
  - pe/noise ratio : 11
- Auto-trigger on 1/3 pe (50fC)
  - pe/noise ratio on trigger channel : 24
  - Fast shaper : ~10ns
  - Auto-Trigger on ½ pe
- Time measurement :
  - 12-bit Bunch Crossing ID
  - 12 bit TDC step~100 ps
- Analog memory for time and charge measurement : depth = 16
- Low consumption : ~25µW per channel (in power pulsing mode)
- Individually addressable calibration injection capacitance
- Embedded bandgap for voltage references
- Embedded 10 bit DAC for trigger threshold and gain selection
- Multiplexed analog output for physics prototype DAQ
- 4k internal memory and Daisy chain readout



SPIROC : One channel schematic




ValidHoldAnalogb
16
RazRangN
16
ReadMesureb
16
Acquisition
Chipsat
NoTrig
StartAcqt
SlowClock
ExtSigmaTM (OR36)
gain
Wilkinson ADC
Discri output
Trigger discri Output
Channel 0
TM (Discri trigger)
36
Hit channel register 16 x 36 x 1 bits
BCID 16 x 8 bits
gain
Wilkinson ADC
Discri output
Trigger discri Output
Channel 1
36
ValGain (low gain or high Gain)
36
EndRamp (Discri ADC Wilkinson)
FlagTDC
Conversion ADC
+
Ecriture RAM
StartConvDAQb
readout
TransmitOn
RamFull
OutSerie
EndReadOut
StartReadOut
Rstb
Clk40MHz
.....
...
OR36
ADC ramp
Startrampb (wilkinson ramp)
TDC ramp
StartRampTDC
Chip ID register 8 bits
ChipID
8
ValDimGray
ValDimGray 12 bits
12
RAM
ASIC
DAQ