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JRA3 DAQ System

- DAQ System Availability updates:
  - DIF: Detector Interface
  - LDA: Link Data Aggregator
  - C+C: Clock & Control
  - ODR: Off-Detector Receiver
  - DAQ Software
- JRA3 DAQ Summary
  - System tests and delivery

DAQ System & availability:

From presentation (M. Wing) 14/07:

- Month 33 (Sep/08): “DAQ system prototype available”
  - Multiples of each component, complete chain moving data

Connecting all components puts particular emphasis on the interconnects and protocols

DAQ System: links

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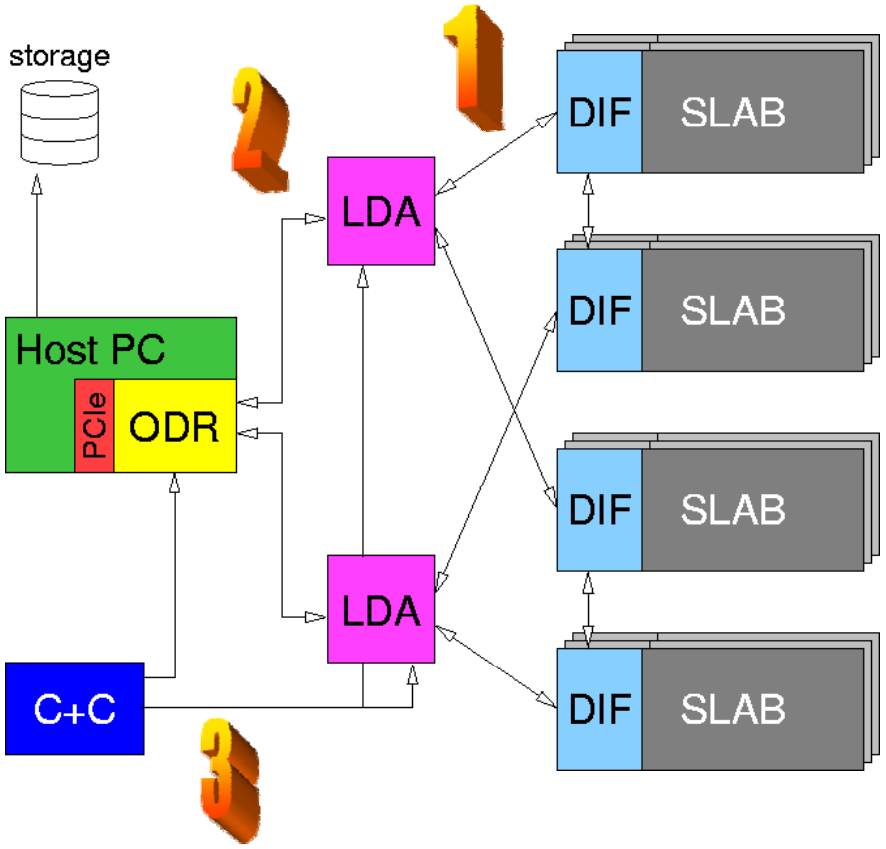
Link types used in ECAL DAQ:

1. DIF ⇔ LDA
   - synchronous, serial link with additional asynchronous pairs. 8B/10B encoded data
   - runs at N*machine clk: frequency 5..150MHz
   - HDMI cabling and connectors
2. LDA ⇔ ODR
   - Gigabit Ethernet (and TLK2501) serial protocol
   - SFP cage connector supports optical fibre
3. C+C ⇔ LDA
   - Compatible with LDA⇔DIF interface
   - C+C & DIF capable of stand-alone operation

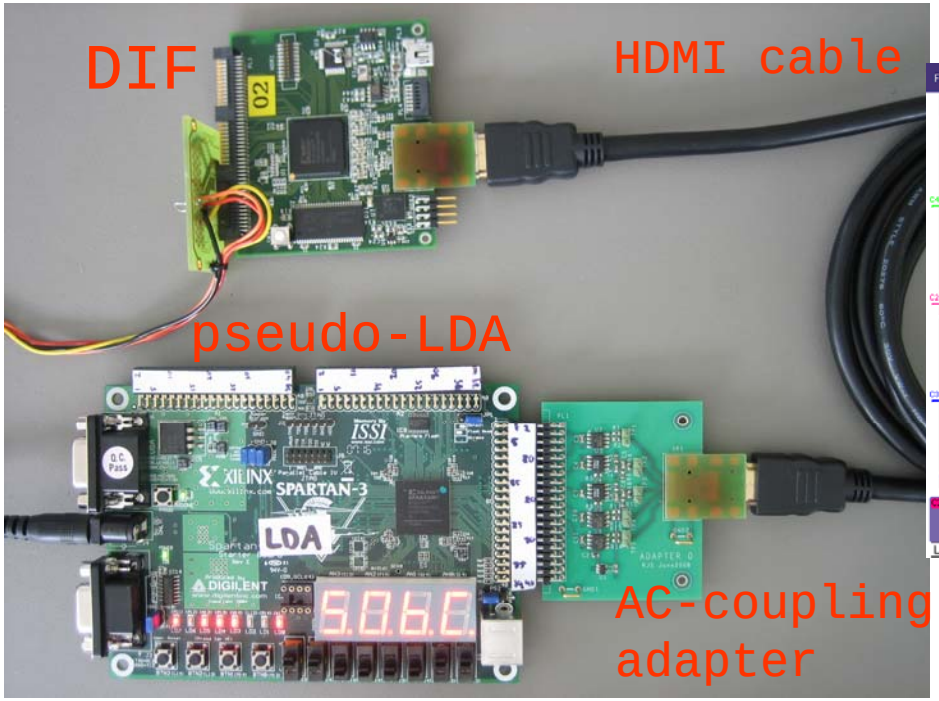


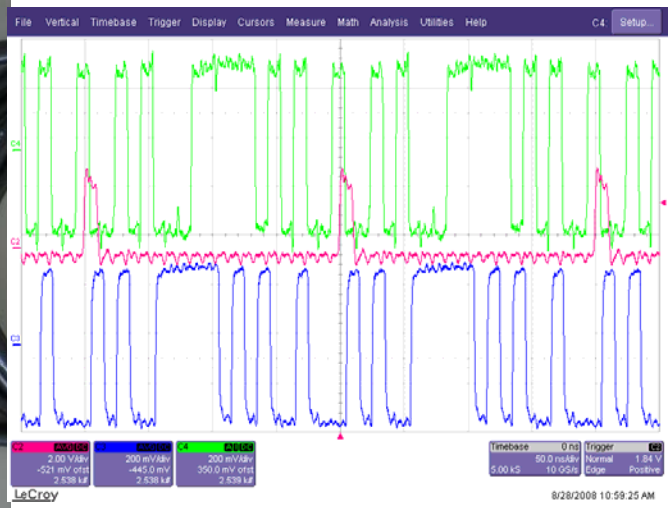
DIF, and LDA link status

M. Goodrick
B. Hommels
(Cambridge)

- 2 DIFs produced, parts available for 10 more.
- DIF hardware is (at least partly) functional

pseudo-LDA sends CLK & 8B/10B data @ 100MHz over AC-coupled LVDS on HDMI cables





data loopback in firmware seems OK: stable transmission

DIF ⇔ LDA link protocol

DIF ⇔ LDA protocol layer:

- Draft definitions for data formats under way
- Commands & Block transfers:
  - Block transfer packet size
  - Pre-defined sequences for commands (NB bit flips!)
  - Data integrity checks: parity & CRC
- ‘User-guide’ style writeup to be made

DIF: component hardware is available now. Next steps:

- Write firmware for DIF data generation
- implement minimal set of DIF commands in firmware for DAQ test
- Extend firmware towards full DAQ functionality

LDA status: interfaces

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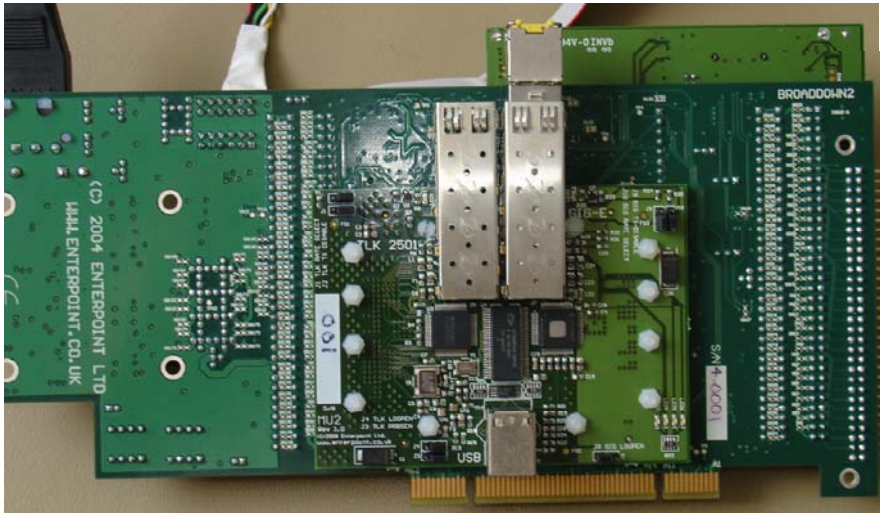
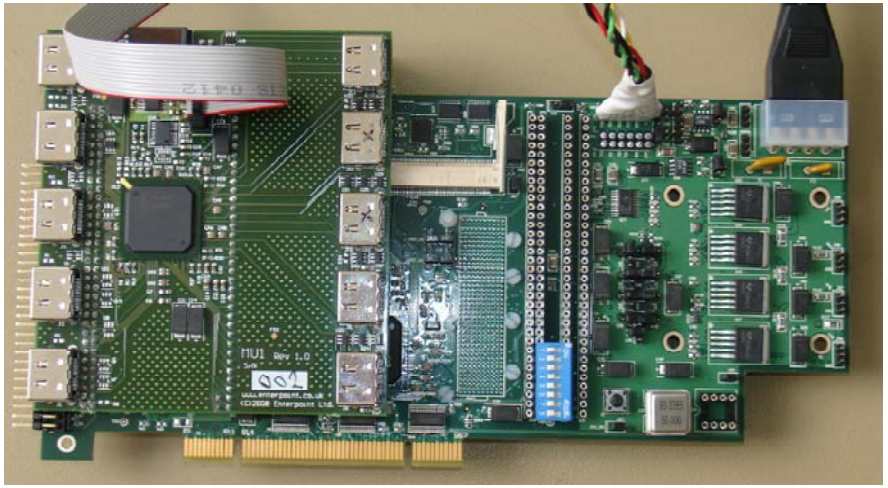
M. Kelly (Manchester)



Gigabit Ethernet interface:

- hardware in place
- Xilinx donated specific firmware IP to the project ☺

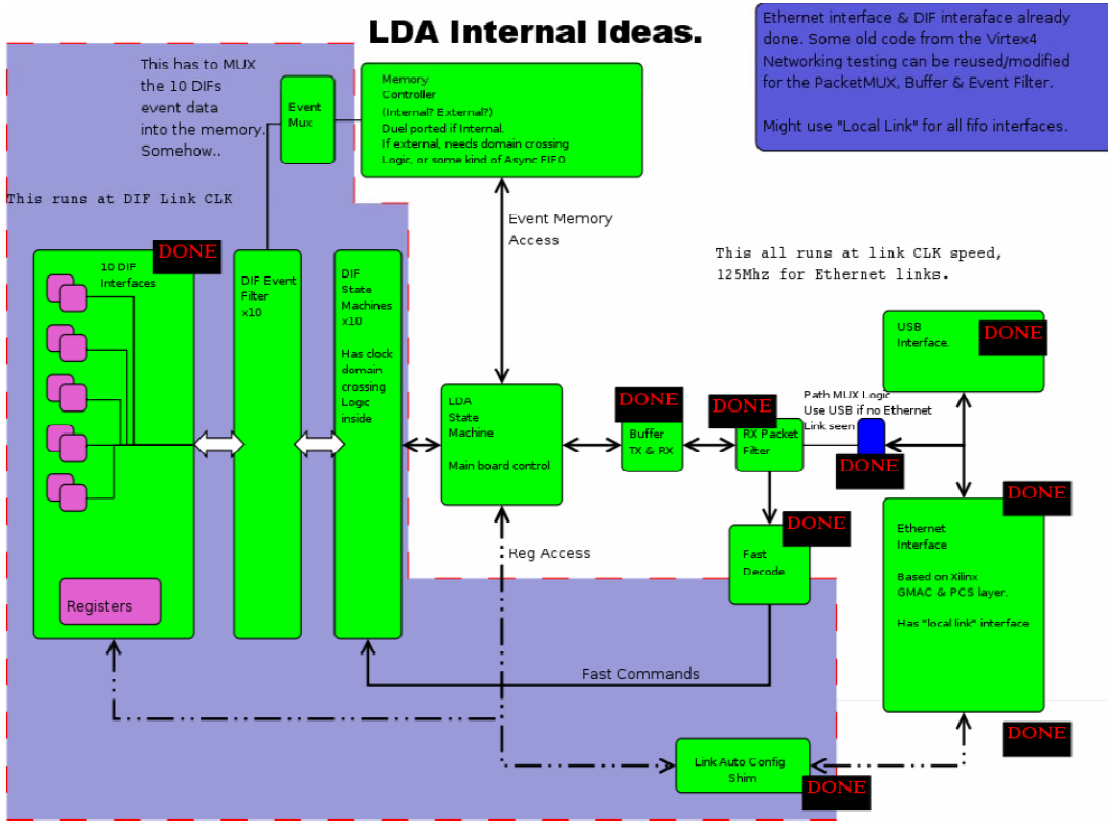


LDA ⇔ DIF interface:

- misunderstanding with manufacturer: links are DC coupled, 2 (of 10) not working yet
- some FPGA I/O pins not connected
- re-issuing of the board takes another few weeks

LDA status: firmware

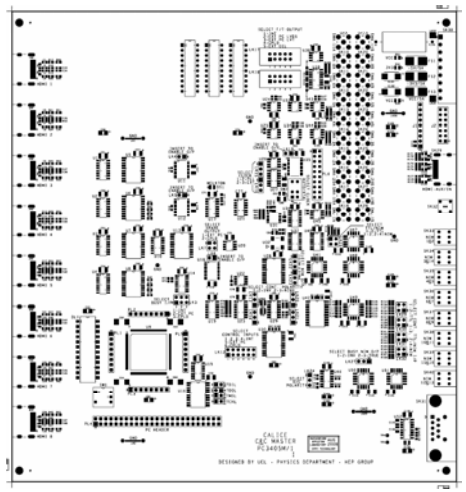
- Good firmware progress, despite the yet incomplete hardware
- Gbit Eth & DIF interfaces have priority over TLK2501 and USB
- details regarding DAQ buffer size, packet format & data handling to be addressed

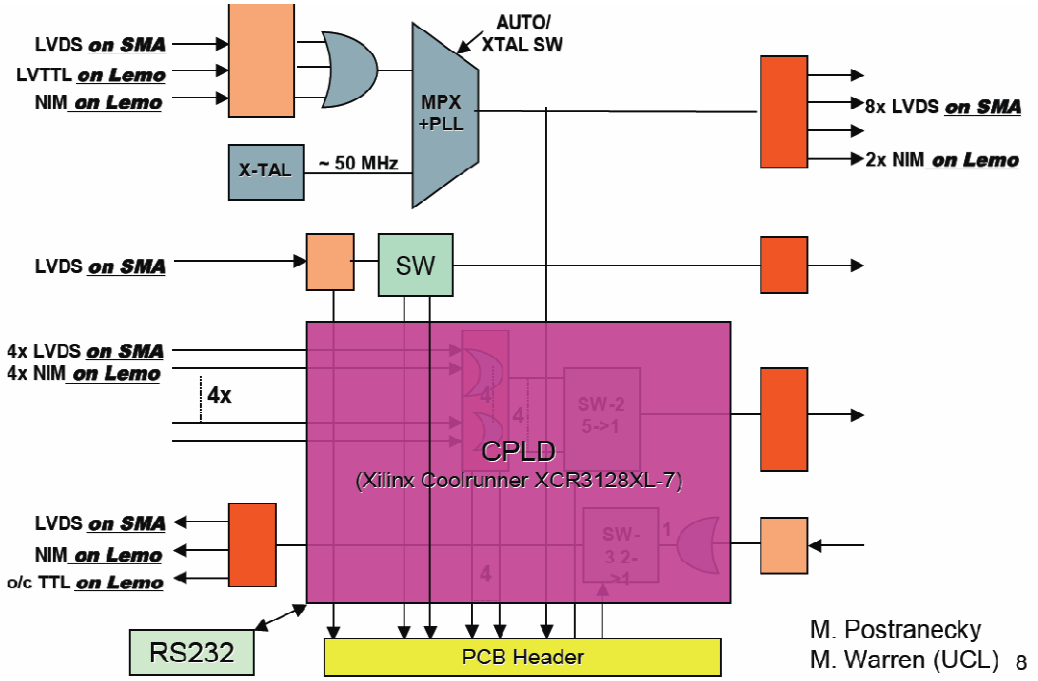


LDA: component on track to become available in September – awaiting re-spin of commercial dev. board

C+C status

- Design ready for ordering 2 initial prototypes
- Production lot of ~10 to follow later
- Detailed specification to be made available
- Implement basic functionality first, extend towards more sophisticated functionality later





C+C: 2 prototypes of the component are being procured: expected to become available in September

ODR firmware status

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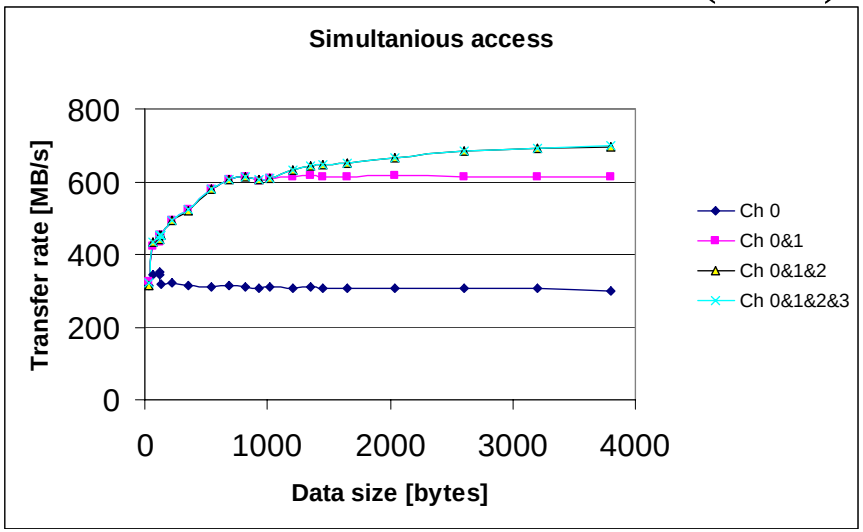
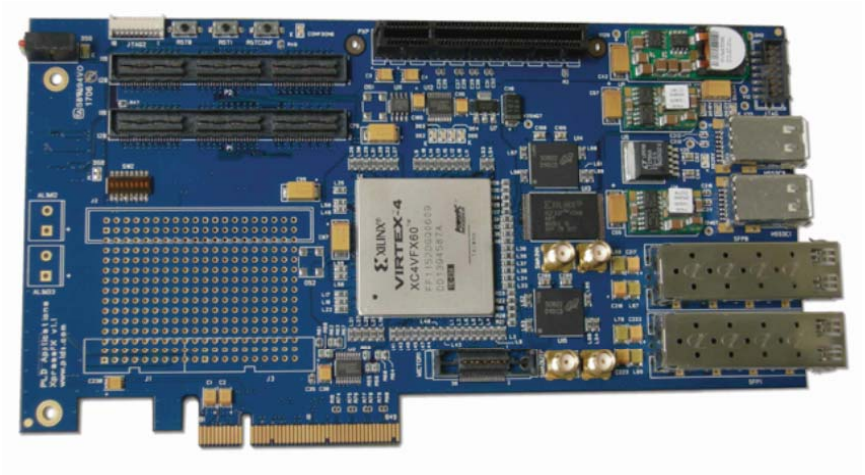
A. Misiejuk
B. Green (RHUL)
M. Warren (UCL)

- Firmware is in place
- Performance is sound –minor optimisation still ongoing
- Software drivers are integrated part of ODR development: seem to be working fine
- Main task is now integration into DAQ software framework



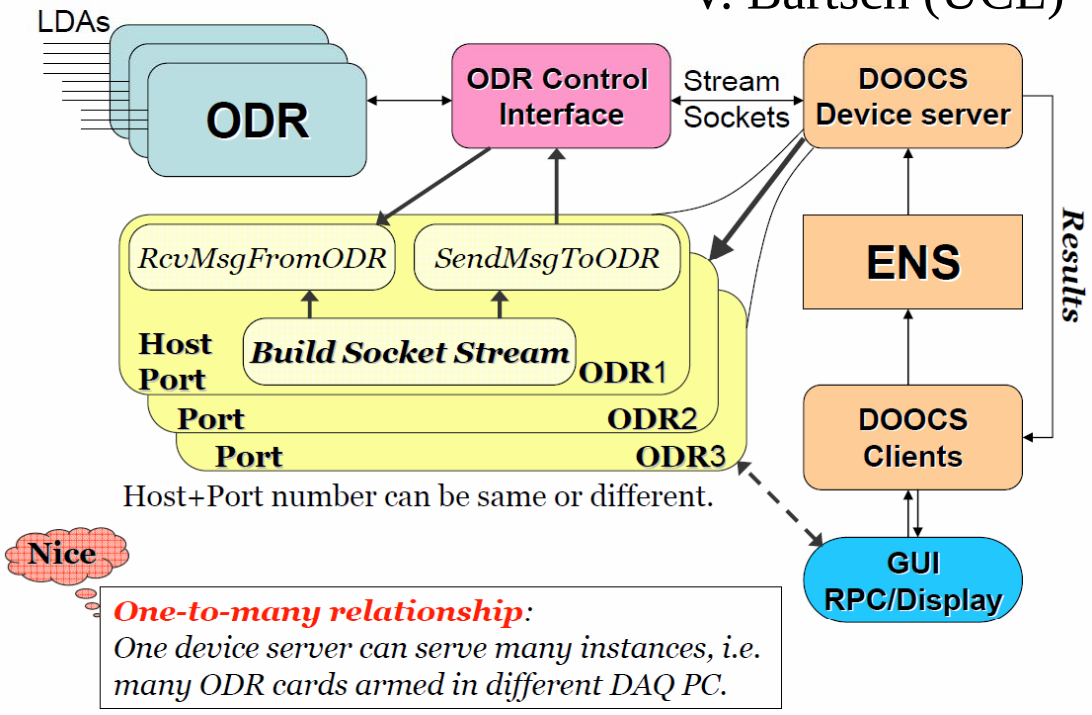


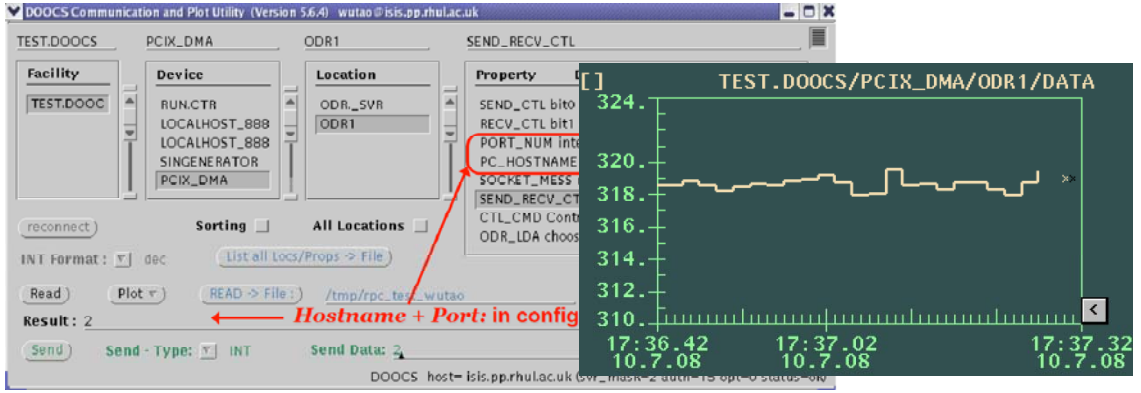
ODR: component is available.

ODR and DAQ software integration

A. Misiejuk,
T. Wu (RHUL)
V. Bartsch (UCL)

- DOOCS framework successfully used to establish communication with ODR
- Capable of message passing through ODR towards LDA
- GUI available for ODR controls
- Can run ODR tests and plot data rates
- System well understood
- Work to be done to integrate entire DAQ into framework





JRA3 DAQ Summary

DAQ system prototype availability:

- Most (prototype) components on track to become available this month
- Effort concentrating on firmware and software for fully integrated system test

DAQ system test – by EUDET meeting in Amsterdam (October):

- Full system test: Test Slab, DIF, LDA, C+C, ODR and DAQ software
- Passing data through entire chain
- Provide more documentation on components

Steps to completion:

- Multiple partial system tests: integration of various components
- Provide minimum functionality, extend where possible

Summary:

- EUDET programme is our essential work
- JRA3 Calorimeter DAQ reasonably on target