	CALICE Electronics meeting : minutes **DIF, LDA and CCC** **Detector running modes** **Signals and synchronization**	Draft 0

Revision status	**Comments**	**Date**
Draft 0	First version by RC. Distributed to participants for comments	31/07/08

CALICE Electronics meeting: minutes

DIF, LDA and CCC

Detector running modes

Signals and synchronization

Held on Tuesday July 29

The purpose of this meeting was to have a first thought on the way the data would be acquired on the detector (EUDET test beam) and to agree on common definitions. Various consequences about clocking and commands have then be discussed.

The meeting started at 14:05 CEST.

List of the participants: Mathias Reineke (DESY, remote), Bart Hommels (Cambridge), Maurice Goodrick (Cambridge), Matt Warren (UCL) , Aboud Falou (LAL), Franck Gastaldi (LLR), Vincent Baudry (LLR), Remi Cornat (LLR)

Agenda on Indico : http://ilcagenda.linearcollider.org/conferenceDisplay.py?confId=2890

The first part of the meeting was dedicated to Si-W ECAL.

1) **ECAL** DIF and integration on EUDET

ECAL oriented discussion on SLAB assembly and pending questions on mechanics at the DIF side (Bart, Aboud, Maurice and Rémi).

- Assembly procedure: Gluing of ASUs

Influence of soldering temperature profile ? Two techniques are investigated at Cambridge : Infrared (global heating, ~200 °C during 20s) or laser (local, ~0.5 mm, fraction of second).

At which step do we glue the wafers ? Before or after the assembly of ASUs ? : evaluate the risk due to the heating during gluing of ASUs + pressure applied on the brigde+ transportation from one location to another.

Assembly procedure: share of work and location of the operations? We are at the level of technological studies and things are done in many places : opportunity to “concentrate” the assembly on 1 or 2 locations only ?

- Assembly procedure: Kapton Film for HV

Shape of the Kapton film is not defined as well as the way to attach it to the wafers. The main constraint it to be able to unmount the ASUs : a single glued Kapton film is prohibited. On the other hand many Kapton ribbons (1 or 2 per ASU) would not make easy the connection at the DIF side.

Idea: try to use a single Kapton film, not glued or soldered. Need to ensure good contacts at the wafer backside: thermoformed bumps acting as springs ? To be studied.

- Assembly procedure: Mechanical compatibility of DIF and copper sheet/cooling pipe

New design of the adapter board and DIF with new dimensions “V1” (schematics shown). DIF is foresee to be “independent” and connection problems are located on the adapter board. Except for the colloing of the DIF fpga.

- Cooling of the DIF fpga

Does the DIF fpga need to be cooled ? What about its impact on the SLAB (ROCs) cooling ?

The DIF fpga is connected to a ground plane acting as thermal dissipater. Connecting this plane to the cooling pipe seems electrically risky. The copper sheet could be extended up to the DIF : not realistic. A dedicated connection between the cooling pipe and end DIF (single contact on the fpga ? use of thermal foam on the whole board ?) would be better. See above.

- Assembly procedure: Mechanical compatibility of DIF and LV, HV connections

HV and LV cables will come along the cooling pipe. They will be connected to the DIFs. The actual design foresees the HV/LV connectors to be on the adapter board.

Future version of the DIF should provide connectors for LV / HV within the same dimensions.

The huge capacitance needed in the case of power pulsing from a low current power supply is not included yet.

- Thermal tests: location of FPGA

Thermal simulations have shown a strong impact of the DIF fpga (power dissipation and location). The location has to be known quickly to enable the design of a “thermal demonstrator” (forthcoming month) as well as to tune the simulations.

- Thermal tests : Power dissipation of the DIF fpga.

The allocated power budjet (used in thermal simulation) for the DIF is 3 W. It is probably over-evaluated. Bart provided numbers about a similar fpga loaded with a firmware close to what it could be for the DIF. The power dissipation is around 250 mW + 10% per additional lvds I/O. The impact of internal logic is low, consumption from the I/Os is dominant. Some LVDS I/O are missing : new numbers should be provided soon.

A new power budget of 1 W would be more realistic for the simulations.

- Design status of Ecal DIF and future version

See slides attached to the agenda.

Then the discussion continued on various topics (not in time order in the following)

2) Short review of the previous meetings

- Sharable blocs

Good feedback from users of the 8b/10b interface.

USB blocs are in use for the HCAL test beam, limitation exists for the DAQ rate (20 Hz) but should be ok for Slow control and debug. No feedback from other users.

LPC (Clermont) won't work anymore on ECAL DIF for the cosmic test bench. Thus a common bloc for the DIF-ROC/SLAB itf is not designed. Rémi proposed to start working on this bloc (proximity of LAL is an advantage).

- USB

Questions about the need to program the PROM with IDs, simple SW procedure for first attempts ?

- Running modes

Following the various meeting where running modes have been described, a document is in preparation. It has been discussed again, see below.

3) Requirements for thermal tests and power pulsing : **Demonstrator running mode**

The next CALICE/EUDET prototype will be used to prove the technological feasibility of the system from the point of view of the mechanical structure, thermal dissipation, power consumption (power pulsing), front-end chips embedding, noise …

The detector should run in a special mode, different from the one used for test beam (higher event rate, triggered DAQ, stringent timing requirements due to the beam structure) which is not optimal for such studies.

Several points have been discussed, trying to find solutions to ensure low power (minimum heat dissipation of DIF minimizing its thermal impact on the SLAB) as well as data exchange optimizations:

- Low power firmware loaded (or configured) into DIF

Several DIF features could be disabled like external memory, spare HDMI, USB, … Storage buffers could be reduced in size. Hibernate state of DIF ?

- DIF-LDA link configuration

As only one ROC is read at a given time, the data rate at the output of DIF cannot exceed the Slow clock frequency (actually it has to be multiplied by the number of partitions). If chips are partitioned, partitions could be read one by one. The read out time can be longer than for test beam mode assuming 199 ms between bunch trains and then slow signal could be used. Serialization could be avoided?

- Hardware configuration

Check if some components can be disabled.

- Beam structure

The demonstrator mode relies on the availability of an ILC like beam structure. If it not the case, the val_evt signal could be used to prevent ROC to trigger (emulated beam structure).

- Signaling

No external triggers, no slow control as well commands during acquisition and conversion (except start/stop train).

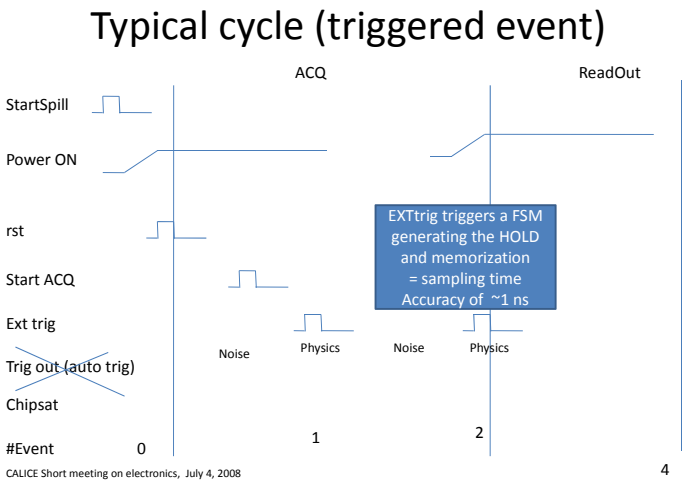
Some ideas about the demonstrator mode have been expressed. This mode is still to be specified in details.

4) Triggering scheme for test beam : Test beam running modes

Test beam modes have been reviewed from the point of view of synchronization and DIF-LDA link optimization.

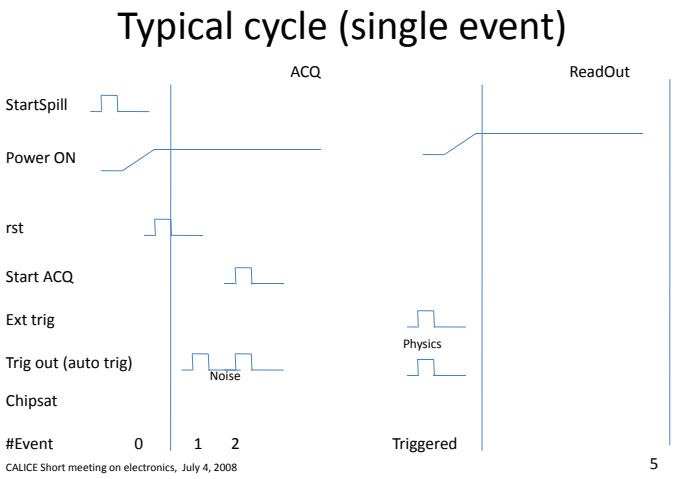
- Ext trig

An external trigger is used to select events (only triggered event are stored in the ROC rams). It triggers the sampling of the date (HOLD signal). All channels can be forced to acquire the event.



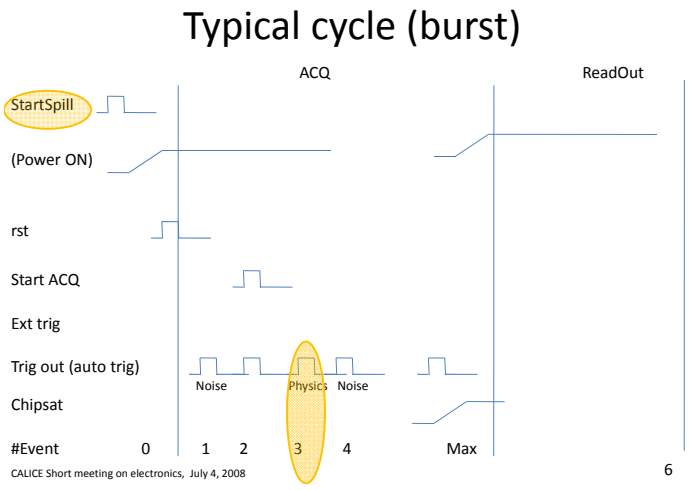
- Int trig, single

The ROCs acquire data in auto-trigger mode but a physics event is selected thanks to an external trigger then the acquisition stops.



- Int trig, burst

The ROCs acquire data in auto-trigger mode. Acquisition is stopped when a first chip is full (ChipFULL signal). It avoid other data to be acquired by other chips and then the read-out time of the whole detector is optimized. The acquisition process is launched again right after the read-out. The event rate is then optimized.



For the Bust mode, the chipsat signal has to be transmitted to the CCC system (BUSY) which then need to feed all DIF with a StopAcquisition.

The DIF-LDA connector provides 5 links : Clock, SerialDataIN, SerialDataOUT, FastIN, FastOUT, FastIN.

The fastIN usage could vary according the running mode (avoid another signal to be transmitted).

Mode	**FastIN**	**FastOUT**
Ext trig	TRIG	N/A
Int trig, Single	TRIG and STOP	N/A
Int trig, burst	STOP acquisition	BUSY

5) Feedback from DHCAL TB

See Vincent's slides.

6) Status of ECAL DIF, LDA, ODR, CCC

See slides in the agenda.

- Ecal DIF hardware available, firmware is being developed (LDA side)
- Problems encountered on the LDA-ODR link testing the LDA (TX data corrupted).
- CCC board designed (schematics and first P&R)
- ODR is working (fast dump of data, SW), together with LDA soon (future upgrade).

7) Synchronization and control

Various specific questions have arisen during the meeting. Some of the most significant are listed below:

- Commands

Commands are sent on the SerialDataIN using a K character. It can be sent interrupting the data flow. Several K characters are available in addition to 8b command ID (first bit used to select first or second DIF though the DID-DIF link). The command is issued at the DIF side with a latency of 4*8 fast clock periods. See slides.

Special SYNC command issued at the DIF side selecting the clock edge: clock and time alignment. See slides.

For the int trig, burst mode, the re-start of the acquisition can be done thanks to a command (small latency can be neglected with respect to the time spend for the previous read-out)

First attempt to list all needed commands (Bart): clock on/off, start/stop read-out, start/stop transmission, read temp and voltage probes, mode switching, force neighbor link (DIF-DIF) resets, R/W identifier, R version, …

- Busy

Ram saturation (ChipSat) signal are sent to LDA by DIF (BUSY signal). All BUSY signals have to be ORed at the level of CCC. Then a feedback have to be send to the whole detector to stop acquisition and start the read-out. The feedback should be fast (latency) enough to avoid many more data to be stored in ROCs (it would result in the degradation of the event rate).

No additional fast line is foreseen. The feedback will use the EXT TRIG fast line.

- Latency and phase adjustment of signals

Questions about the need to adjust the phase of each clock (CCC-LDA) or only at a global level (one phaser before the fan out stage).

Same question for the FastIN signal.

Commands can be aligned on a given FastClock (rising) edge (20 ns steps typ.).

Not all the outputs of CCC board can be phase controlled. Timing alignment will essentially be done adjusting cables lengths. Do we need to implement “delay chips” (to avoid if possible) ? with which time steps ? at which level (CCC, LDA) ?

Beware of the SLAB length resulting (for Si-W ECAL) in a delay of about 10 ns.

For DHCAL, the TDCs require to be initialized (StartSpill) at a well known time with a small spread over the detector.

Counters should be used on DIF to crosscheck timing or BXid, trigger number etc…

CCC signals are AC coupled allowing pulses only. BUSYs cannot be ORed by hardware nor held by DIF.

- SlowControl and partitions

Slow control lines suffer of a heavy capacitive load. The speed is then slow (1 Mb/s) :about 100 ms per SLAB.

As the new gluing technique of ASUs allows a highest number of connections, the opportunity to double the SC lines has been envisaged (Si-W ECAL SLAB).

- StartSpill (aka TrainSync)

A Start of Spill (or train synchronization) signal should be provided by the machine interface. It is supposed to come in advance to allow a clean reset and power up to be performed. A similar signal is needed to re-start acquisition in the case of the train or spill is not finished after the read-out (event rate optimization).

- Ext trig

The meaning and the use of ext trig vary according to the running mode. When in the ext trig mode, it is used to trigger the HOLD (sampling time) then the writing in memory. The accuracy of the timing should be around 1/10 or 1/20 of the shaping time.

When in int trig, single mode, the ext trig validates the writing in the analogue memory and should occurs during the HOLD active time.

- Resets

Resets will be done with commands. It requires a proper functioning of the DIF-LDA link (DIF-DIF link can be used instead).

No hardware reset is foreseen at the moment. Should we have one?

Possible solutions for an hardware reset :

  - Switch the power off : from where ? with which granularity ?
  - Switch off the clock and detect the mean level at the DIF side (reliability?)
  - Use undefined state of differential pairs (common mode modulation) but AC coupling!

Conclusion: A lot of various aspects of the design have been discussed (Si-W ECAL orientated). Some points need some clarification: accuracy of timing adjustments, resets, demonstrator mode. Several specification documents are in preparation and should help to complete the work.