DAQ signals (again) & a few lessons from DHCAL TB

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Three TB Running modes:

- **Physics**
  - as fast as possible *IN SPILL*,
  - poissonian stat → As low as possible PILE-UP
  - Data with “low occupancy” (particle type & E dependant)
- **Demonstrator**
  - as close as possible from final ILC conditions
    - power pulsing, auto-trig
    - beam conditions close to ILC ? (Duty cycle, occupancy)
- **Calibration / noise**
  - *a priori*: off spill, fixed rate
  - all cells (“maximum occupancy”)

TB DAQ modes

buffer (Hardroc: 128, Spiroc: 16)

Single Event + Ext. Trig

- External trigger (from hodoscope or calibration system) = HOLD
  - Stop Acq, Hold analog data + sampling, Start Acq
- Noise & Beam condition safe (only 1 evt per trigger)

Single Event + auto-Trig

NOW USED IN DHCAL TB

- **External trigger** (hodoscope) → DIF
  - Stop Acq, Read chips (last evt ~ triggered one), Start Acq
- **Data sync** (for Event building)
  - On synchronized BC ID → **need for a SYNC @ MClk (100– 400 ns)**
  - On trigger timestamp (e.g. On DIF Timecounter on last internal trigger to ext. trigger): time = (BC-LastBC) × τ_{BC} – DiffCounter × $\tau_{DiffCounter}$
  - **BUT: for the AHCAL/Spiroc:** the TDC signal needs a SYNC of the clocks **±1ns**

Rems:

Fine if no RAM full
e.g. # rejected triggers + noise event per chip < 128 [16 for the ECAL/AHCAL!]

Sync can be x-check by a BC counter in the DIF's

TB DAQ modes: single event with auto-trig

Using ROC chips: auto trigger, buffer (Hardroc: 128, Spiroc: 16)

Single Event + auto-Trig

External trigger (hodoscope) → DIF

Stop Acq, Read chips, Start Acq

Data sync (for Event building)

On synchronized BC ID → **need for a SYNC @ MClk (100– 400 ns)**

On trigger timestamp (e.g. On DIF Timecounter on last internal trigger to ext. trigger)

BUT: for the AHCAL/Spiroc: the TDC signal needs a SYNC of the clocks **±1ns**

Single events “in phase” : Noise runs

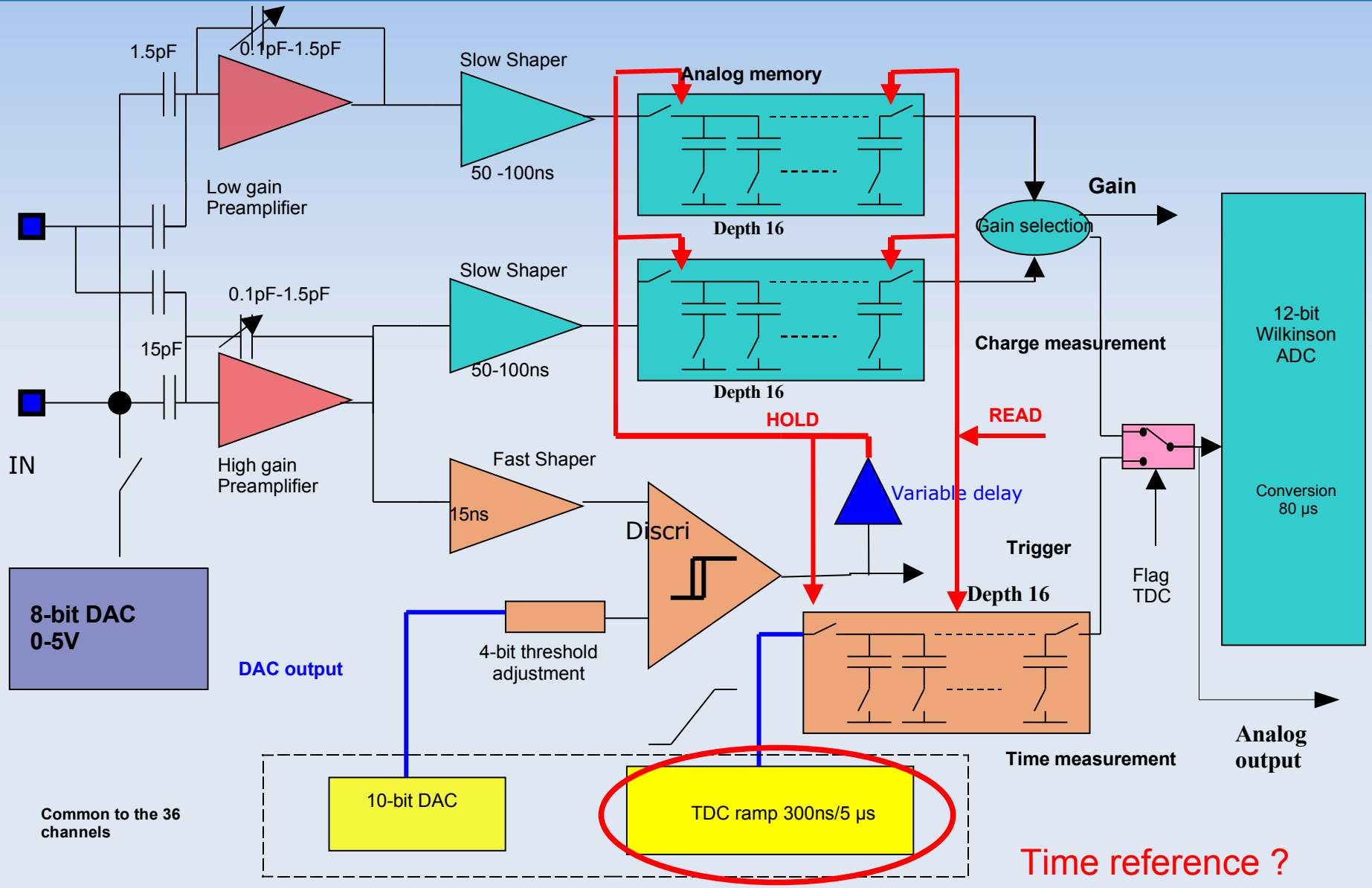
need a fast trigger (δ<1ns ???? TBC)

Rems:

Fine if no RAM full
e.g. # rejected triggers + noise event per chip < 128 [16 for the ECAL/AHCAL!]

Sync can be x-check by a BC counter in the DIF's

SPIROC diagram



TB DAQ modes

Burst mode (≤128 FOR DHCAL): *TB data, Calibration, ILC*

No external trigger but independent recording of trigger mode (⊃ Timestamp)
(could be 1 HR recording Trigger bits)

- Data sync internal [synchronisation on reset of BC ID on all HR], at the Beg of a Spill
- Internal «RAM full» management needed
  Every 128 DHCAL [ECAL: 16] events

  LOCAL: in DIF with immediate RO of SLAB

  - 4 ms for 100 GeV π's without Reset (avoid loss of sync)
  - **Indiv DT**: might be hard too handle.
  - ~~Local storage of data ????~~

  Global

  - fast Ramfull → DAQ (stop of Acq, RO of all chips, and restart)
  - periodic interruptions
  - *counting of part*: for example one Hardroc for the Hodoscope (large scint)
    → RAMfull (with some additional events at the beg to produce an offset)

Signals

Clock

- Machine Clock (Mclk)
  ×16 on data (?)
- MClk rebuild in DIF's
  from Data clock (?)

fast sync

- ≤ 1/MClk
  (≤1 ns if TDC's)
- Sync @ SpillSTART ?

External trigger

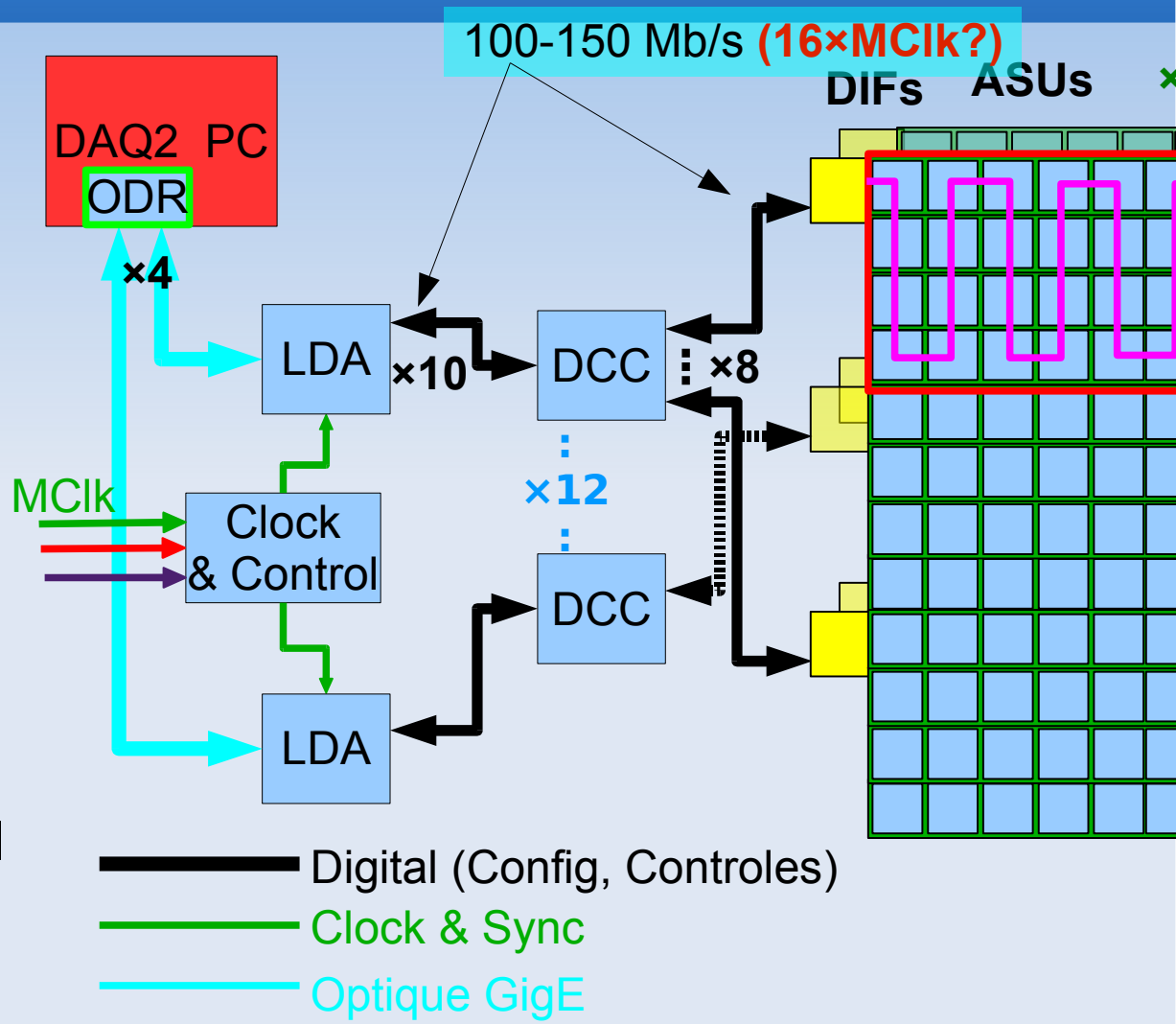
- δt ≤ 1/MClk

StartAcq/tStopAcq/EndSpill

- from ODR

BUSY

- RamFull: DIF→LDA→C&C→trig
- LDA → ODR (⇒ End of RO)



Propositions (outdated ?)

Trigger

- have a simple logic in the C&C card:
  - OR(trigger inputs) AND !OR(BUSY)
  - could go to the DIF as a *fast command*

Fast signals

- = sync signal @ beg. of spill
- needs a special treat[t] in LDA & DCC and a **dedicated line to the DIFs** (reason: a *fast command* has (10 bits/100MHz = 100ns jitter)

BUSY

- Generated by the DCC/LDA and **released** as soon as the **data** from all DIF is **in memory.**
- Option if needed: a RAMfull could also generate a BUSY (via a status word DIF→LDA), propagated to the C&C card and generating a trigger to stop all the DAQ.

Learning from the 1rst DHCAL TB

"First experience with a detector embedded RoC with local memory in test beam"

Set-up:

- CERN PS T10 & T9: 0.4s spill every 48 or 33s (day/night cycles).
  - low part density (punch through π's)
- 4 cards of 4 HardRocs managed by 1 FPGA
- Running mode: single event with auto trig
  + BUSY logic & automatic RAMFULL recovery (⊃ BUSY signal)
- USB readout: LabView (R. Della Negra) + libDhcal (C. Jauffret)
  - asynchroneously RO of all cards ("LabView thread")
  - 2 commands:
    - polling on each card ("every ms")
    - readout order
- Data re-formated on PC for a fixed length (~ for "memory allocation")
  - Storage as such in binary files
    - dominated by 0's ⇒95% of reduction by std bzip2

Performances:

Bad:

- “modified set-up for electronic tests, modified for TB”
- last minute changes (comand reduction, RAMFULL clearing)

BUT working!!!

- Maximum rate ~20 Hz for a low volume of data
  (≤100Hz: single board with no data)
  - event for muons ⇒ dominated by noise
  - maximum volume/card:
    - 20 kbit × 4: 80 kBits @ 1 MHz ⇒ ~ 8 ms
  - Speed limited by the USB connection establishement ~16ms,
  - due partly to the the preparation of data (no pipelining)
    - USB link: ↗ 1 MB/s with one card
    - not fully understood...

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Data format & storage:

- Binary storage NEEDS some markup & redundancy in case of pbms
  - zero suppression → no fixed length...
- Consistency of Data:
  - number words in header**S** (all headers) & possibly version
    many versions for testing
  - End word ⇒ recovery possible
  - Eventually CRC ? ⇒ local/missing bits
  - Internal counters!!! (trigger numbers)
- Idem for all stage of data (DIF)/event (was missing here)

  ADDITIONAL: possibility to verify FW versions at all stages
  ⇒ ⊃ list of commands
- Exemple mixing of events:
  - asynch. readout of cards ⇒ event mixing (10% of total)
    - evt 1: card 2, 3, 1; evt2; card 2; evt 1: card 4; evt 2: card 4,3,2, ...
    - ⇒ recovery using a “trigger counter” on the cards

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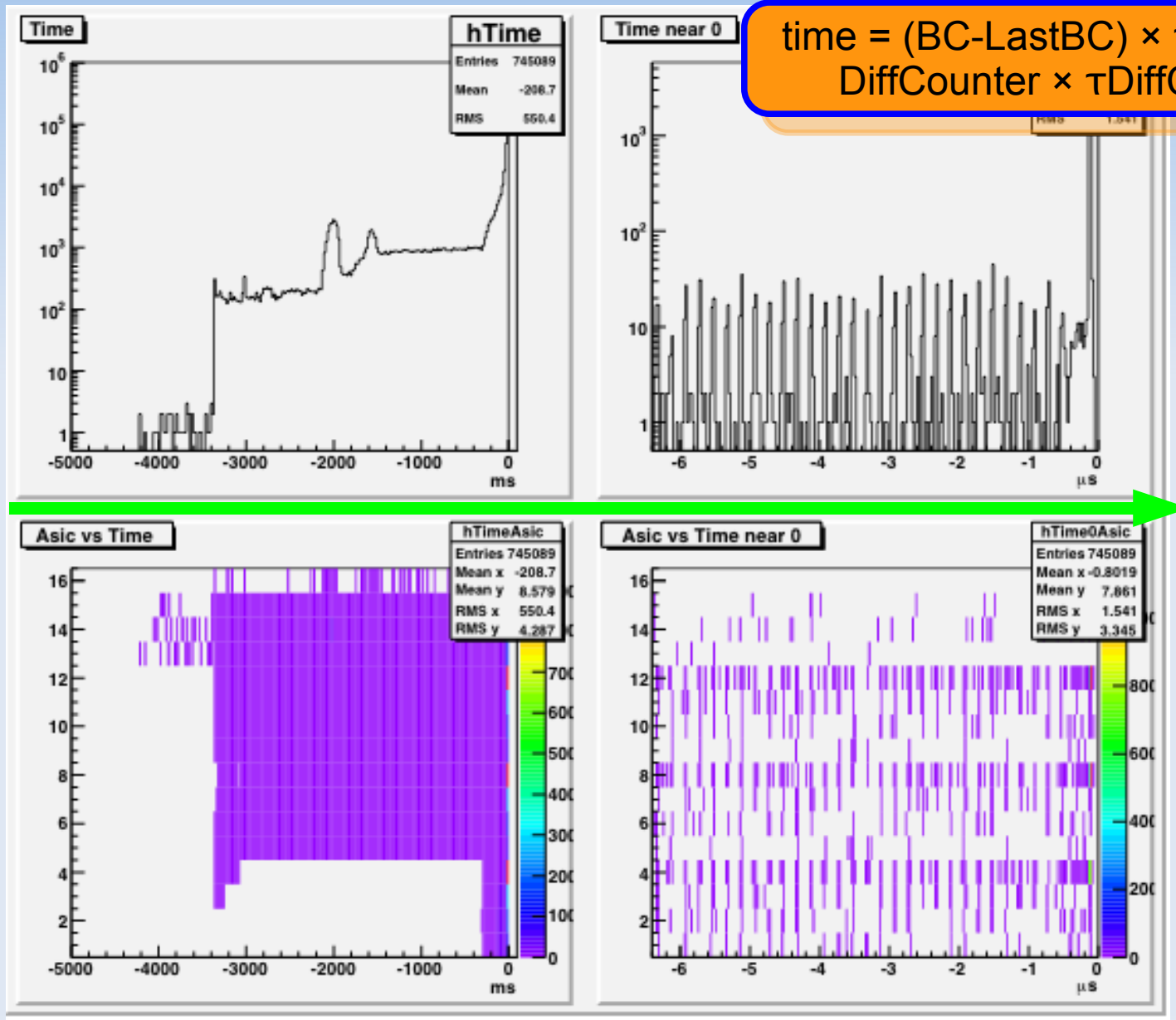
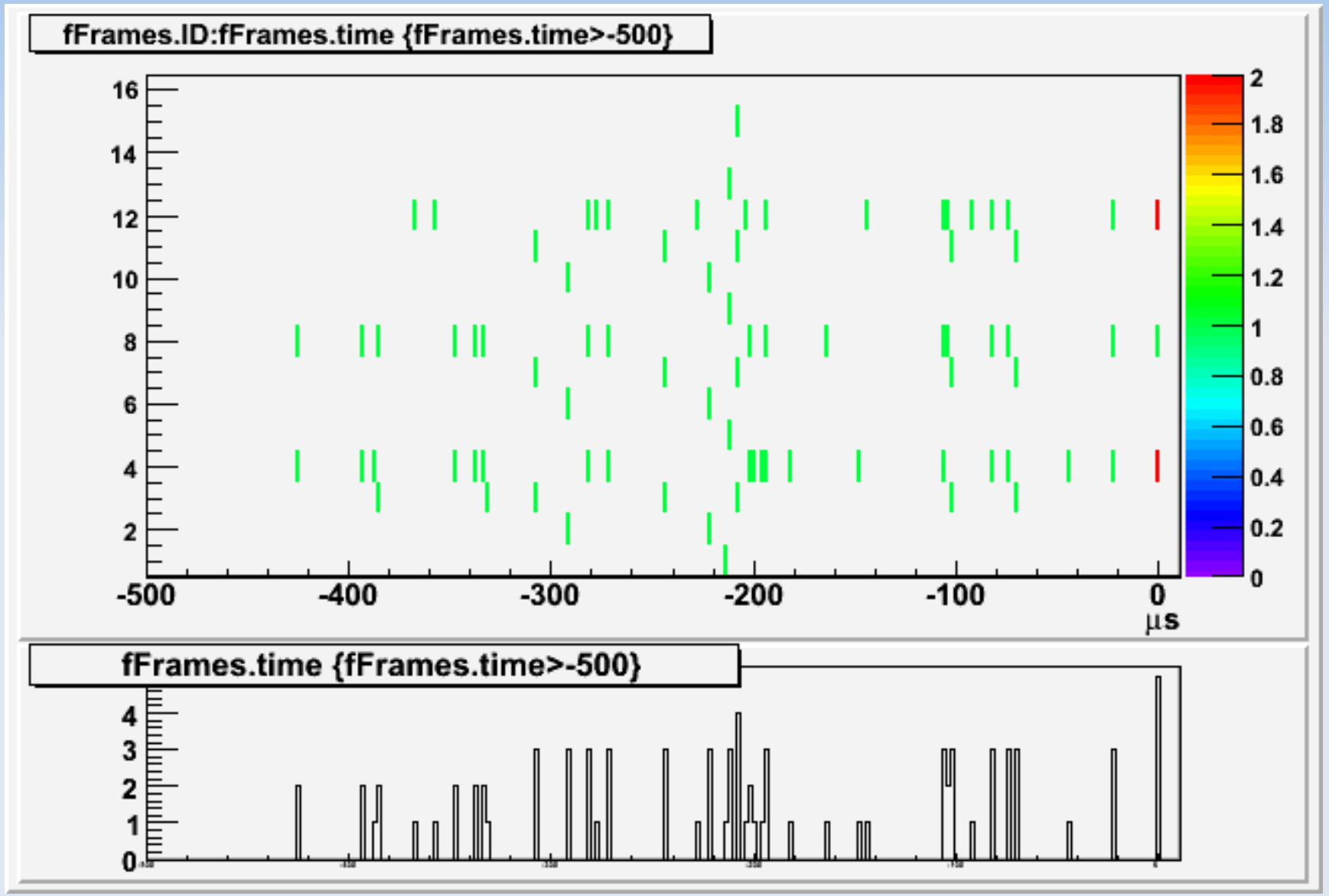
DHCAL single event + auto-trig

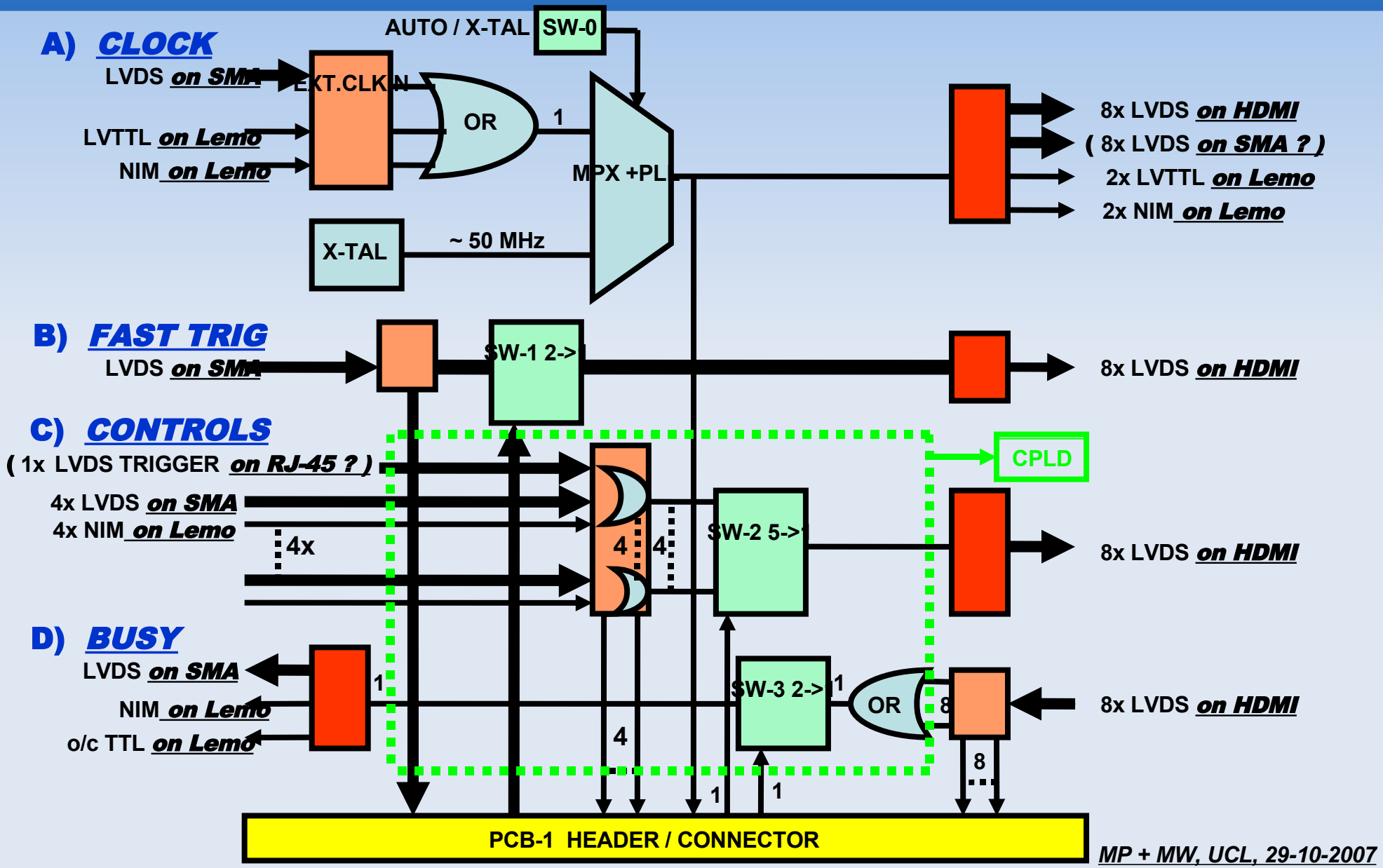


DHCAL single event + auto-trig



Back-up

Clock & Control Card [reminder]



DAQ2 DHCAL M³ Test Beam contingencies

- ASIC's in auto trig
- DHCAL Data rates in TB
  - Expected from 100 GeV π (J-C. Brient's note)
    - 5 ASIC's touched in average (max 18) / plane
    - All on the central DIF
  - 1 evt = 160bits
    - Readout time 1 ASIC @ 5Mb/s = 0.032ms
    - RO 1 plane ~ 0.16ms [6 kHz]
  - 1 full HR (128 events) = 20480 bits
    - Readout time 1 full HR @ 5Mb/s = 4ms
- see Remi's talk for ECAL
- TB rates: 10^4 (10^8 at FNAL ???) part/s during 10s/min (SPS mode).
- RPC limitation: ~100Hz/cm²
  µMegas: basically not limited...