Clock & Control Card Status

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C&C Logic and Interfaces (UPDATE)

CPLD (XCR3128XL-7) replacing many jumpers and switch logic
RS232 interface as a means of control
Many buffers, 0Ω resistors and solder links for better signal integrity, isolation and configuration

Signal Inputs:

- CLOCK
  - 1x LVDS (SMA DC)
  - 1x LVTTL DC (Lemo)
  - 1x NIM/TTL (Lemo) AC/DC
- ASYNC
  - LVDS (SMA) DC
  - ECL (2 pin LEMO) AC
- Controls (SYNCCMD, BUSY etc. + more)
  - 4x LVDS (SMA)
  - 4x NIM/TTL (Lemo) AC/DC

Signal Outputs:

- CLOCK
  - 2x LVTTL on Lemo
  - 2x NIM on Lemo
  - 2x LVDS on SMA
  - 8x LVDS on DIL Header
- TRAINSYNC
  - LVTTL on Lemo
- GEN (was Busy)
  - LVDS on SMA
  - NIM on Lemo
  - OC-TTL on Lemo
- Spare (DATA_D2L)
  - LVTTL on Lemo

HDMI I/O: x8

- LVDS AC/DC

OUT:

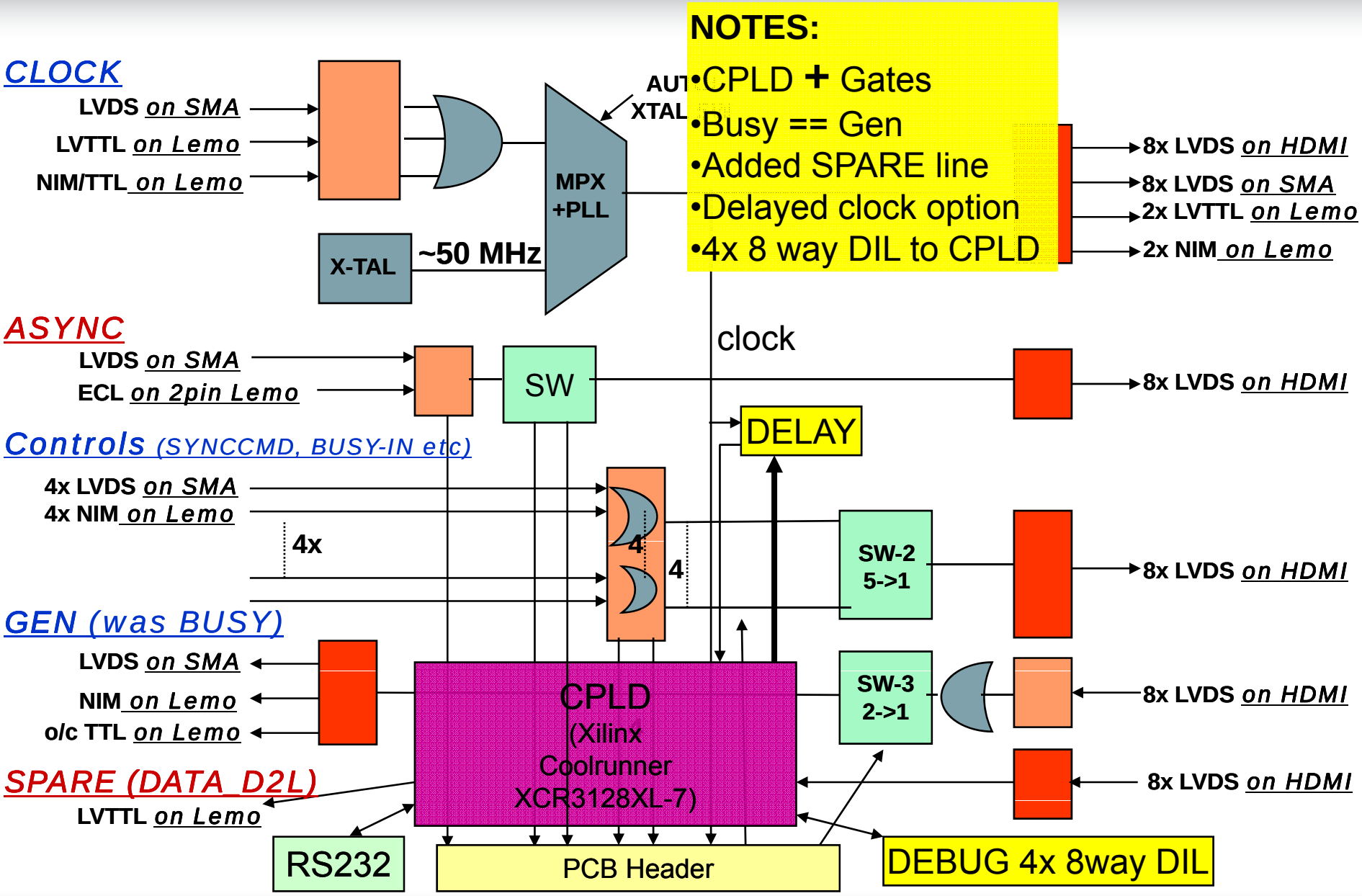
- CLOCK
- ASYNC
- TRAINSYNC

IN:

- GEN (was BUSY)
- SPARE(DATA_D2L)

***NO RJ45**

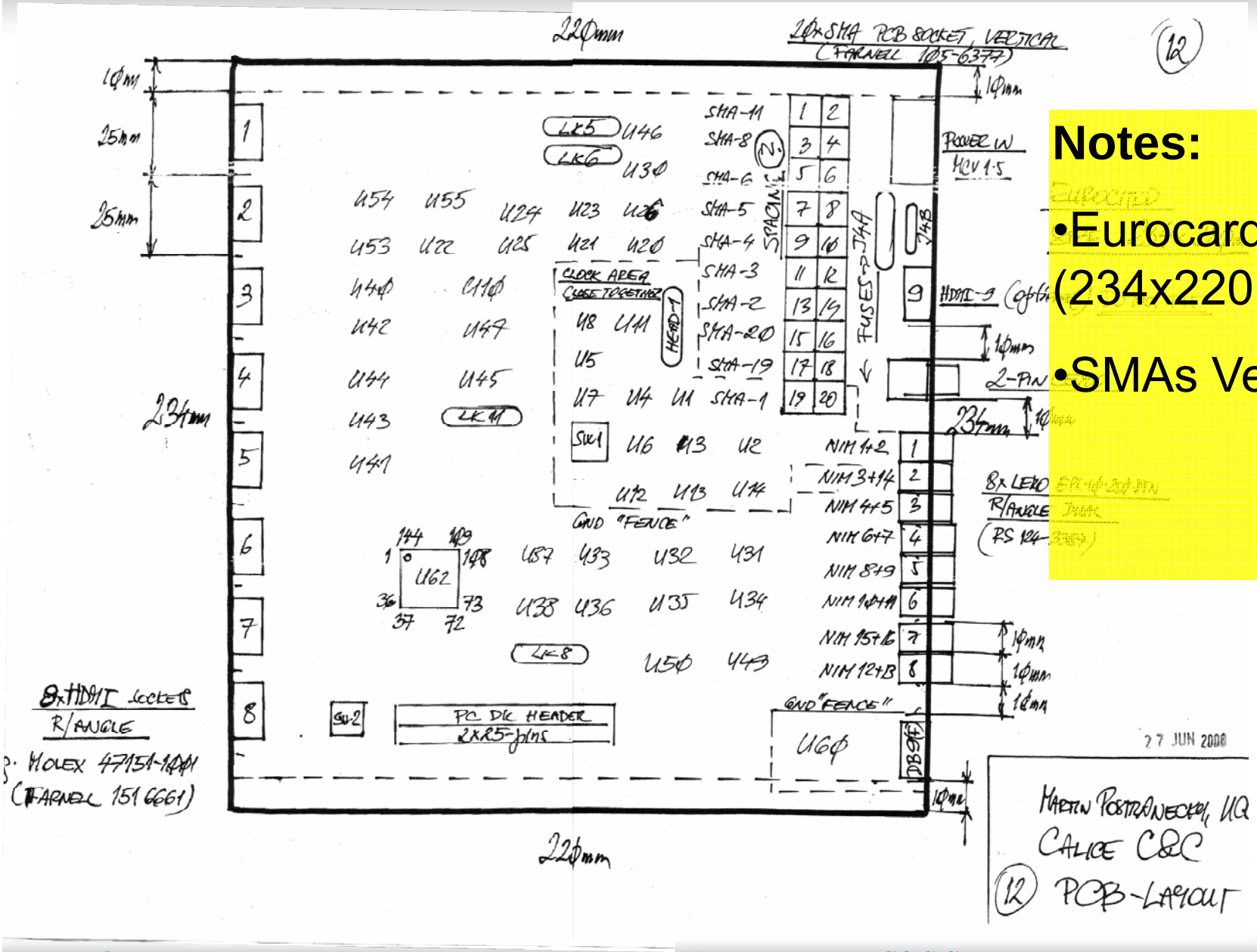
Overview Schematic



Some Hardware Details

- Clock:
  - PLL/MUX - *ICS581-02*
    - +/-150 ps jitter
    - 45min/55max Duty Cycle
    - Failover if external clock missing for 3 cycles.
  - Local Osc. 100 MHz/2 = 50% duty-cycle 50MHz
- CPLD: *Xilinx CoolRunner XPLA3 XCR3128XL-7*
  - 3.3V, low power
  - 128 macrocells with 3,000 usable gates
  - 5.5ns pin-to-pin logic delays
- Extra IO via IDC header.
- Single PCB with connectors at the edge (big!)
- Separate PSU
- Clock Delay Option to CPLD – 64x0.5ns?
  - For *signal* deskew (CLOCK unaffected)

Rough Board Layout



Status/Schedule UPDATE

- Schematic **DONE**.
  - Double checked
  - But getting mods (delay)
- Layout
  - Initial: in-progress, may be done now.
  - Final: mid-Aug (was mid-June)
- Manufacture
  - Mid-Sept (was July/Aug)