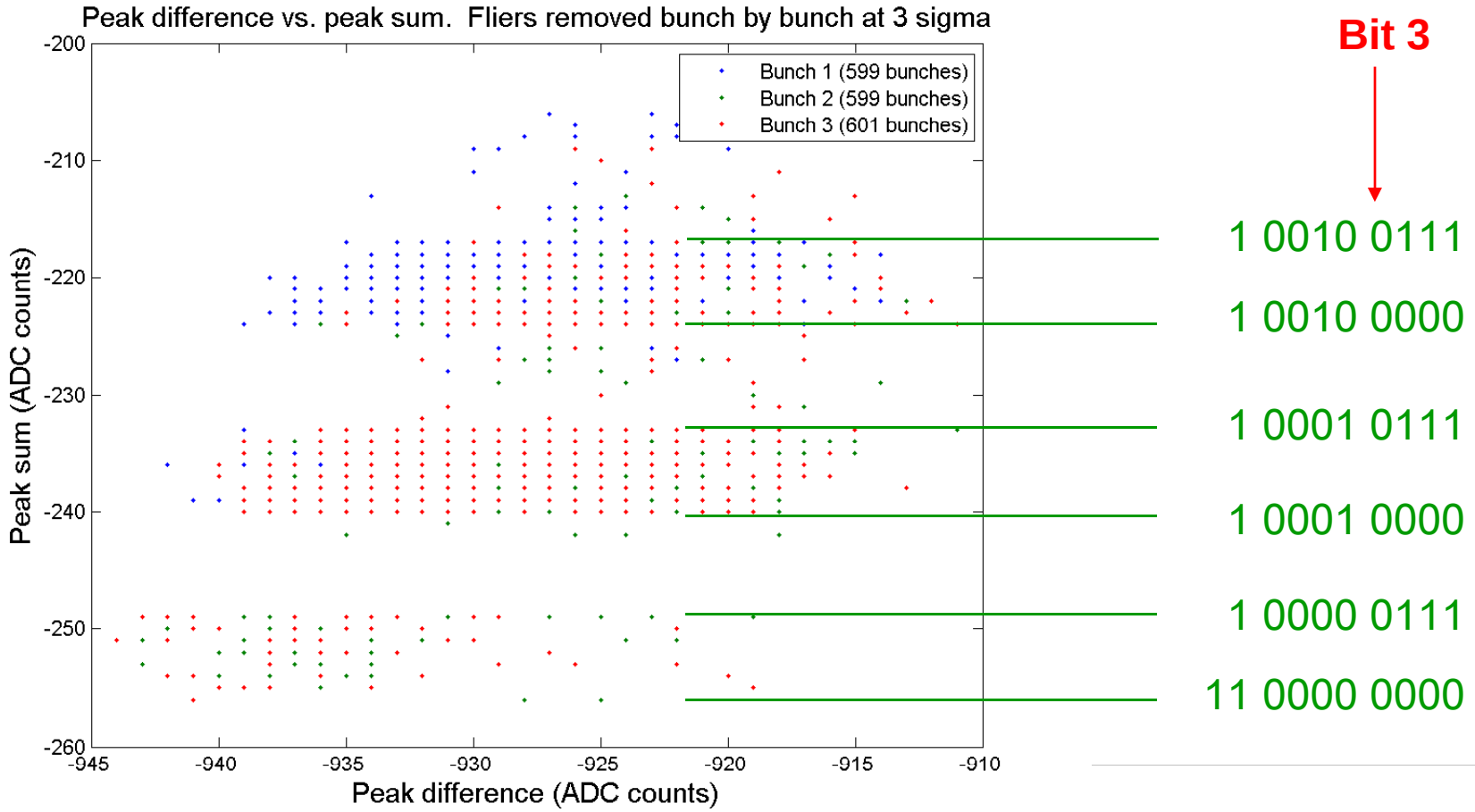
Sum signal banding

- From last week:



Modifications

Testbench

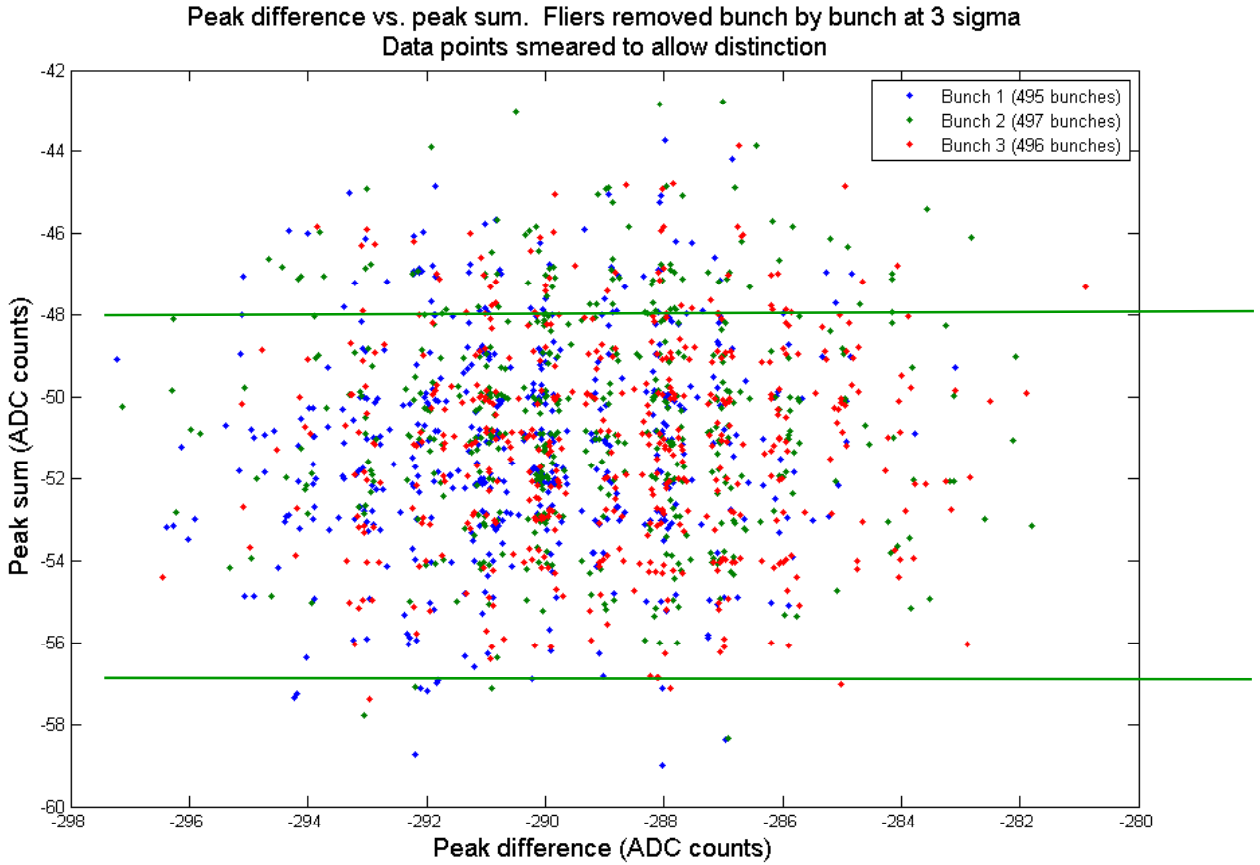
- Unsuitable splitters causing poor ring clock pulse
  - Giving timing glitches on bunch output
  - Now using two 2.16MHz signals from ATF racks
- Board 3 now outputs on ring clock cycle selected by trigger

FONT4 firmware

- Tightened timing constraint on 357MHz by 40ps
- Enabled ‘timing driven mapping’
- Ran high effort place and route
- Timing slack now 56ps

Testbench: sum signal banding

- If bit 3 tended toward **zero**, would expect empty band in the region bounded below



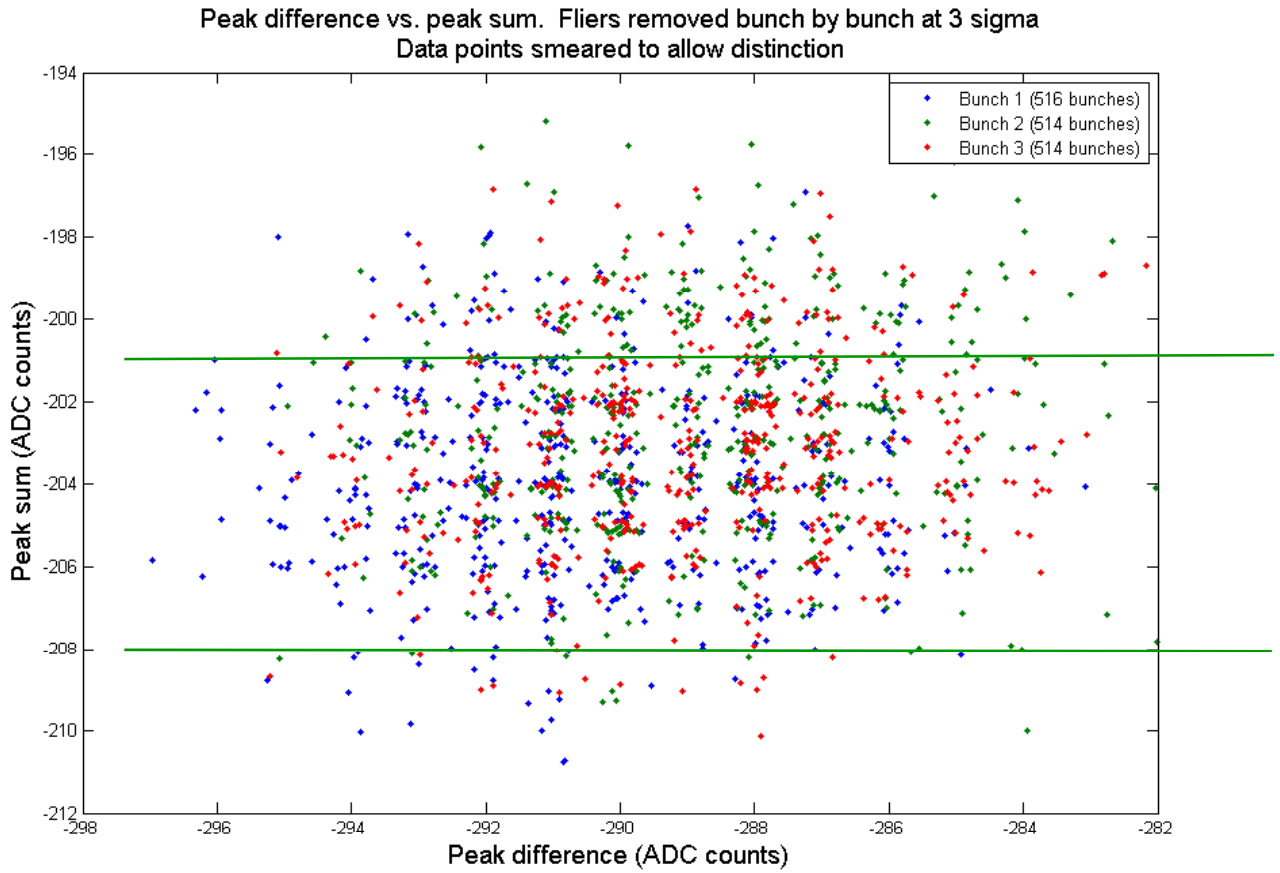
Bit 3

1 1101 0000

1 1100 0111

Testbench: sum signal banding cont.

- If bit 3 tended toward **one**, would expect empty band in the region bounded below



Bit 3

1 0011 0111

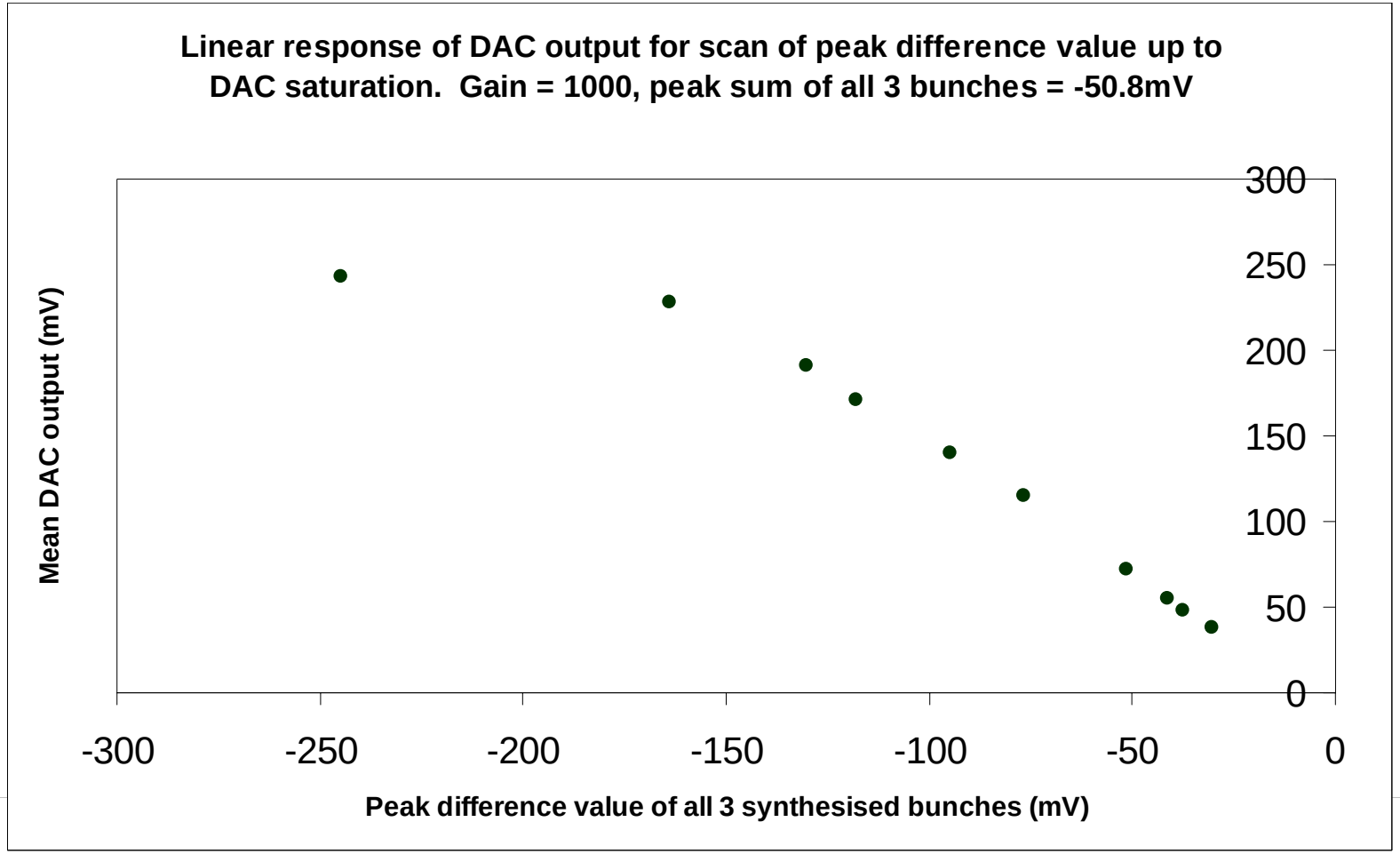
1 0011 0000

DAC feedback signal response

- Varied sum and difference signals from testbench using combinations of attenuators
- Tested CN firmware with good timing slack
- Measured resulting peak sum/difference using scope
- Averaged DAC output using scope
- DAC output very stable

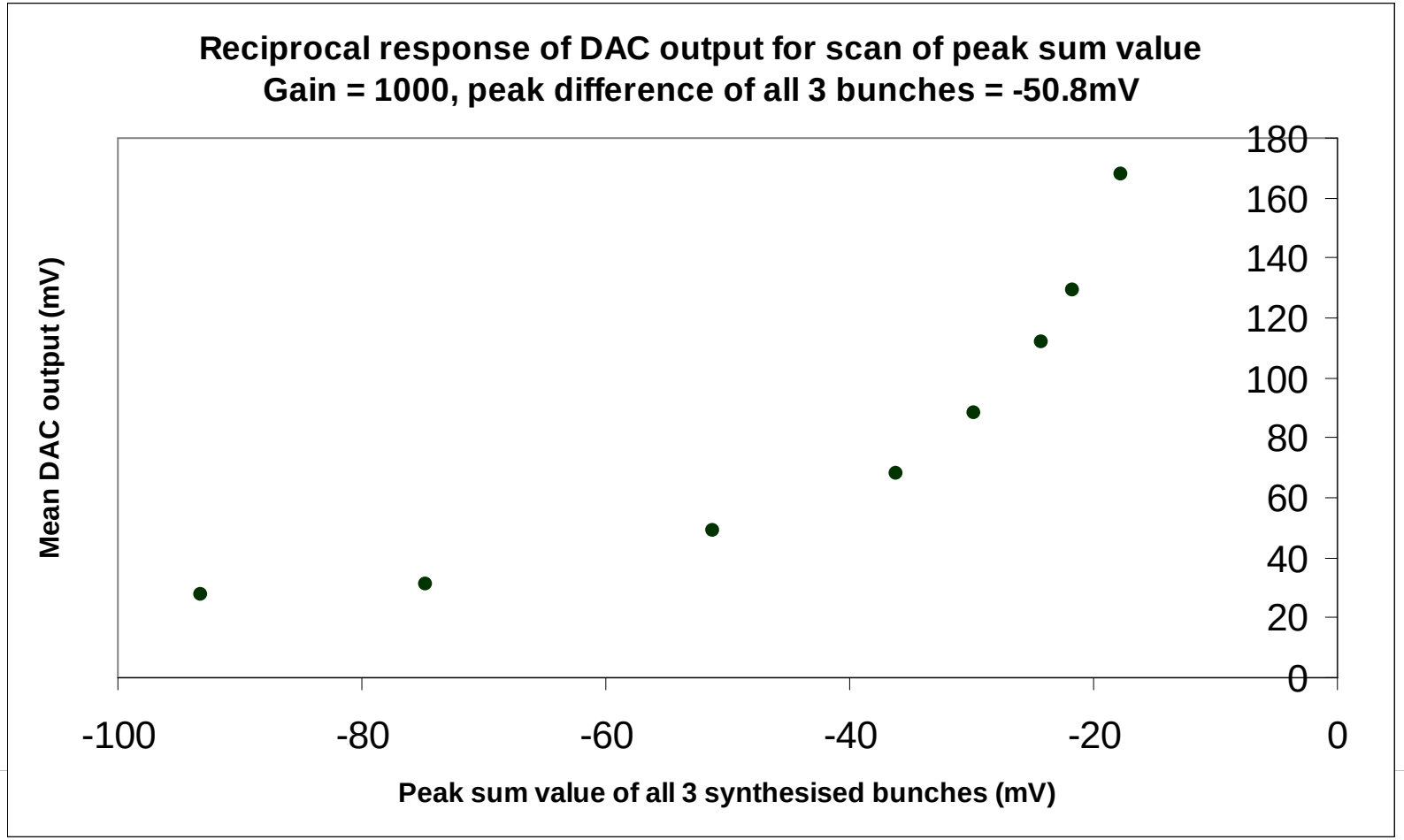
Testbench: DAC response difference scan

- Feedback signal varies linearly with peak difference



Testbench: DAC response sum scan

- Feedback signal varies reciprocally with peak sum



Additional: Oxford difference scan

- Scan over difference using square pulse also shows a drop off in DAC output before reaching full scale