ATF2 digital feedback board

- 9 channel board with replaceable daughter board (RS232 etc.)
  - Board will log data from 3 BPMs
  - 3 channels per BPM: both x and y difference along with one sum
  - Each channel has a 14-bit ADC (13 bits used)
  - ADCs to be clocked at 357 MHz
  - Single Virtex 5 FPGA
  - Control and DAQ via RS232

- RS232 protocol
  - RS232 transmits 8-bit bytes
  - MSB is reserved: 0 indicates a command or a frame, 1 indicates data
  - (Compatible with eventual XON/XOFF software flow control if required)
  - Each 13-bit ADC sample split over 2 bytes

ATF2 digital feedback board

- Data acquisition - firmware
  - As before, trigger selects ring clock cycle containing pulse
  - Each channel is sampled for entire ring clock cycle at 2.8ns intervals
  - (It will be possible to specify a subsection of the cycle to sample over)
  - Sampled data then framed and transmitted over RS232 at 38k baud
  - Position of bunches initially set by hand (eventually auto-detected)
  - Bunch samples framed and transmitted
  - All current operational settings are framed and transmitted
  - Expect this to take approx. 0.65 seconds in total (c.f. 3/2 Hz single bunch mode)

ATF2 digital feedback board

- Data acquisition - software
  - GUI interface will display all 9 channels in real time
  - Bunch samples will be used to display real time normalised positions
  - Current control settings will be displayed pulse-by-pulse
  - Data will be logged as ASCII and time-stamped
  - Considering ‘sub-windowed’ approach to display
  - C++ / QT?

  - GUI development can start now
  - Use software to generate simulated RS232 stream

ATF2 digital feedback board

- Board control - firmware
  - UART will pass received bytes to an interpreter module
  - Commands specify one of several control registers
  - Subsequent data are then written to specified control register
  - All control logic on slow clock domain (40 MHz oscillator?)
  - Control register contents exposed to 357 MHz domain via metastability guards
  - These settings are then used during operation
  - Interpreter will have RAM_LOAD state, where subsequent data are written to the charge normalisation look-up table RAM
  - Again, this is on the slow clock domain
  - Allows gain to be set without reprogramming the FPGA

ATF2 digital feedback board

- Board control - software
  - GUI will be used to send commands/data over RS232 to FPGA
  - Software will calculate look-up table contents for a given gain
  - It will be possible to fill the lookup table with values corresponding to no charge normalisation

ATF2 digital feedback board

- Clock synchronisation
  - ADC clock phases will be adjustable to allow sampling time optimisation
  - Initially, ODELAY output delays onboard the FPGA will be used
  - Control logic to reset ODELAYs each time they're changed to guard against glitching
  - Initially changed by hand, eventually auto-optimising
  - Possible to replace ODELAY logic with control logic for RF phase shifters should clock jitter become a problem
  - RF phase shifters would be added to daughter board
  - Relative phase of ADC clocks and FPGA clock will be continuously monitored
  - May be adjusted to ensure sampling window is correct