

Omega

ECAL Electronics Status

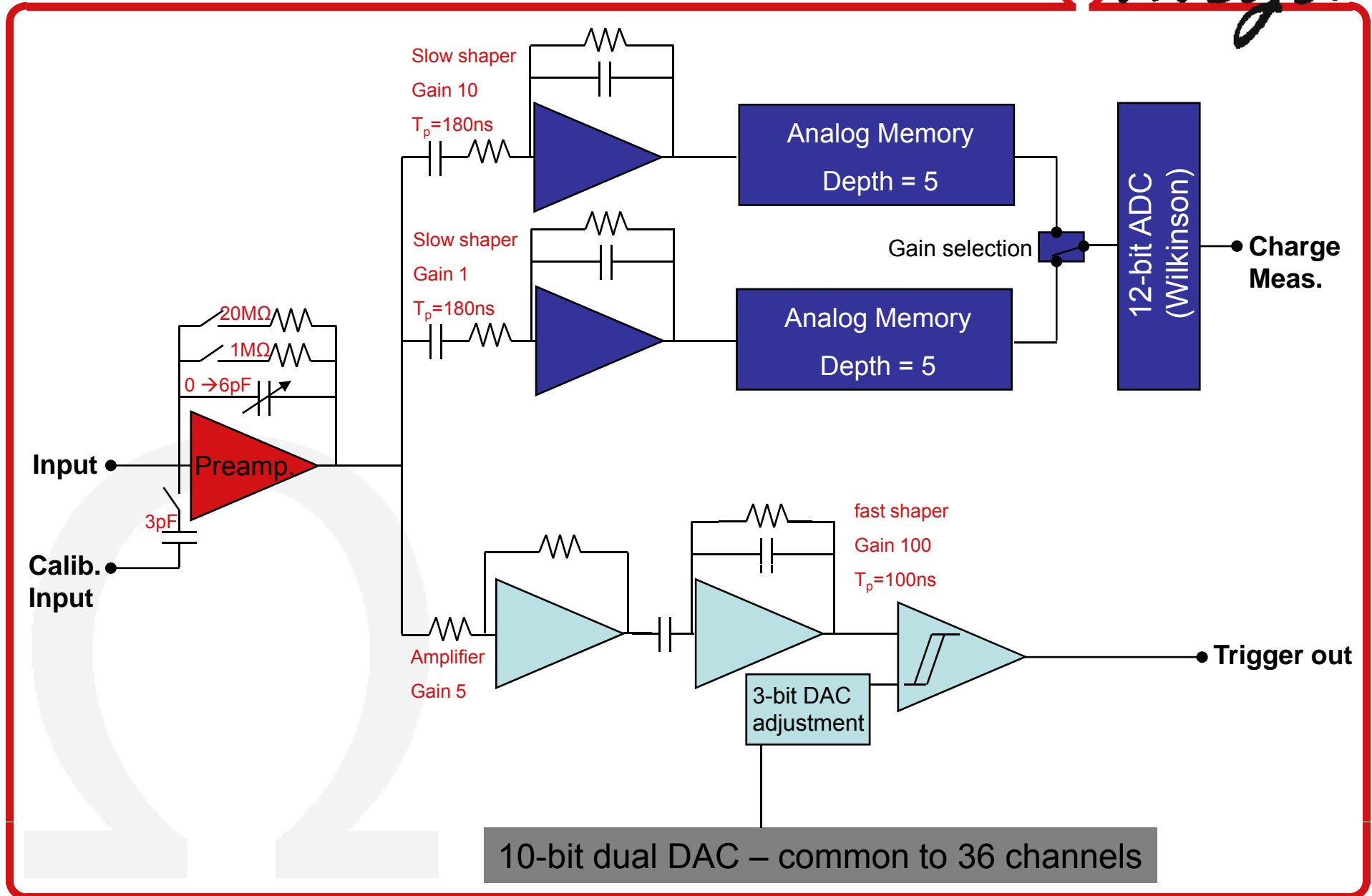
1 December, 2008

Orsay MicroElectronics Group Associated

ASIC design SKIROC 2



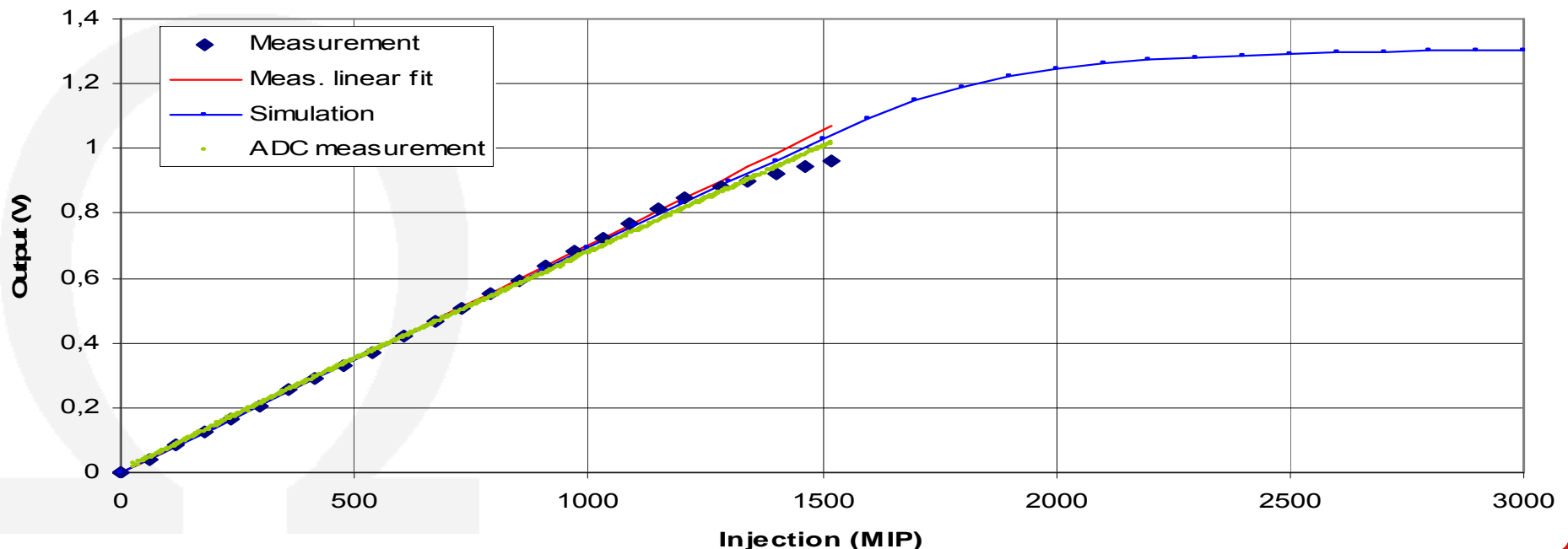
SKIROC1 One channel block scheme



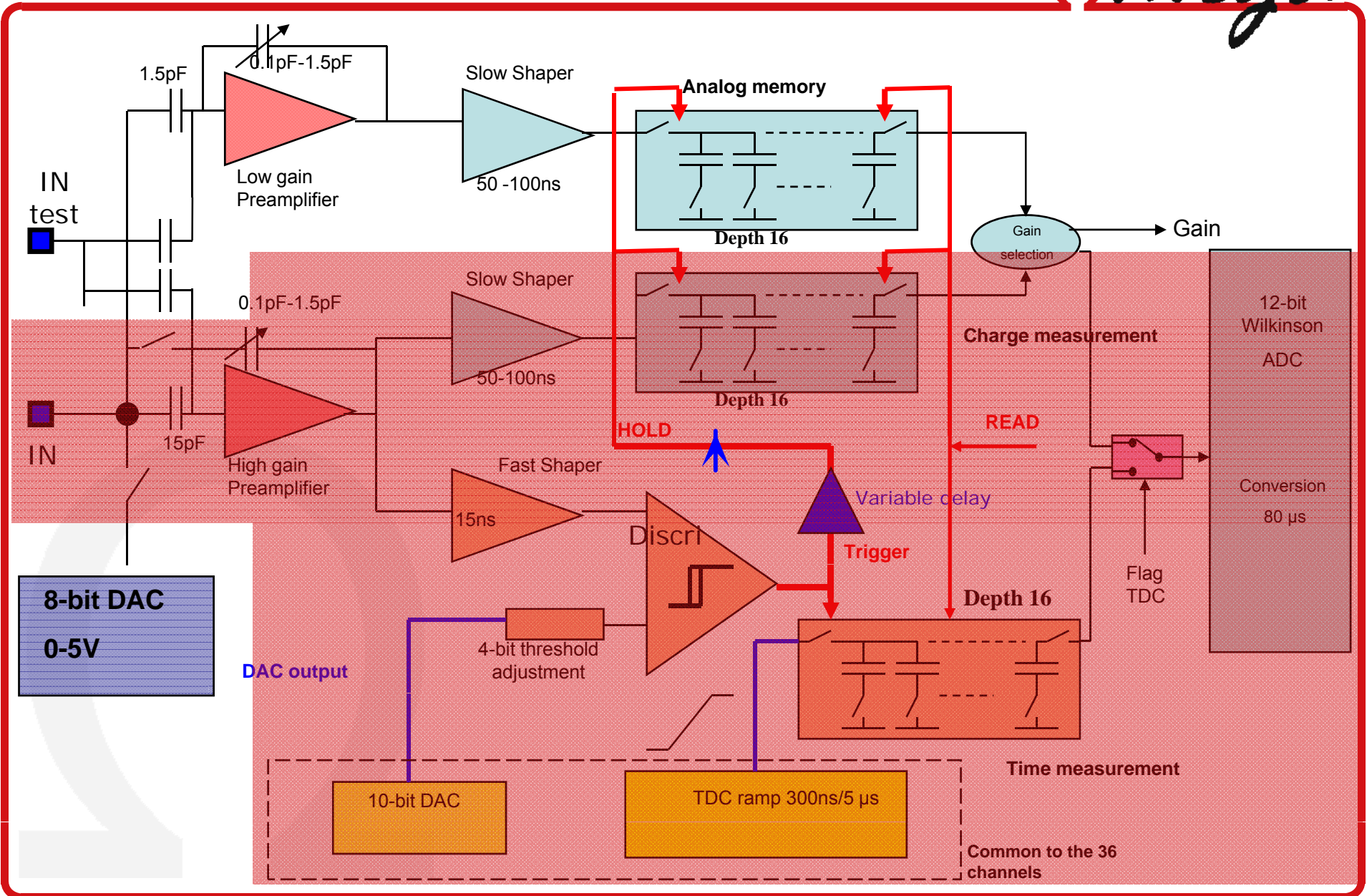
SKIROC 1 design limits

- Most critical issue : Too much dynamic range in the charge preamplifier
 - Max input signal : 2000 MIP
 - Noise floor : 0.15 MIP
- Preamplifier gain too small
- Huge gain in the trigger path to be able to trig on $\frac{1}{2}$ MIP

SKIROC linearity results



SPIROC used in SKIROC mode



- Dynamic range :
 - 500 MIP/cell → same as physics prototype
- Number of channels :
 - 36 instead of 64

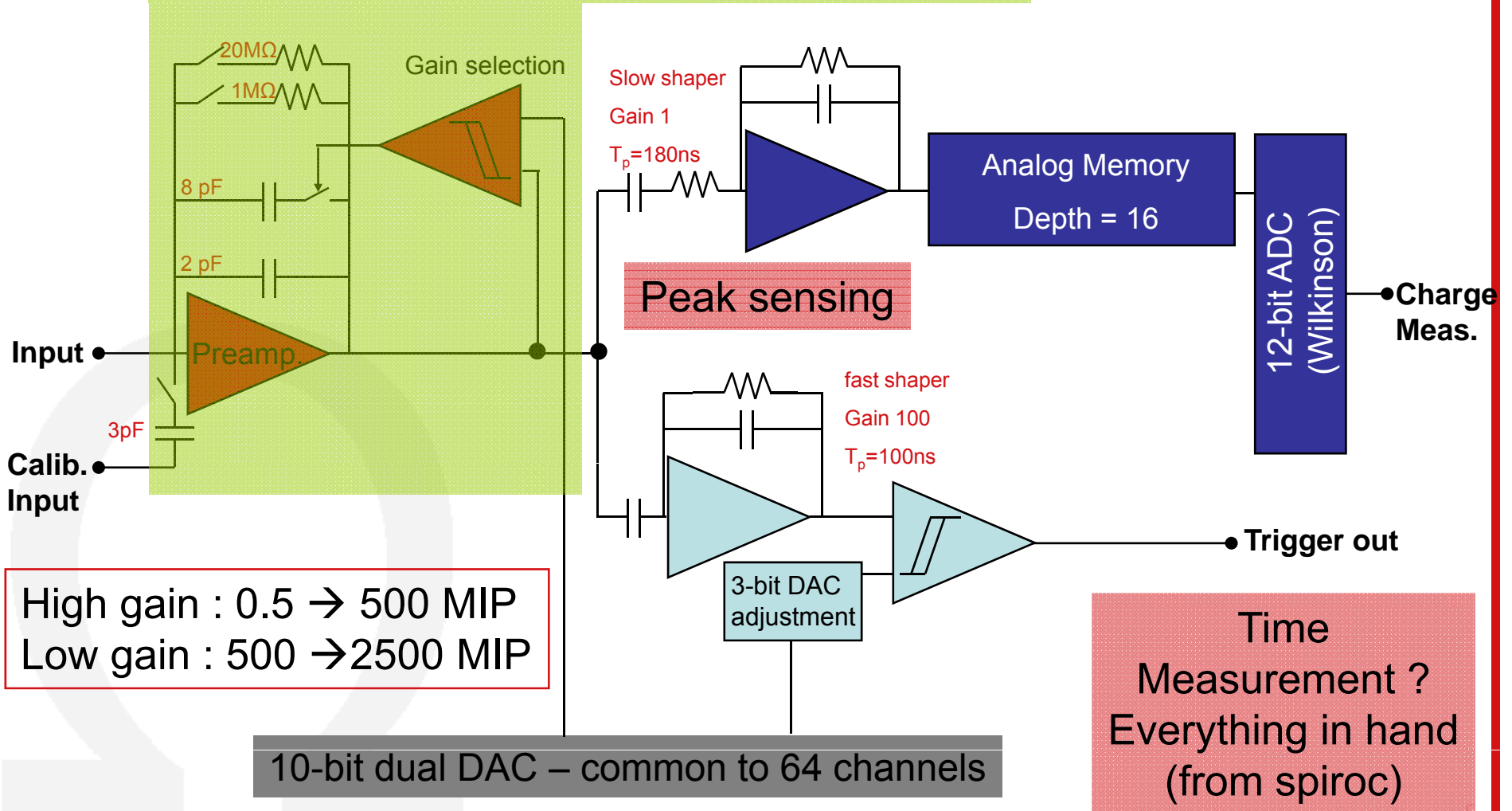


- 64 channels to read out new 256 pads wafers with 4 chips
 - This is a critical PCB requirement
 - This will make SKIROC2 the biggest chip of the ROC family
 - 50-60 mm²
- Capability to operate in ILC mode and in test beam
 - This is a physics requirement to take data with EUDET module
 - Calculation of data rates to be validated
- High dynamic range from 0.1 to 2500 MIP
- (Eventually) time measurement to tag events in test beam (not useful in ILC mode)

SKIROC 2 block scheme proposal



We already have that kind of structure on the shelf



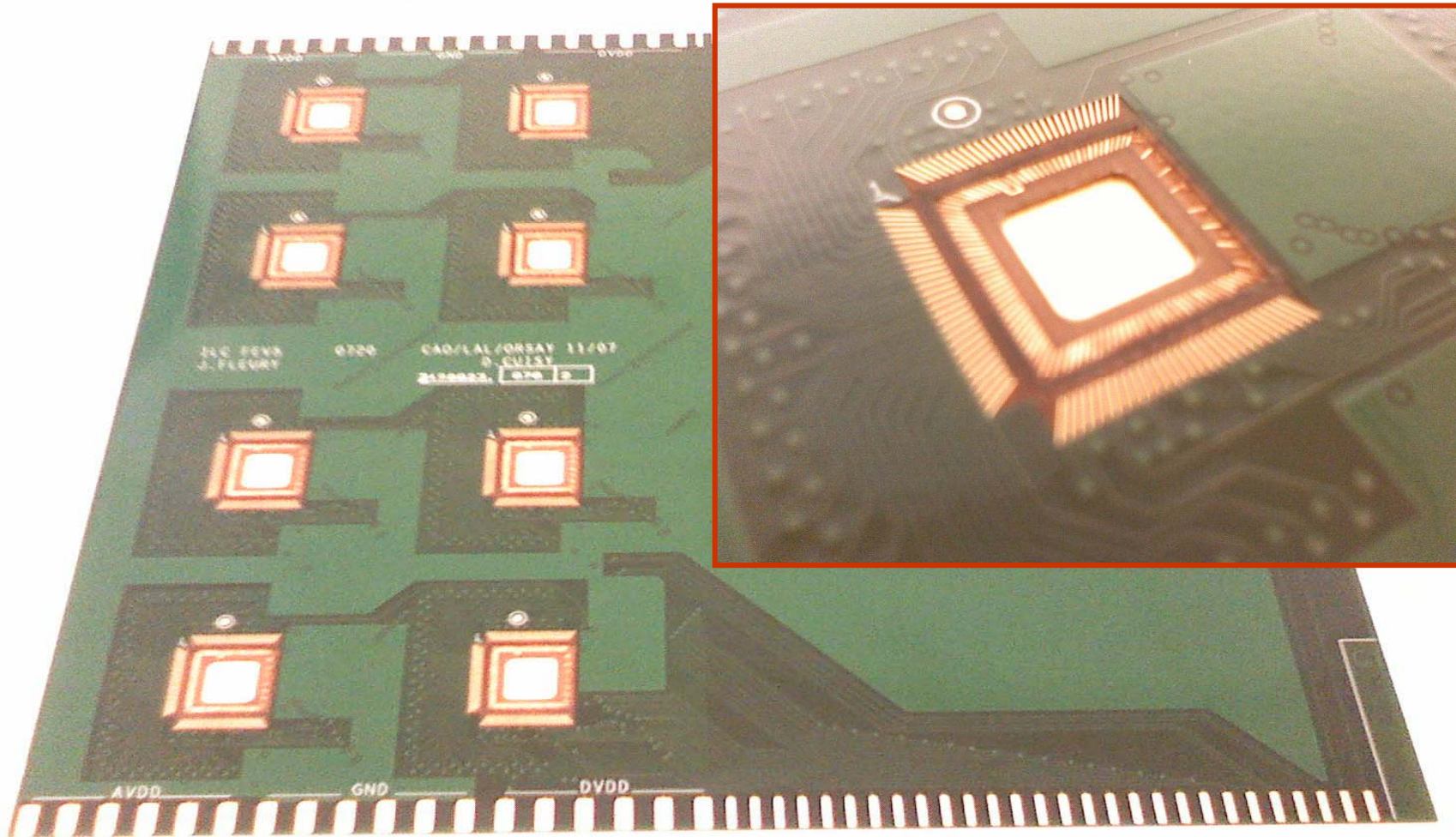
- Skiroc 2 expected to be sent in fab in March'09
 - Sharing of the HARDROC2 and SPIROC2 production
 - If SKIROC 2 is validated → production in hand for EUDET module
 - Cheaper than an engineering run for prototyping due to big silicon area (60mm² ie ~60k€)
- Next PCB prototype will use SPIROC2 with Hamamatsu wafers
 - Validation of all electronics and assembling process
 - missing : dynamic range (500MIP/2500MIP), granularity
 - PCB in hand before the end of the year ?

PCB design FEV 5 presentation



FEV5 : design

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Chip Embedding + PCB Pile-up

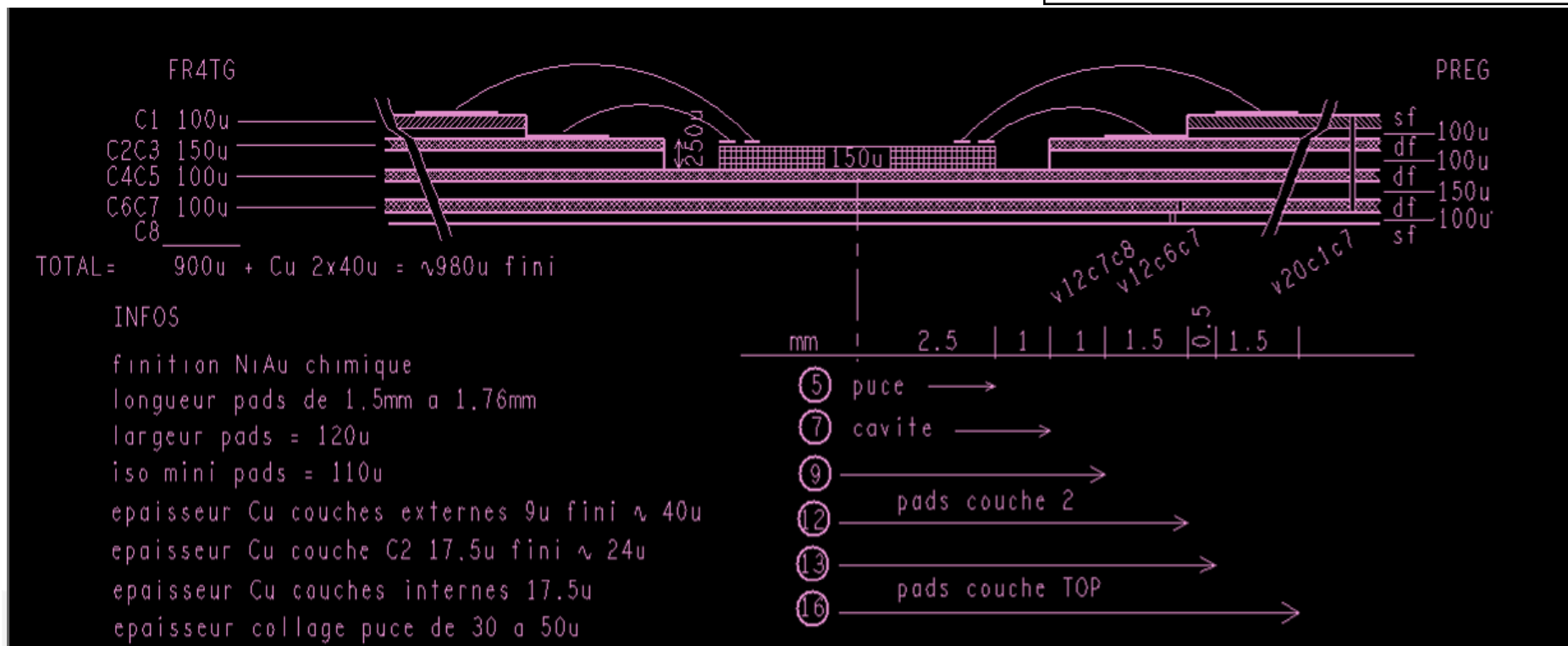


Pile-up

TOP	GND+routing
C2	AVDD+routing
C3	AVDD+DVDD
C4	GND + horizontal routing
C5	AVDD+ vertical routing
C6	GND+pads routing
C7	GND (pads shielding)
BOT	PADS

3 drilling sequences :

- Laser C7-C8 120 μ filled
- Laser C6-C7 120 μ
- Mechanical C1-C7



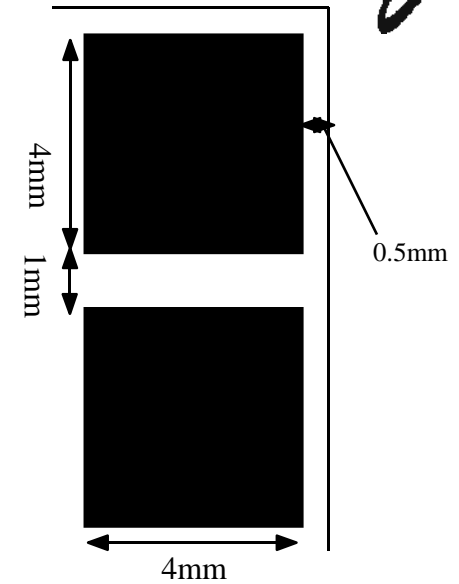
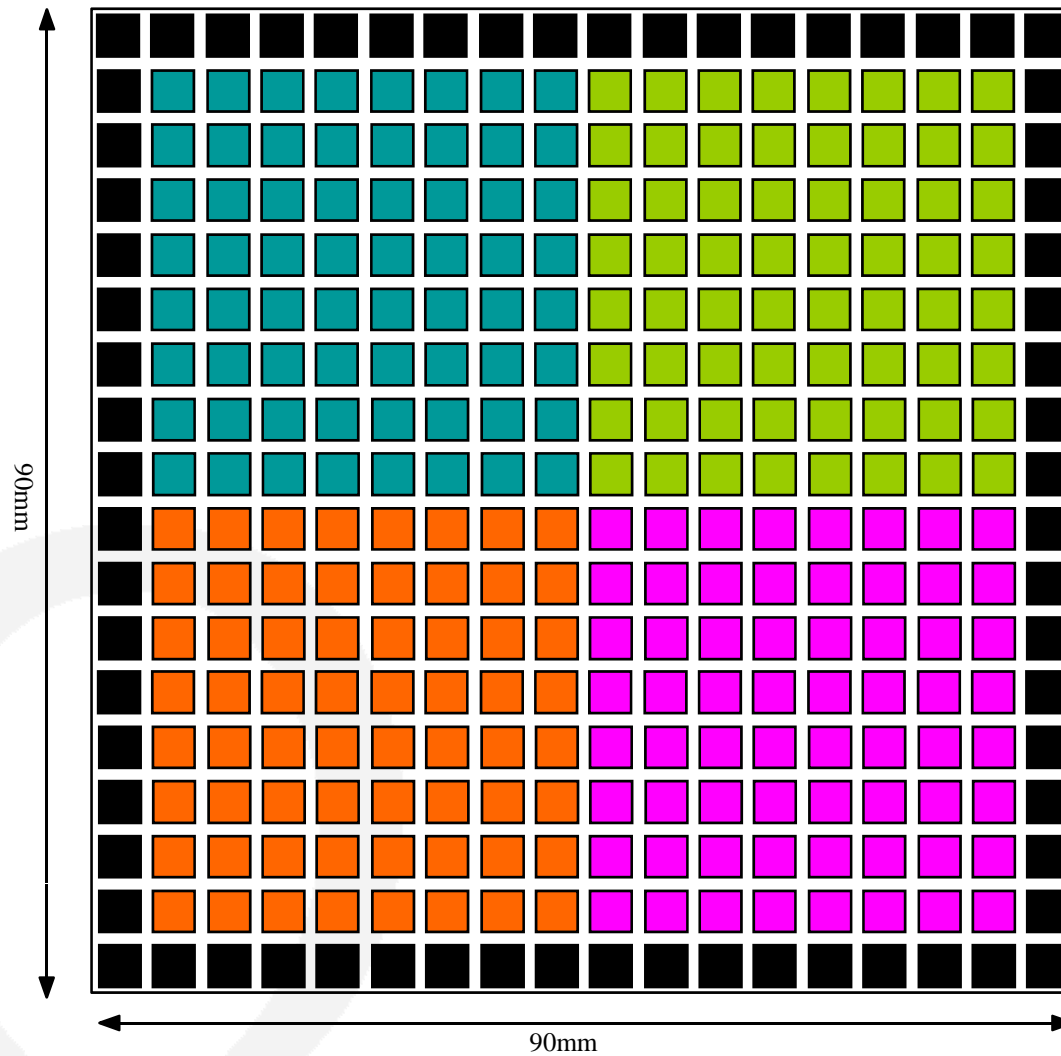
Issues : Layer 2 not bondable

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Wafer : channel equipped

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-  Chip 1
-  Chip 2
-  Chip 3
-  Chip 4
-  NC

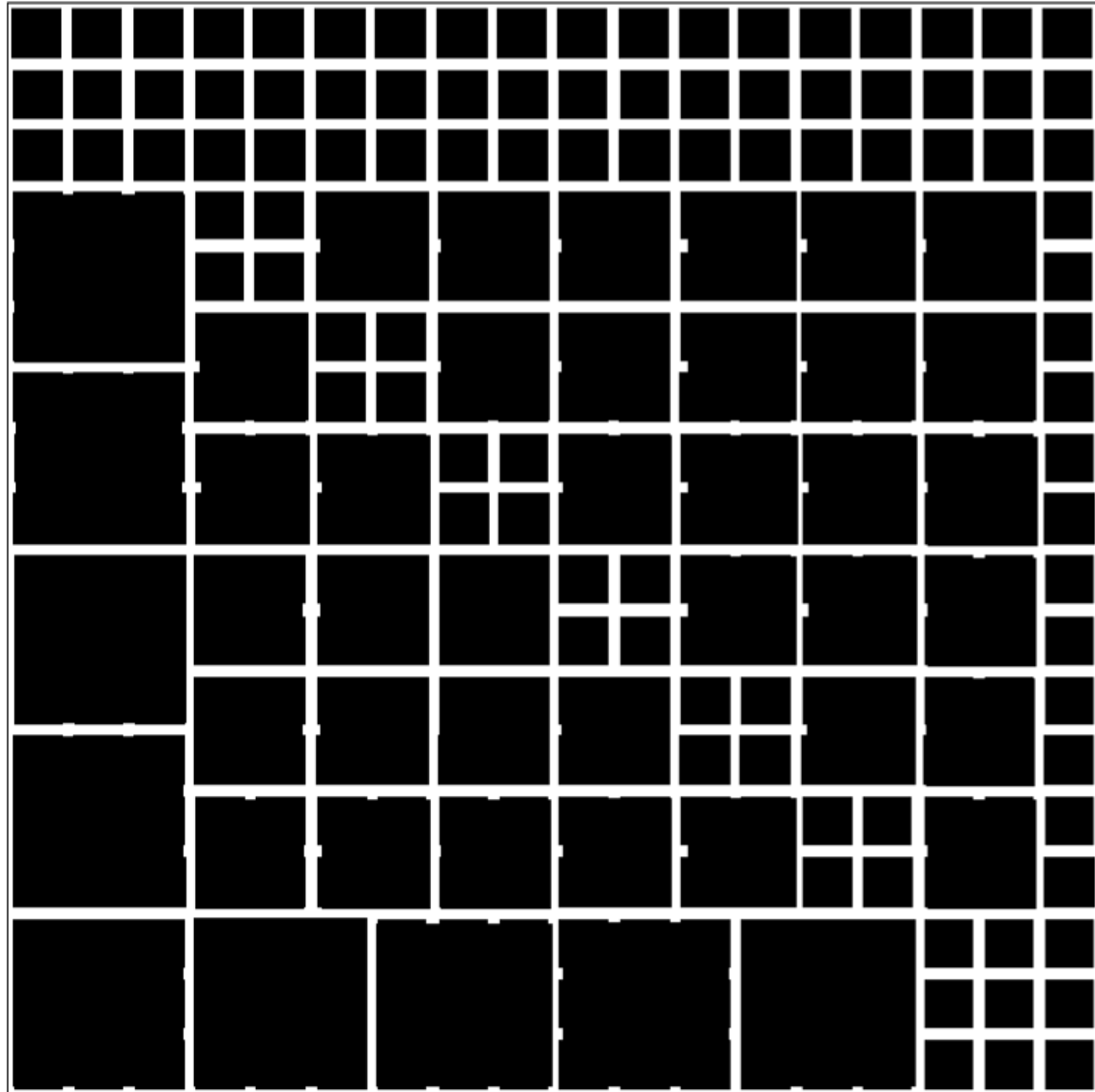
- First EUDET compliant PCB, using SPIROC2 in SKIROC mode.
- several pads merged for each electronics input
- Halfway from expected granularity and physics prototype granularity



FEV7 wafer footprint



144 Channels
Will be used for Wafer charact.
Need SPIROC2 validation



- PCB design
 - FEV5 engineering done
 - NOT SO EASY TO BUILD → still not validated
 - Opportunity to have 256 ch. Wafers ? (5.5mm pads)
 - For FEV8 design
 - To be available in Spring 09
 - FEV7 design using hamamatsu Wafer and Spiroc 2 in 2008
- Front-end ASIC design
 - Skiroc2 planned for march 09
 - All test with Spiroc2 before then, when validated