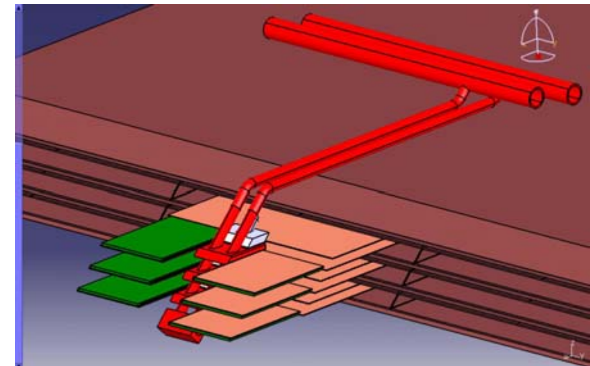
SLAB COOLING

- *DEMONSTRATOR*
- *EUDET*
- *CALICE*



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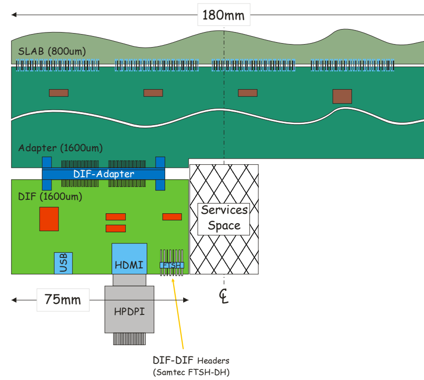
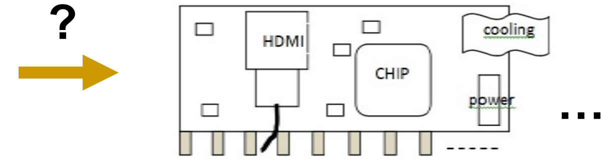
SLAB COOLING – CONSTRAINTS

Calorimeter for ILC

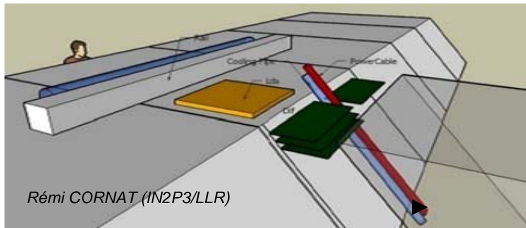
Mechanical constraints on ECAL electronics:



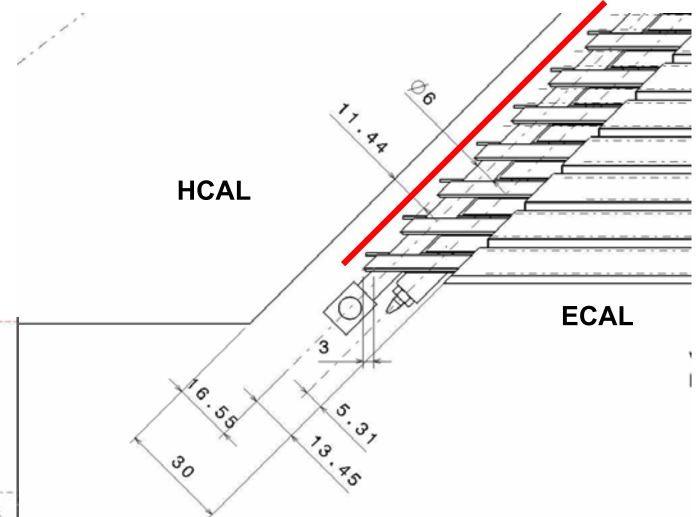
?



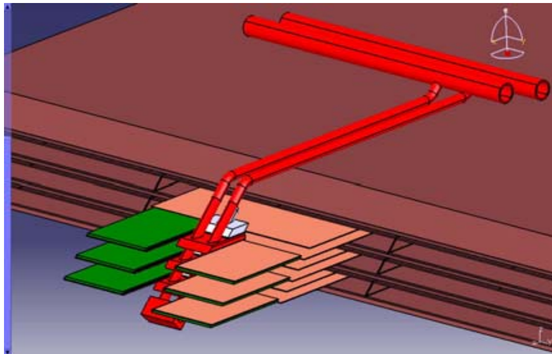
DIF is part of last ASU of the SLAB
Minimum Space for cooling necessary



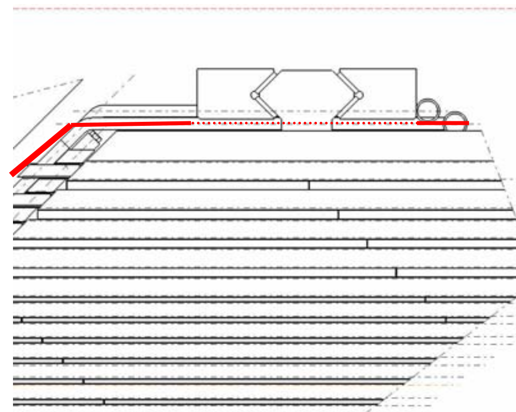
Place for cabling : DAQ + HV + GND
Service space between cooling and HCAL >1cm



Space for HV and GND



Demonstrator: cooling and copper drain extremities



Passing trhough the rail: OK

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SLAB COOLING - DEMONSTRATOR

Calorimeter for ILC

DEMONSTRATOR design

Hot Point = FPGA power : 200mW to 2 W

Nominal : 275 mW

Maxi : 1 W

Hot Points (Σpower = 0.2 W to 1 or 2 W)

868 mm

124

- 6 ASU with only thermal sensors
- 1 ASU with hot points *(LAL)*

(location to be confirmed for simulations. Patrick?)

40mm 55mm

AdapV1 (0.8mm)

DIFv1 (73x55x1.6)???

non-component side

180mm

SLAB (800um)

(MANCHESTER/CAMBRIDGE)

30

65

25

8 *Hole for tie rod*

15

Demonstrator False DIF: *(LAL)* **50*55*1.6**

Cooling System *(LPSC)*

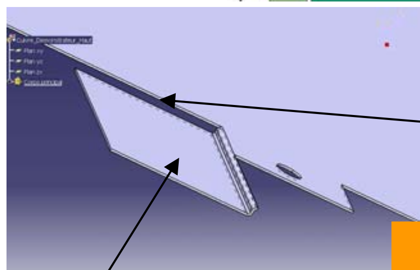
Next Version

Inter connexion *(no overlapping)*

(see DIF-ASU-ASU_Interconnect_2008 _07_10_EVO_Mech from Maurice & Bart)

The copper foil should recover this geometry In order to validate thermal simulations / tests

- The goal of thermal test is to build a slab as close as possible to numerical simulations in order to validate the slab's model (transfert coefficients) and check the ~*real thermal dissipation* , so, to verify the behaviour of the cooling system in EUDET's configuration; even if it's not the last version of design (PCB, Interface and DIF cards…)



FPGA cooling (direct contact by local copper deformation)

Limit of copper foil (for upper side + ~6mm for back side due to 45° angle)

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FPGA Cooling with the rest of slab

size of Interface and DIF cards to be confirmed – FPGA too

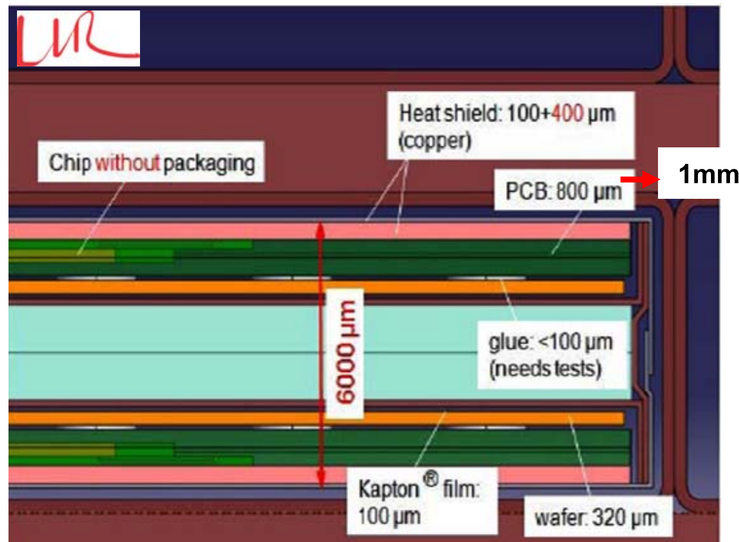
Design of copper foils

The expected heat shield thickness is 500 µm=100+400 µm:

⇨ Brazing of copper foils (T<300°C) to be validated

Heat shield : 100 (housing Al or CuBe?**)** + 300 or 400 µm Cu = 4 options for copper assembling to test:

- **Options 1**
  - 100µm housing Cu.. + **400 µm** Cu (without brazing – with holes) / **0.4 mm** considered for simulation. Thermal grease only in holes (1.8x1.8 cm² chips***400 µm** thick).
- **Options 2**
  - 100µm housing Cu.. + **400 µm** Cu + 0.05 (silver brazed) / **0.5 mm** considered for simulation. Thermal grease only in holes (1.8x1.8 cm² chips***400 µm** thick).
- **Options 3**
  - 100µm housing Cu.. + **300 µm** Cu + 0.05 (silver brazed) / **0.4 mm** considered for simulation. Thermal grease only in holes (1.8x1.8 cm² chips***300 µm** thick).
- **Options 4**
  - 100µm housing Cu.. + **400 µm** Cu (whithout brazing) / **0.4 mm** considered for simulation. No holes (1.8x1.8 cm²), chip no overlapping.



Simulations to be performed on the final option for demonstrator.

Actually done with 100µm housing Al + 300 µm Cu with holes and grease (0.4 mm considered for simulation)

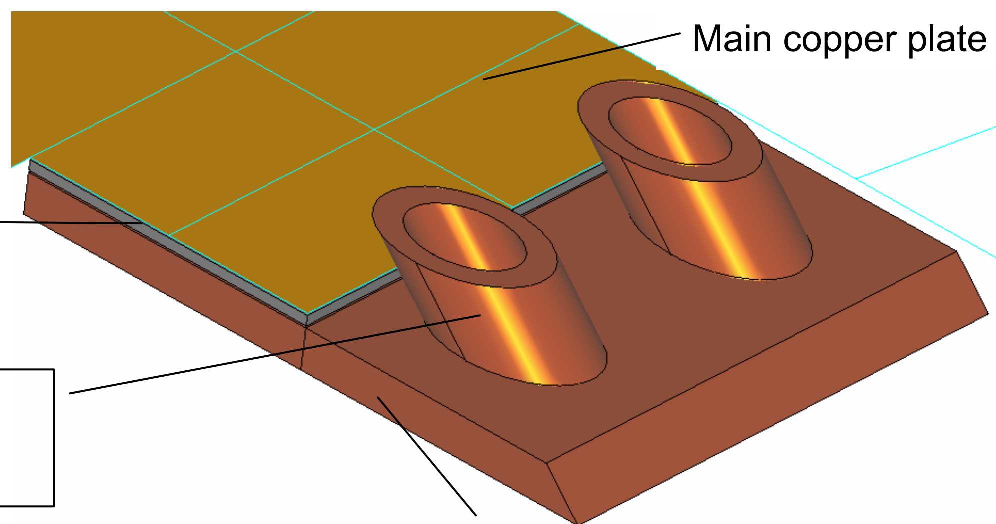
For simulation : the 100µm housing Cu do not cover the ADAPTER et DIF cards.

The copper drain is adapted / DIF card to be in contact with FPGA on DIF (« hot » Kapton for demonstrator)

SLAB COOLING - EUDET

Calorimeter for ILC

Boundary condition:



Thermal foam : **λ = 3 w/mK**

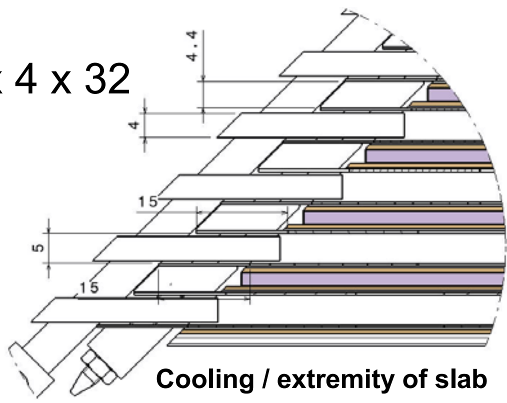
Convective flux into pipe with fluid at 20°c (h = 3445 W/m².K)

Cold copper bloc inserted between 2 copper plate of 1 slab

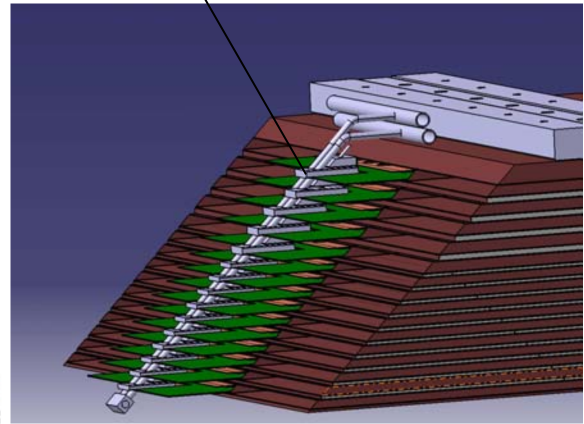
Load (for 1 half slab = 1 side)
Channel heat flux : 25 µW
Number of channel / chip : 64 (Hardroc)
Number of chip / wafer : 4
Number of wafer on ½ SLAB : 32

Total wafer power : 25 x 10^{-6} x 64 x 4 x 32
= **0.205 W**

FPGA power : **0.3 W nominal**
=> 2 W for test



Cooling / extremity of slab



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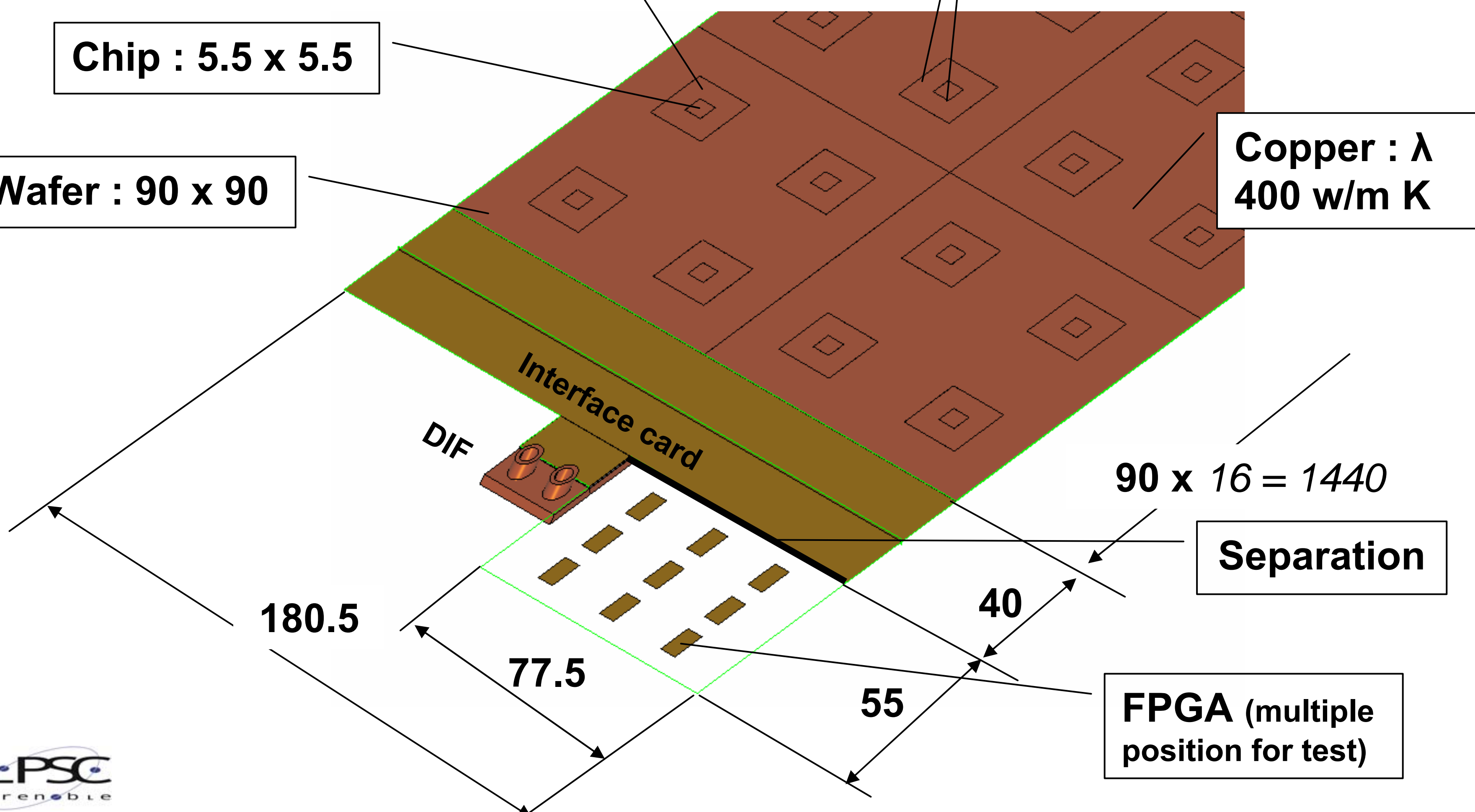
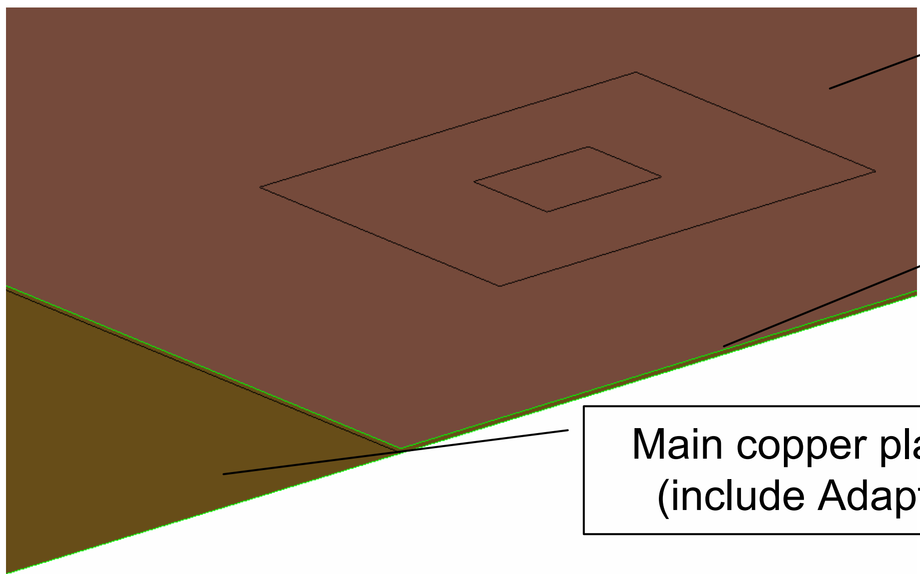
SLAB COOLING - EUDET

Model presentation:



SLAB COOLING - EUDET

Calorimeter for ILC



Upper copper plate : Ep = 0.1 mm

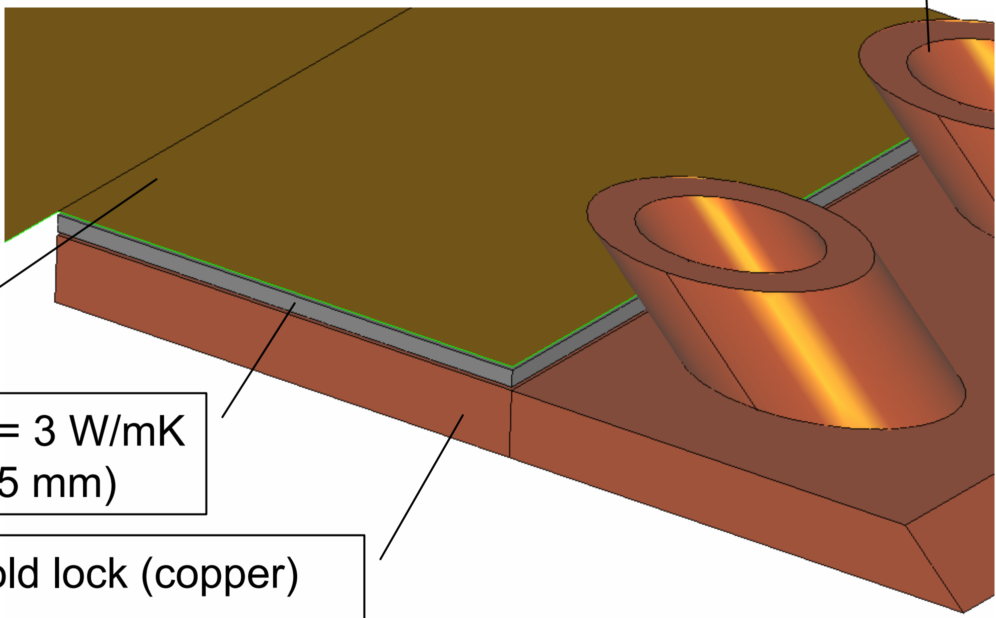
Full thermal contact between Upper and main copper plate

Main copper plate : Ep = 0.3 mm (include Adapter and DIF card

Fluid circulation pipe

Note : The thermal finite element model (shell element) is favorable near the ship power input.

The error estimation is 1°c.



Main copper plate

Thermal foam λ = 3 W/mK (thickness 0.5 mm)

Cold lock (copper)

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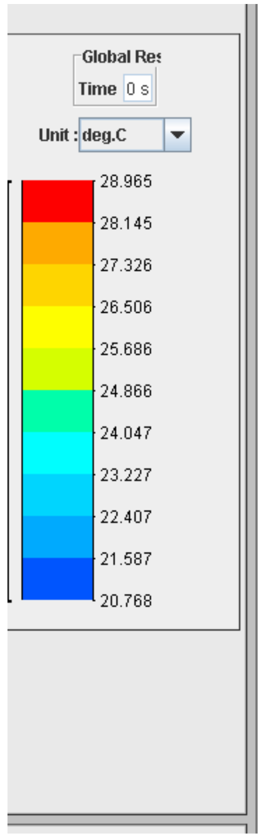
SLAB COOLING - EUDET

Load case 1 : Main plate : 0.3 mm; Upper plate : 0.1 mm; SHIP power : 0.205 W; FPGA power : **0,3 W => FPGA power distribution : 55 x 77.5 (KAPTON)**

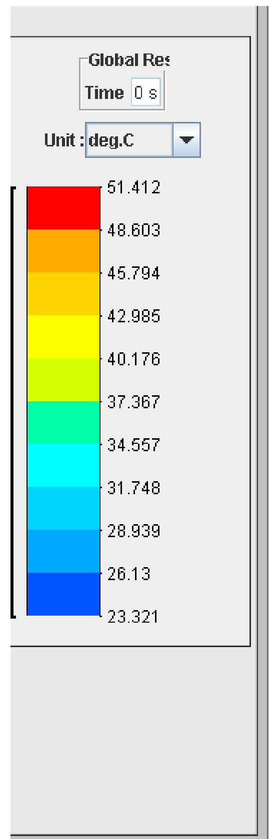


Temperature :
Full amplitude : 8.2°c
OK

SLAB COOLING - EUDET

CALICE — Calorimeter for ILC

Load case 2 : Main plate : 0.3 mm; Upper plate : 0.1 mm; SHIP power : 0.205 W; FPGA power : **2 W => FPGA power distribution : 55 x 77.5 (KAPTON)**



Temperature :
full amplitude : 28.5 °c

ship amplitude : 12 °c

OK

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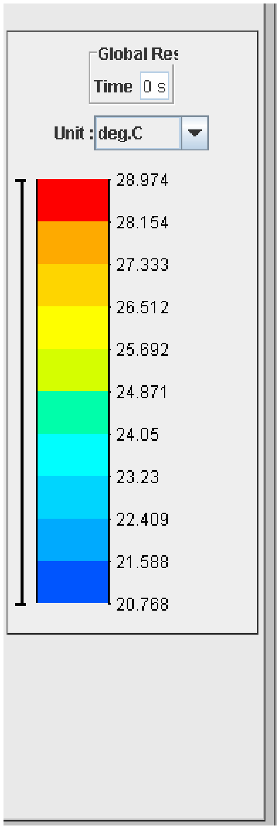
SLAB COOLING - EUDET

Calorimeter for ILC

Load case 3 : Main plate : 0.3 mm; Upper plate : 0.1 mm; SHIP power : 0.205 W; FPGA power : **0.3 W => FPGA power distribution : 10 x 5 extrema position**



Temperature :
Full amplitude : 8.2 °c

OK

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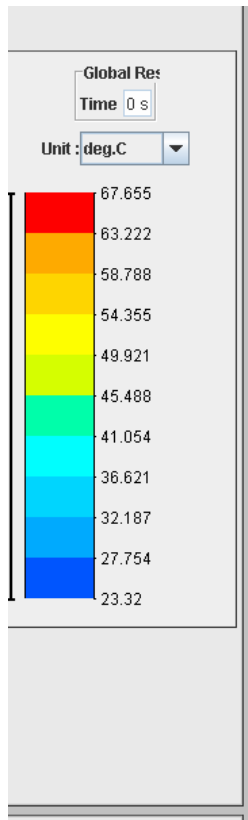
SLAB COOLING - EUDET

Load case 4 : Main plate : 0.3 mm; Upper plate : 0.1 mm; SHIP power : 0.205 W; FPGA power 2 W **=> FPGA power distribution : 10 x 5 extrema position through foam ep 0.2 mm**

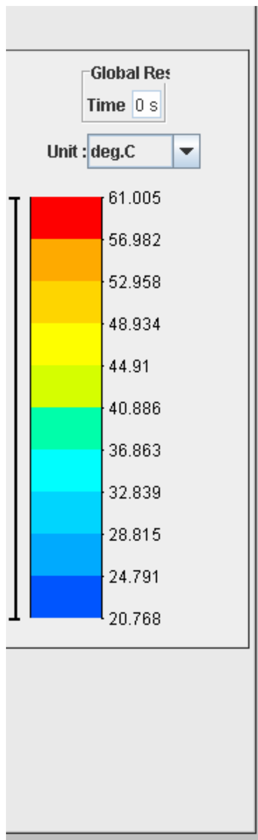


Temperature :
Full amplitude : 44 °c

Ship amplitude : 20 °c

SLAB COOLING - EUDET

Load case 5 : Main plate : 0.3 mm; Upper plate : 0.1 mm; SHIP power : 0.205 W; FPGA power 0.3 W **=> FPGA power distribution : 10 x 5 extrema position through PCB EP 1.6 mm (λ = 0.26 W/mK) and foam ep 0.2 mm**



Temperature :
Full amplitude : 40 °c

Ship amplitude : 15 °c

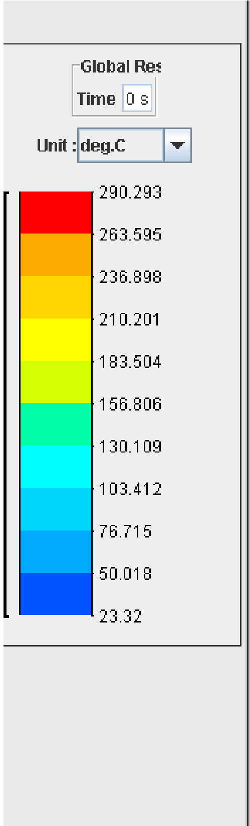
OK but…

…better cooling if direct contact with FPGA !

SLAB COOLING - EUDET

Calorimeter for ILC

Load case 6 : Main plate : 0.3 mm; Upper plate : 0.1 mm; SHIP power : 0.205 W; FPGA power 2 W => **FPGA power distribution : 10 x 5 extrema position through PCB EP 1.6 mm and foam ep 0.2 mm**



NO

Cooling to be in contact with FPGA !

Temperature :
Full amplitude : 270 °c

SLAB COOLING - DEMONSTRATOR

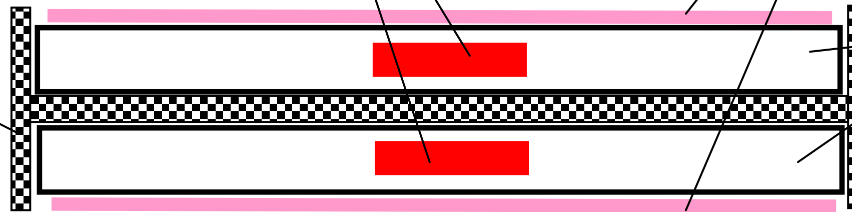
CALICE Calorimeter for ILC

DEMONSTRATOR design (more questions …)

To reproduce as precisely as possible these tests in simulations:

Hot point + temperature sensor

Copper



H composit

PCB

Q1 : For simulations: location and dimensions of heat sources & probes

Q2 : FPGA real consumption and position

Q3 : Distance between Hot point and temperature sensor

Q4 : Hot point / Copper liaison (thermal paste), real thickness ?

Q5 : Thermal paste conduction = 0,4 W/mK ?

Q6 : (for EUDET too) PCB thickness up to **1** or 1.2 mm - Hole in copper/chips : 18 x 18 mm ?

Q7 : Bumpy resin for chips on wire-bonding.. => thermal paste only on chips ?

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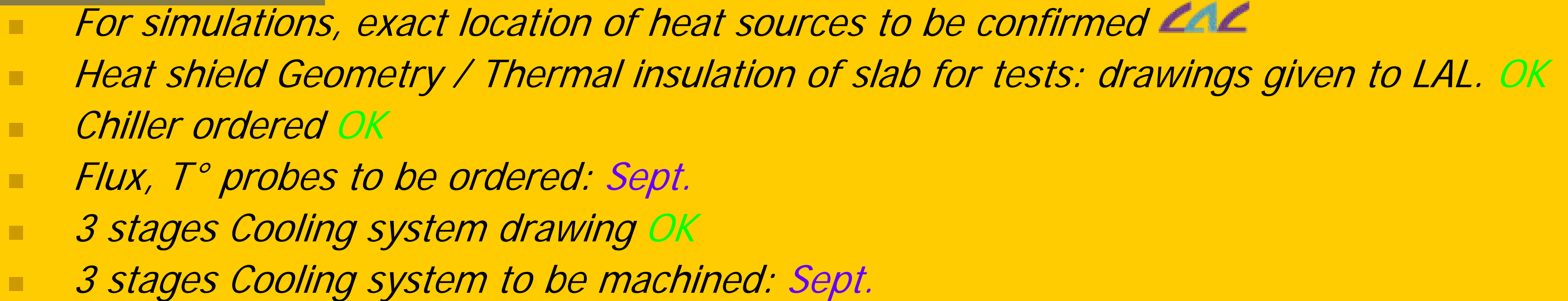
SLAB COOLING

Calorimeter for ILC

Demonstrator

To sum-up, in order to install the cooling system and to correlate with numerical simulations:



Goal: **- Test of cooling system: mechanical aspect and performances**
- Optimization of simulation: conductivities, materials, geometries

EUDET

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Backend system (DIF support): **Confirmation of FPGA consumption and position…**

EUDET module: structures to be assembled and tested with cooling system.

Detector slabs **integration for thermal tests** with tuned power, copper shields with specific geometry and temperature probes.

- Interface card ? Dimensions and specificities ?
- DIF: integrated or not, supporting, jumble…

Goal:

- **Simulations to be performed with demonstrator's approved values to validate the whole cooling of EUDET.**

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