Ecal Design Note – Comments on first draft

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Ecal Design Note

Editorial Work: R.P.

Chapter	Author	Max. Pages
1) Introduction and Purpose	R.P.	1
2) Overall Design	Marc, Aboud, R.P.	3
3) Structures and Moulds	Marc	3
4) Si Wafers	Remi	3
5) SKIROC Chip How detailed?	Julien F.	2
6) PCB and ASU + Interconnection How detailed?	Julien F., Maurice, Patrick	3
7) DIF Card	Maurice, Bart	2
8) Gluing Wafer <-> PCBs	David, Ray	2
9) Heat Dissipation of EUDET Module	Denis, Julien G.	2
10) Assembly of Prototype	Aboud	3
11) First Validation Steps – The Demonstrator	R.P., Marc	3
12) Conclusion and Outlook	R.P.	2

Note should describe the state of the Art of today and what realistically can be built
Not what we may expect in one year, note improvements are always welcome

Deadline for submission 30th of September

1) Introduction and Purpose (+Abstract)

- Remark on Demonstrator is missing

- Remark that project is co-funded by national agencies

- Fairly complete
- Mentioning of Demonstrator (might be left for Introduction)

- Remark on Logistics?

To be integrated into the Integration Chapter (10) and left for an 'After'-Amsterdam Update

- Looks fairly complete

- Too much on Wafers for Prototype
- Not clear what is past and what is present
  Refer to Ecal Paper and list the conclusions and discuss mainly the work for the EUDET Module, e.g. Tests of Hamamatsu Wafers

- Important Reference to power distribution

  -> To be described in Section 6
  Parapgraph on HV Capton Feeding be Remi and Marc

Title to be changed to: DIF and Adapter Cards

- Looks fairly complete

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- Do we still consider the Thermal grease to be deposited on the Chips?

Bonded wires will be embedded in resin (to be described by Julien F.)
Thermal grease on top of resin (to be described by Denis, Juliem G.)

Details on wording and coherent text to be discussed among corresponding authors (+Marc and R.P.)

- Looks fairly complete

- Time Schedule is missing, approximate time needed for each step

(General) Time Schedule left for 'After' Amsterdam update

Paragraph on Quality Control and Database to be added by Aboud

- Maybe the largest single chapter of the note

- Considered as a 'document within a document'
  All items discussed before should be resumed in terms of
  their role/realisation for the demonstrator (apart from SKIROC Chip)

- More reference to the document itself

- (Still) contains 30th of June 2009 as deadline!!!

  Keep this deadline for the design note

- Timetable in an Appendix?

  Left for an 'After Amsterdam' Update