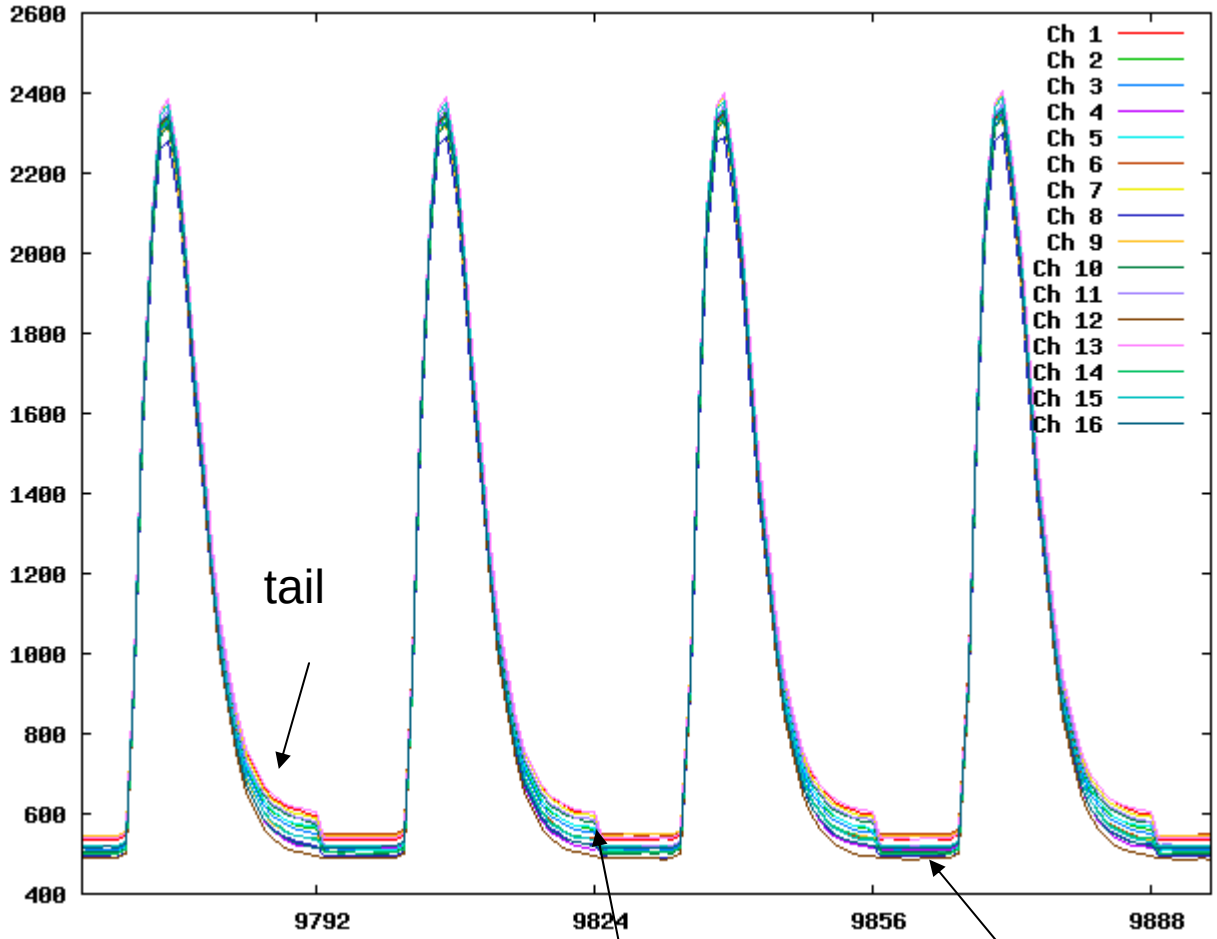
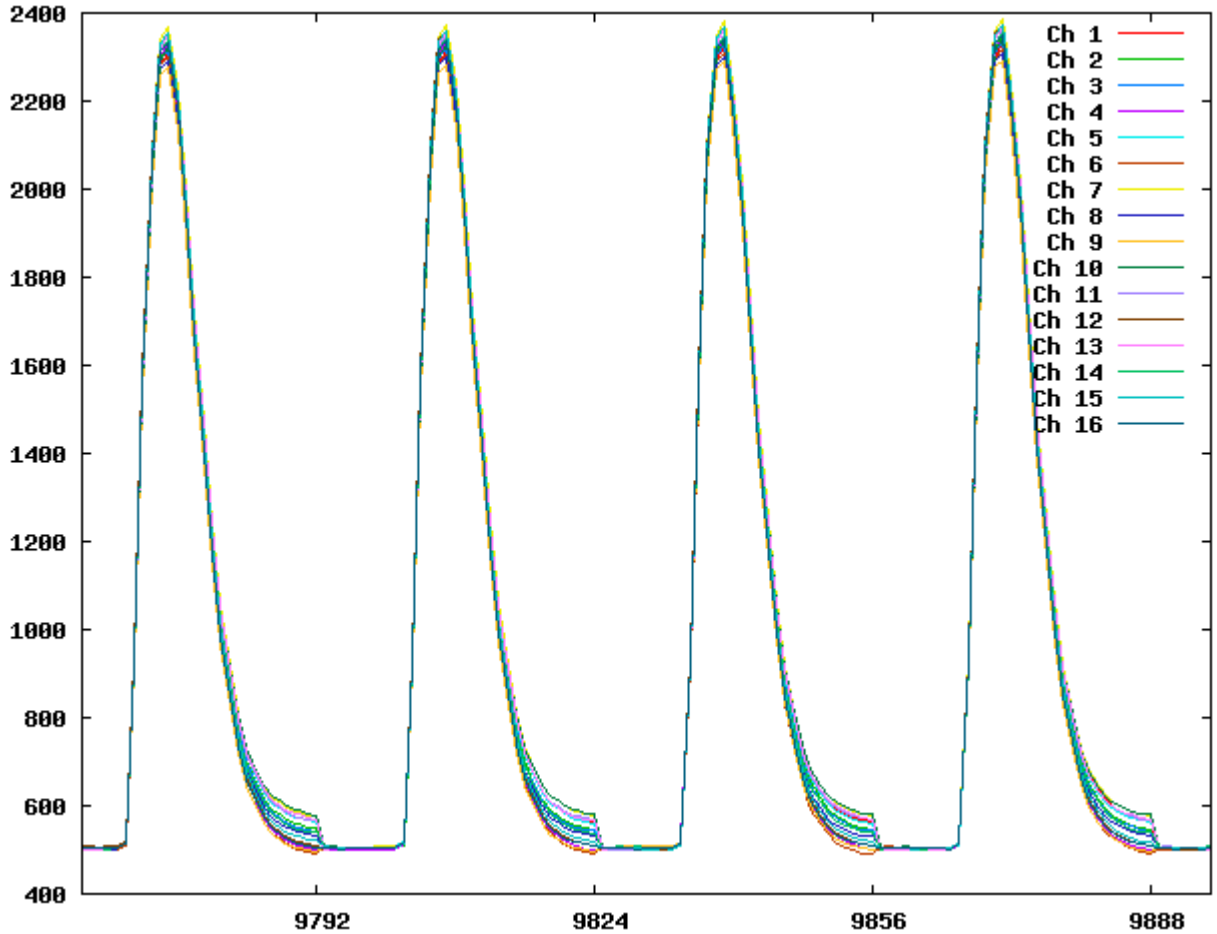
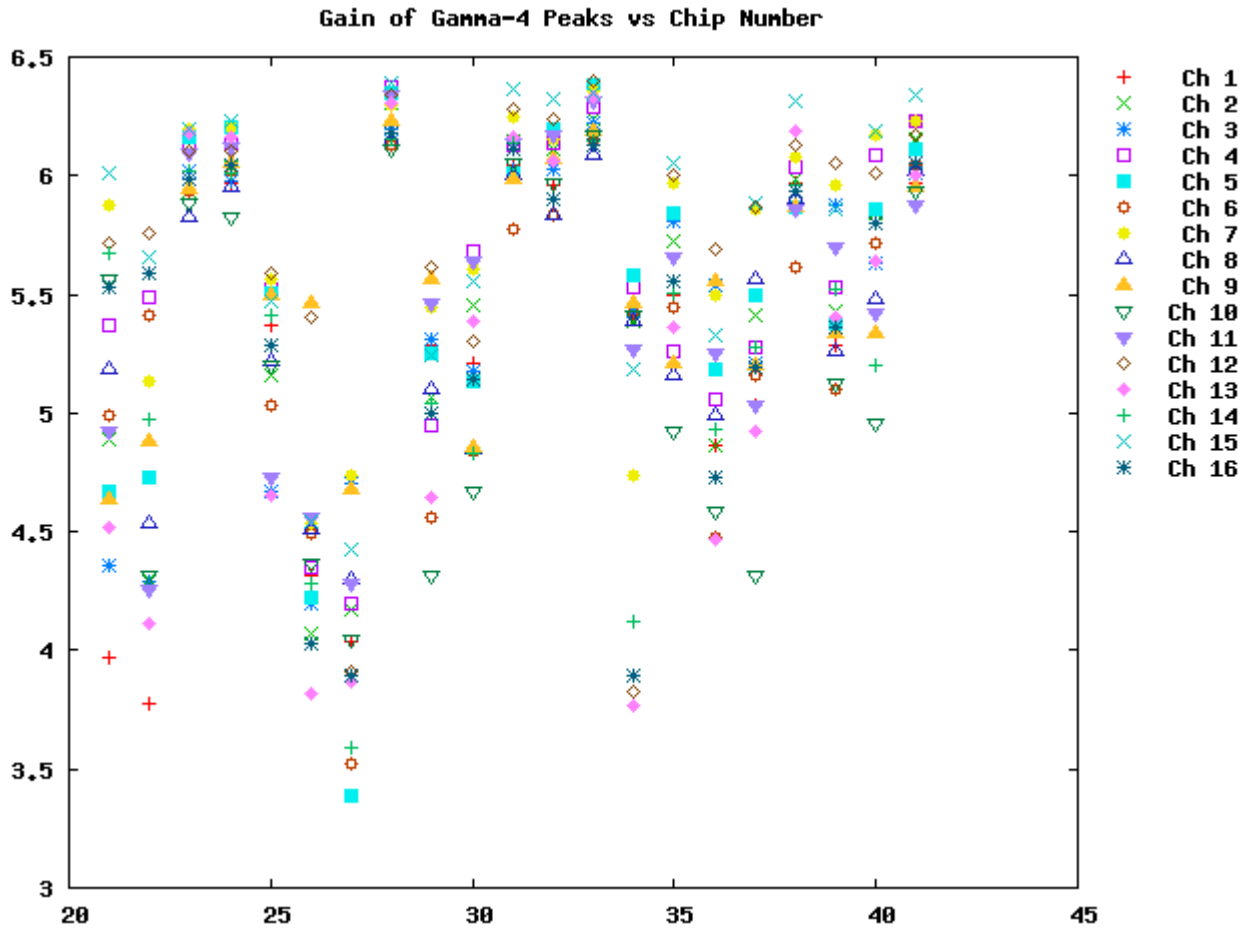
Sequence of test pulses. 12mV/fC, long shaping, long PA-decay



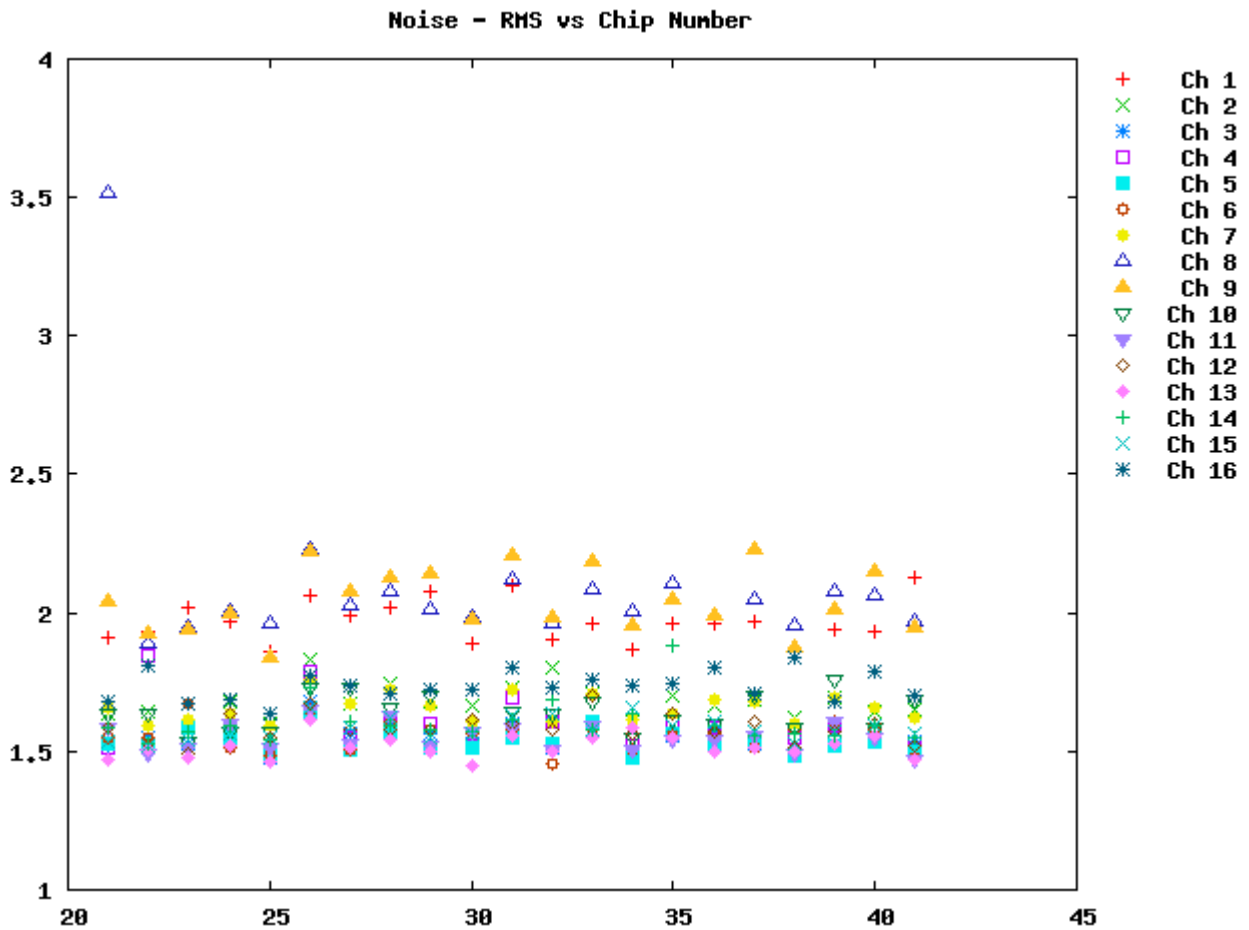
Tester digitizes 12 bit, 40MHz



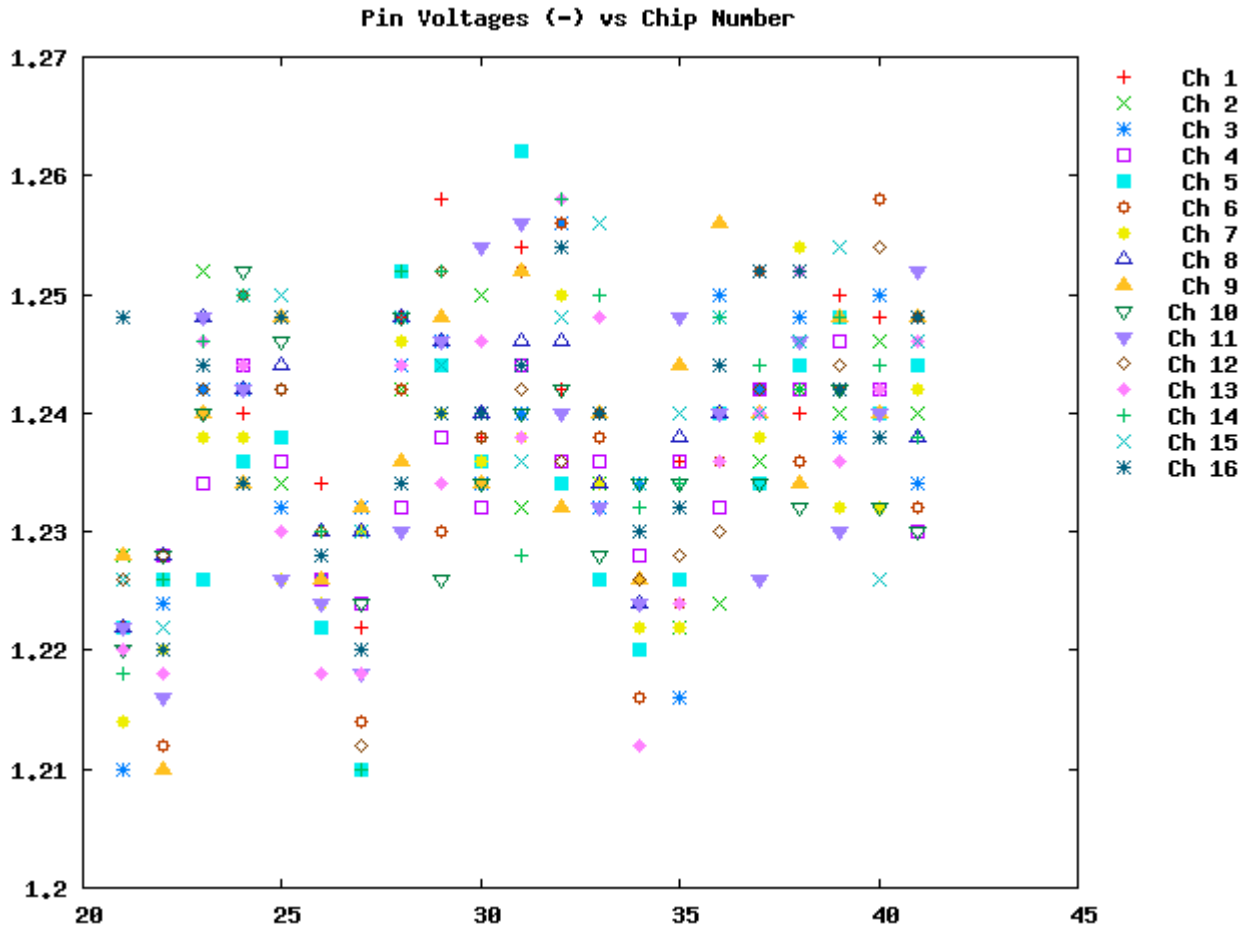
Renormalise DC levels by measured values



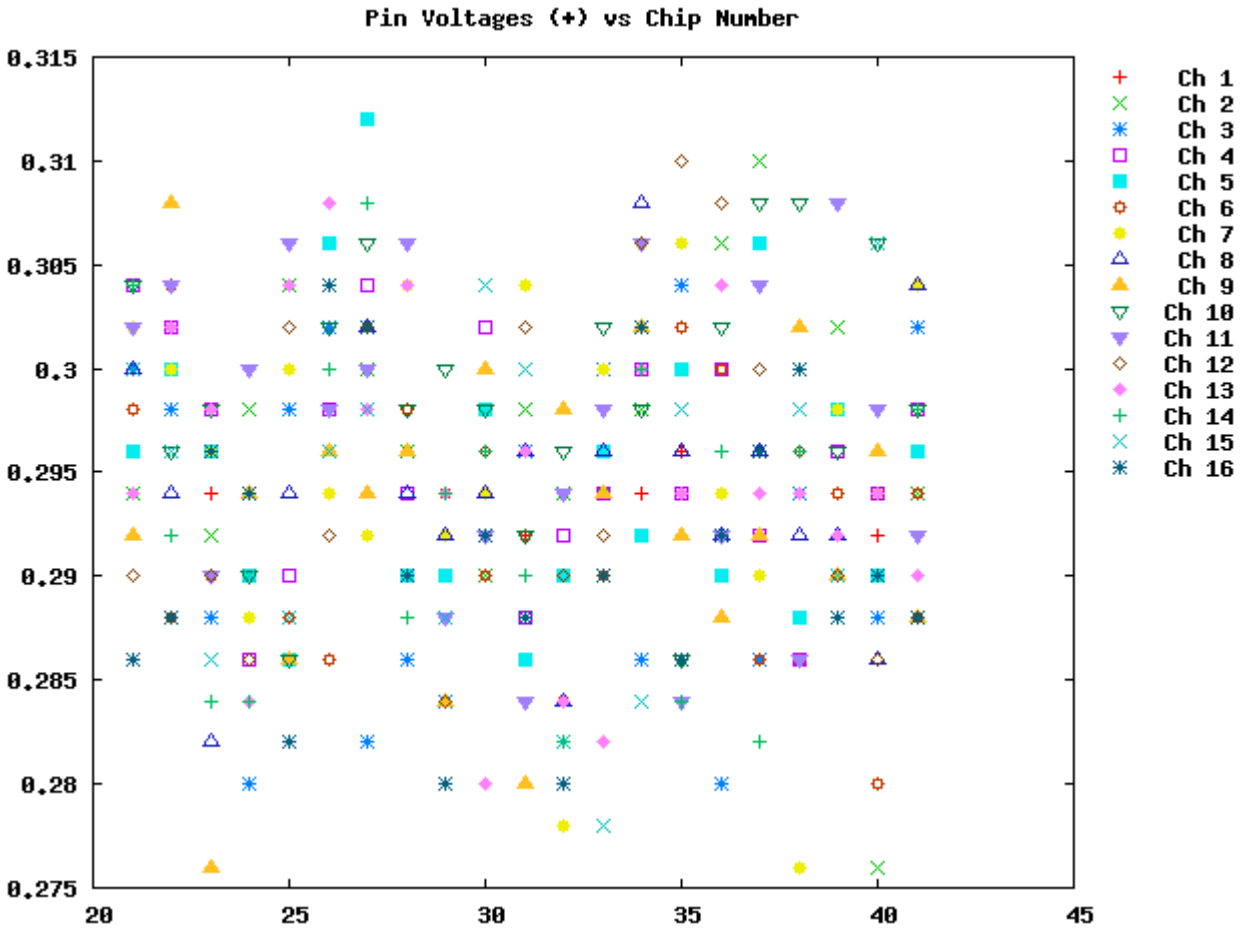
Pulse fitting does not work properly. Believe it because of the tails
We do the judgement from the previous figure if we can not get it to work automatically.



Noise RMS in ADC channels. Some setupdependence

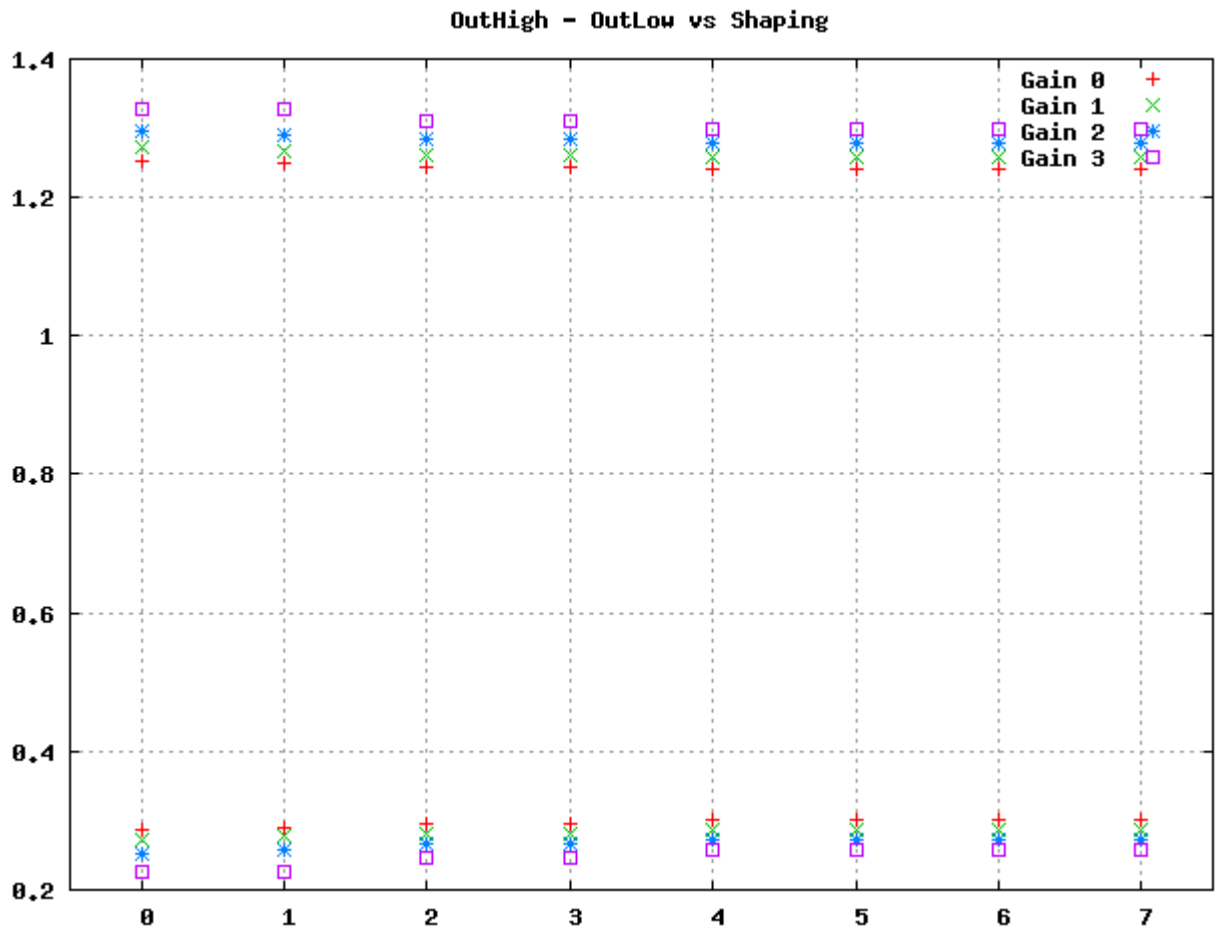


DC levels on low ouput.+/-20mV in chip, +/-50MV between chips.
Shaping time and gain shanges DC levels

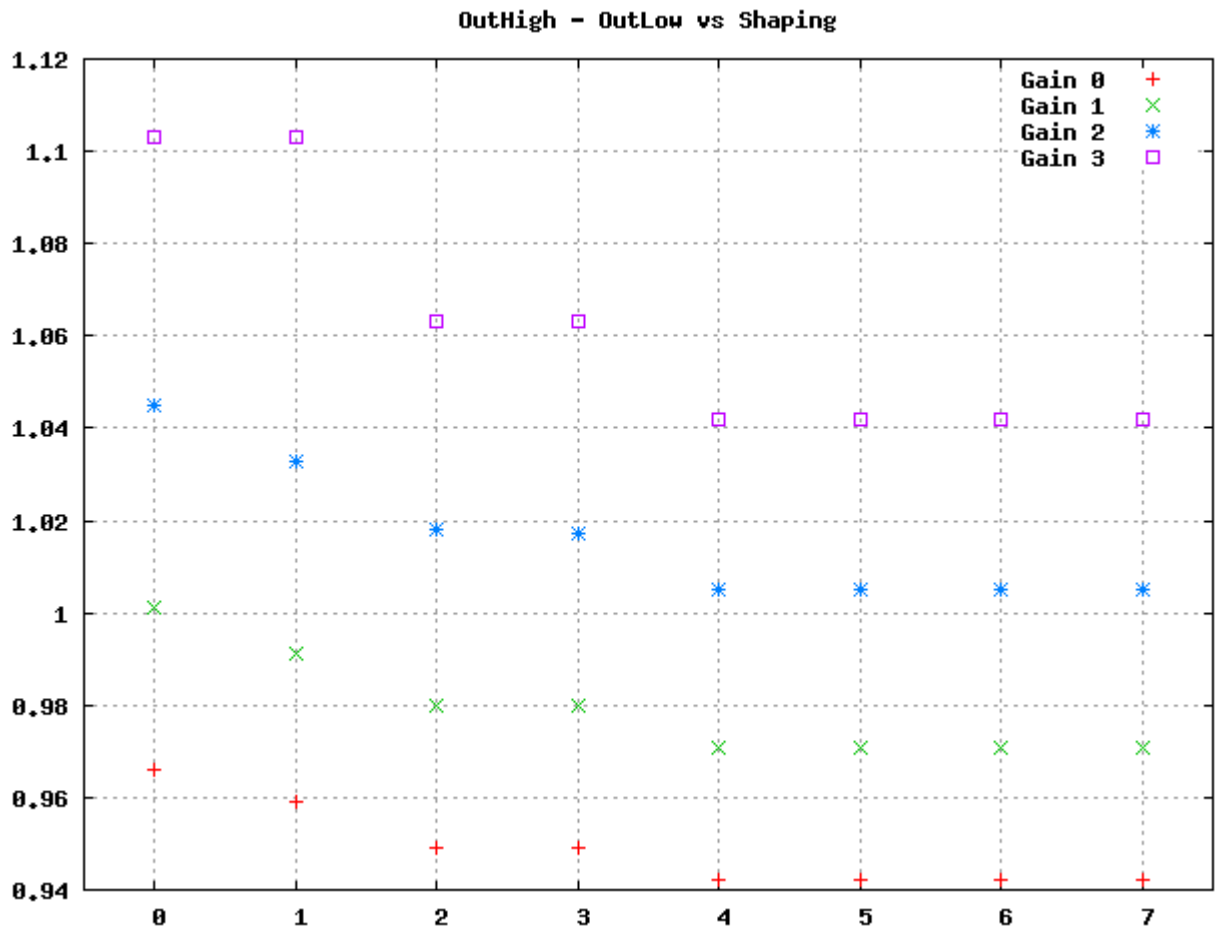


DC levels on High output

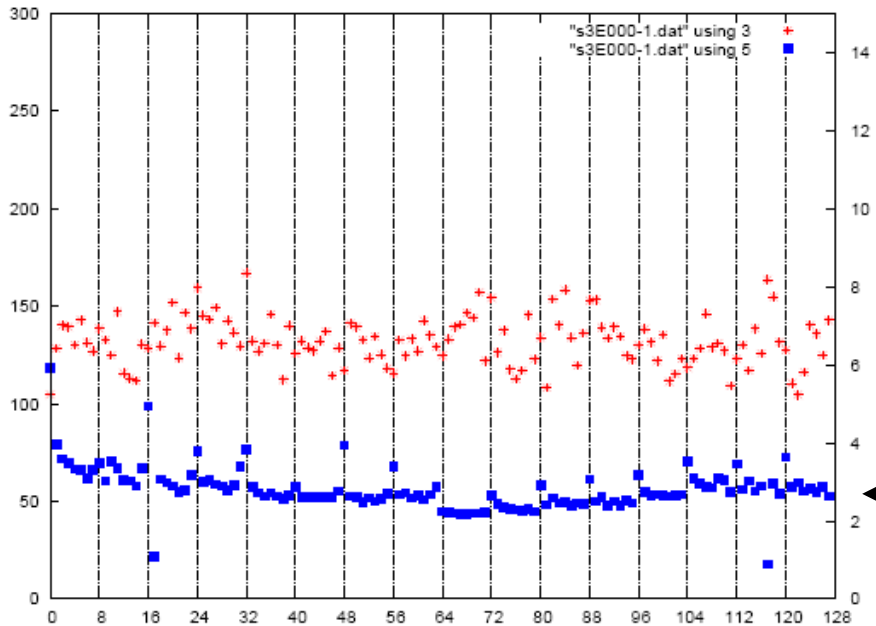
One channel, different settings



Changes more with gain setting than shaping time


OutHigh - OutLow vs Shaping
Gain 0
Gain 1
Gain 2
Gain 3
1.12
1.1
1.08
1.06
1.04
1.02
1
0.98
0.96
0.94
0
1
2
3
4
5
6
7

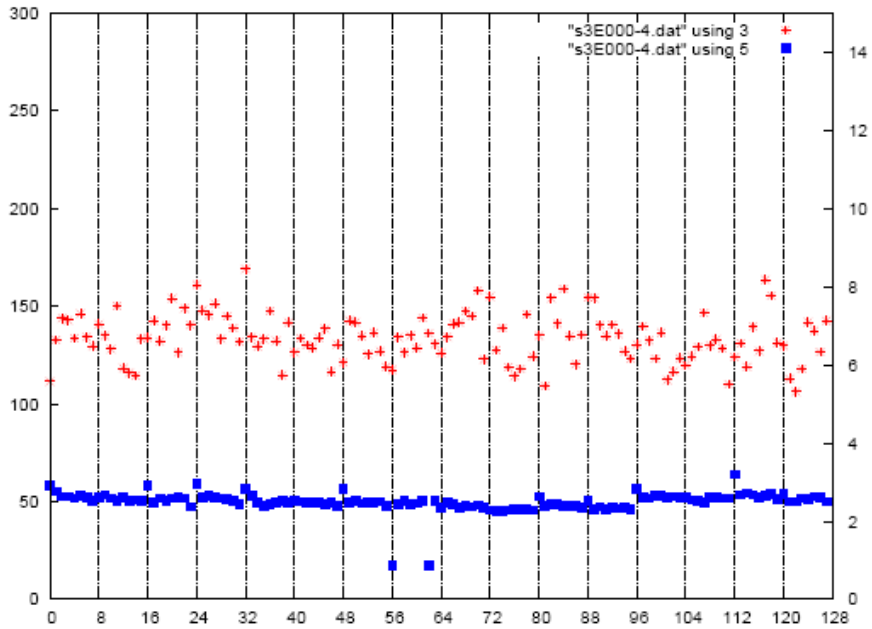
FEC test



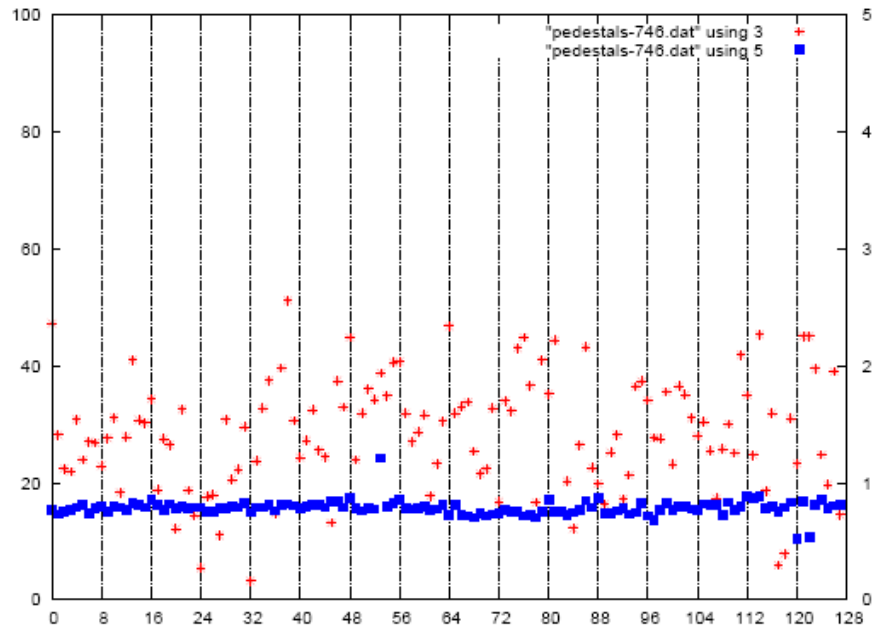
RMS noise

All 128 channels, cable connected

Highest gain, shortest shaping (wrong polarity)



Same setting, local grounding of ALTRO analog & digital



On the small chamber, 12mV/fC, longest shaping, right pol.